EOS/ESD Association, Inc.

Electrostatic Discharge (ESD) Technology Roadmap

EOS/ESD Association, Inc.
218 West Court Street
Rome, NY 13440

Published January 2024

CAUTION NOTICE

Electrostatic Discharge Association (ESDA) standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining the proper product for his particular needs. The existence of such standards and publications shall not in any respect preclude any member or non-member of the Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication that is published by the Association preclude its voluntary use by non-members of the Association, whether the document is to be used either domestically or internationally. Recommended standards and publications are adopted by the ESDA in accordance with the ANSI Patent policy.

Interpretation of ESDA Standards: The interpretation of standards in-so-far as it may relate to a specific product or manufacturer is a proper matter for the individual company concerned and cannot be undertaken by any person acting for the ESDA. The ESDA Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacturers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard.

DISCLAIMER OF WARRANTIES

THE CONTENTS OF ESDA'S STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND ESDA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESSED OR IMPLIED, OF ANY KIND, WITH RESPECT TO SUCH CONTENTS. ESDA DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, AND NON-INFRINGEMENT.

DISCLAIMER OF GUARANTY

ESDA STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLERS' OR USERS' OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND ESDA DOES NOT UNDERTAKE TO GUARANTEE THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURERS' PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA EXPRESSLY DISCLAIMS ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

LIMITATION ON ESDA's LIABILITY

NEITHER ESDA, NOR ITS PRESENT OR FORMER MEMBERS, OFFICERS, EMPLOYEES OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF, OR IN CONNECTION WITH, THE USE OR MISUSE OF ESDA STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING, WITHOUT LIMITATION, LOSS OF DATA, INCOME OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY, AND CLAIMS OF THIRD PARTIES.

Published by:

EOS/ESD Association, Inc.
218 West Court Street
Rome, NY 13440

Printed in the United States of America

TABLE OF CONTENTS

Figures

EOS/ESD Association, Inc.'s Electrostatic Discharge (ESD) Technology Roadmap

1.0 SYNOPSIS

This document is divided into two main sections. The first provides estimates of future ESD thresholds of semiconductor devices and the potential impact on ESD control practices. These levels are strongly technology and design-dependent and need to be periodically revised in the context of advances in the electronics industry. The threshold estimates discussed in this roadmap are intended to reflect the prevailing trends in semiconductor technology as viewed by selected industry leaders. As in previous versions of this document, the integrated circuit (IC) industry is emphasized. Other major electronics industry segments are also experiencing increased ESD sensitivities (lowering ESD thresholds). Some examples are optoelectronics (light-emitting diodes, lasers, and photodiodes), printed circuit board assemblies, and thin-filmed-transistor-based displays and circuits. However, ESD trend information is not usually readily available for these devices, and the standardized ESD tests are not defined or broadly applied.

This document presents the thresholds as "roadmaps" of estimated threshold changes until 2030. These projections provide a view of future device protection limitations driven by circuit performance requirements and technology scaling effects. It also provides a common view of expected device ESD performance variations as viewed by device (IC) suppliers and original equipment manufacturers (OEMs), and other users of ICs. Finally, these trends point to the need for continued improvements in ESD control procedures and compliance. Some linkage of these trends to process capability is also discussed, as is progress in other ESD events characterization such as system-level, charged-board events, and cable discharge events.

The document's second part contains information on device testing trends and characterization from the ESDA and ESDA/JEDEC teams working on these methods. It is followed by an outlook on important trends in the semiconductor industry looking towards 2030. The roadmap closes with a section on electronic design automation (EDA), an important contributor to reliable and robust ESD and latch-up design.

2.0 DEVICE THRESHOLD TRENDS

2.1 Overview

In the late 1970s, ESD became a problem in the electronics industry. Low threshold level ESD events from people were causing device failures and yield losses. As the industry learned about this phenomenon, device design improvements and process changes were made to make the devices more robust and the processes more capable of handling these devices.

During the 1980s and early 1990s, device engineers, after going through a learning curve, were able to create protection structures that could withstand higher levels of ESD stress and thus made devices less sensitive to ESD events. Both device engineers and circuit designers were able to identify key technology parameters and design techniques that helped them develop more robust devices.

However, in the mid to late 1990s, the requirements for increased performance (devices that operate at 1 GHz and higher) and the increase in the density of circuits (Moore's Law) on a device caused problems for traditional ESD protection circuits because they require additional area and add capacitance. This was exacerbated by the continued scaling of the technologies toward sub-100 nm feature sizes to achieve higher density and performance. The situation worsened with the advent of IC chips with sub-50 nm technologies rapidly going into production. With the demand for high-speed internet operations, large, high pin count (> 1000 pins), packaged devices containing high-speed SerDes (HSS) input/outputs (IOs) that need to operate at 10-15 gigabit per second (Gbps) were introduced. These IOs reached 20-30 Gbps at the 22 nm and 16 nm technology nodes, and with today's advanced technology nodes at 5 nm and 3 nm and beyond, HSS IO in the 112 Gbps to 224 Gbps are more prevalent. Consequently, the human body model (HBM) and charged device model (CDM) target levels had to be adjusted to accommodate these new IO performance levels.

The wireless connectivity of the world has driven both an increase in radio frequency (RF) applications and higher bandwidth requirements. In the mobile space, 4G LTE utilizes frequency bands up to 5.8 GHz. With the introduction of millimeter-wave 5G technology, the frequency bands go into the 28 GHz to 60 GHz regime. ESD protection must be balanced with performance for these RF applications since these higher frequencies cannot tolerate additional capacitive loads on signal nodes. Any ESD robustness built into the RF pins is often co-designed with the matching network for the application. This almost invariably leads to reduced HBM and CDM withstand voltages. The expectation is that these trends will continue as increased circuit performance will take precedence over ESD protection levels. HBM and CDM requirements must comprehend these technology trends for future device qualification.

2.2 Device ESD Threshold Roadmaps

The following graphs show the device ESD design sensitivity trends based on the most relevant and important ESD models used by device manufacturers in the device qualification process: HBM and CDM. The sensitivity limits are projections by engineers from leading semiconductor manufacturers.

2.2.1 Human Body Model (HBM) Roadmap

The projections for HBM design (typical min and max) through 2030 are indicated in Figure 1. Although design improvements were made from 1978 through 1993, advanced circuit performance effects started to take place around the mid-'90s, eventually degrading the achievable HBM levels. The maximum levels represent what is typically possible from technology scaling, and the minimum levels represent the constriction from meeting the circuit performance demands.

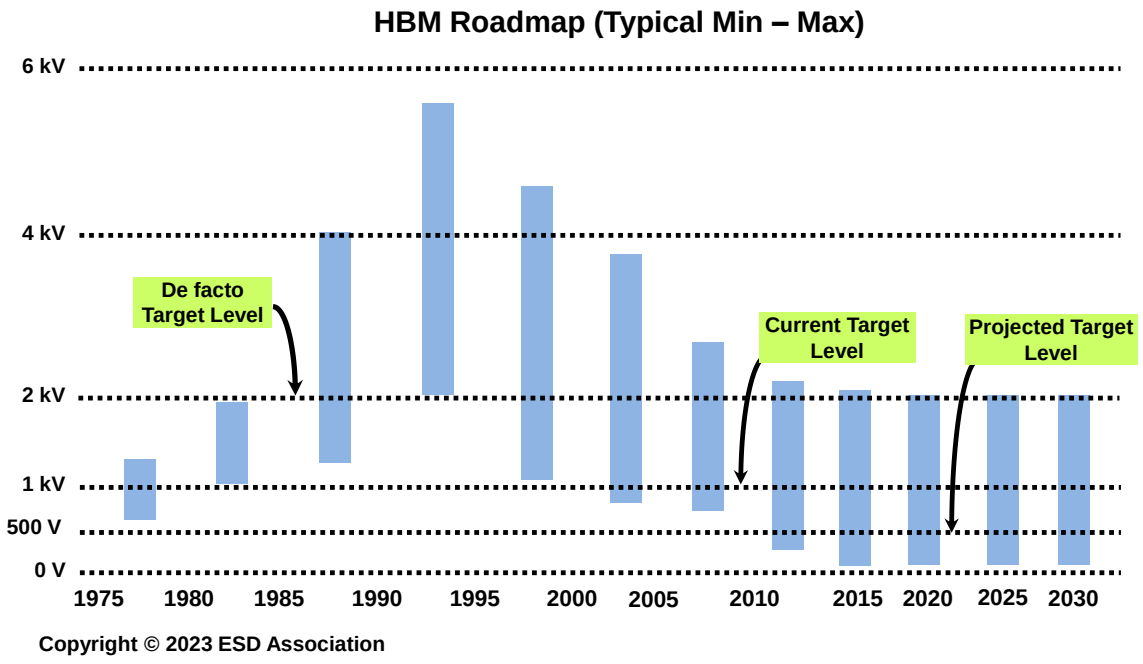

Figure 1: Overall Human Body Model Sensitivity Limits Projections

Figure 2 presents a zoomed-in look at 2010 through 2030. Additionally, Figure 2 shows the estimated ESD control capability for HBM during the same time based on the levels of HBM controls that may be in place. Significantly, HBM control methods in today's production areas have reduced the HBM target level from 2 kilovolts to 1 kilovolt [1]. Even with this *de facto* target, some high-

performance devices may only have a 100-volt to 200-volt threshold. In the 2020 roadmap, it was suggested that a 500-volt limit might be necessary. Looking ahead to 2030, it is unclear whether another drop in the HBM target level will be necessary for anything other than very high-performance IO, such as 224 Gbps SerDes and RF applications. Implementation of improved HBM controls using the limits and requirements in ANSI/ESD S20.20 [2], IEC 61340-5-1 [3], or JEDEC JESD625 [4] will continue to be important to mitigate the risks of lower HBM protection levels. As shown in Figure 2, below 100 volts is a "custom controls" region in which non-standard process-specific controls are necessary. These controls are very specific to the environment and may include, but are not limited to, tighter ESD control limits and tighter frequency of compliance verification. Performing process capability assessments, as discussed in Section 2.5, has become even more important to address higher performance IO risks in manufacturing.

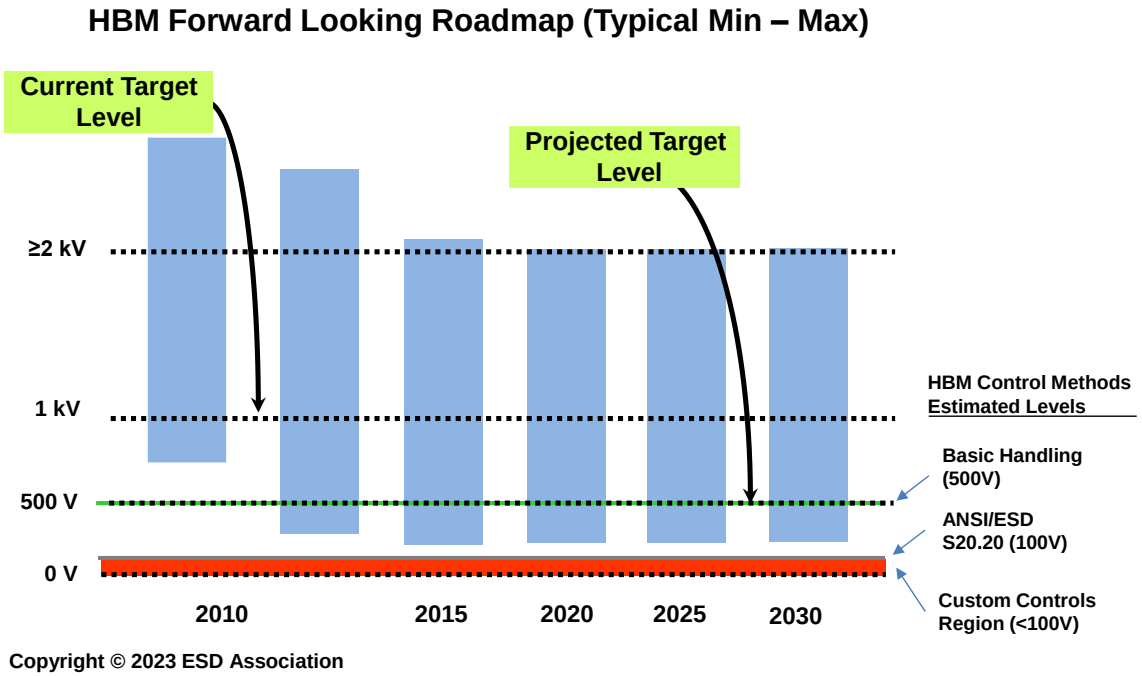

Figure 2: 2010 to 2030 Human Body Model Sensitivity Limits Projections

NOTE: The current target level is 1 kilovolt.

A closer observation of Figure 2 shows that there appears to be little change in the typical range for HBM sensitivity limits looking ahead to 2030, as compared to 2025, 2020, or even 2015. While the *range* may not change dramatically by 2030, the *distribution* of products within this range will continue to vary. This results from some companies remaining on traditional technologies and those who continue to push for technological advancements through the need for higher-performance IO devices.

2.2.2 Charged Device Model (CDM) Roadmap

The technological impact on CDM comes from the required IO speeds and package size effects. Larger packages will experience higher discharge currents at a given stress voltage level. Larger packaging is also possible as more companies explore 2.5D and 3D technologies. Figure 3 illustrates the impact of application and IC packaging on the achievable CDM robustness for package exposed "external" pins and "internal" pins of 2.5D and 3D integrated ICs. The observed impact becomes somewhat independent of the technology node starting around 22 nm as the reduction in oxide breakdown voltages is saturating. It becomes more dependent on the IO performance demands dictated by the loading capacitance. For package exposed pins, the color

scheme adopted in Figure 3 is based on the validation that 250-volt CDM is safe for production areas [5]. This map will change as package sizes become even larger. For example, note that for today's packages of 3000 pins (~3000-3500 mm^2) or more (not uncommon for a microprocessor) in a land grid array (LGA) or ball grid array (BGA), very high-speed IOs might barely meet a CDM target level of 125 volts. An additional package effect, decreasing thickness, was not included here for simplicity. However, it should be noted that this can also impact the peak currents seen by a device independent of the change in package area. In certain market segments, such as in the mobile market space, where the Z-height of the package is critical to market acceptance (for example, phones, watches, and laptops), this package thinning has more impact.

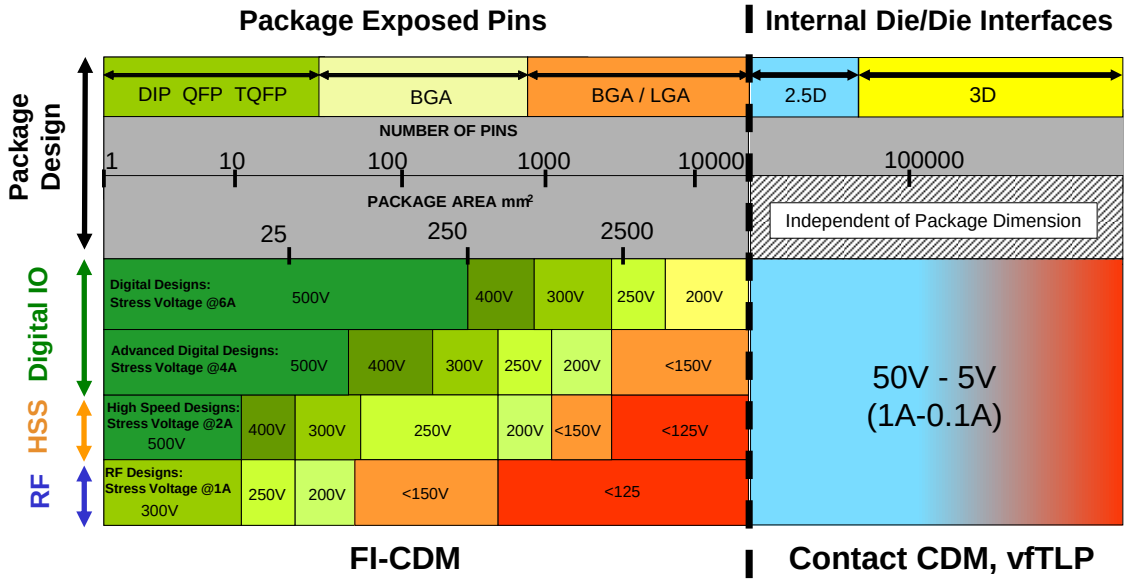

Figure 3: Combined Projected Effects of IO Design and IC Package Size on CDM

There is often a delicate balance between CDM robustness and RF performance in the RF space. Exacerbating this CDM sensitivity is that capacitors, frequently damaged by CDM transients, are widely used in RF designs for DC blocking, matching networks, filtering, and other applications related to the application functionality. Any circuit that would be used to protect these capacitors will ultimately degrade linearity, insertion loss, or otherwise impact the integrity of the RF signal. As higher bandwidth RF applications become more widespread, the achievable CDM performance will likely decrease further.

With this update to the technology roadmap, an extension to Figure 3 has been added introducing internal die-to-die (D2D) interfaces. This is an important extension to CDM risks introduced by heterogeneous packaging. For internal pins, the provided range is based on the area constraints for internal IO that only allow the use of very little to no additional area to enable minimal CDM robustness. Often, this minimal CDM robustness is only achieved by the self-protection capability of the connected circuitry. The testability during ESD characterization is limited because of the huge number and small size of internal pins. Different testing methods like contact CDM or very-fast transmission line pulsing (TLP) are applied to assess the robustness of the pins.

The projections for CDM sensitivity levels (typical min and max) at the IC level (packaged exposed pins) until 2030 are indicated in Figure 4. The figure shows that the current CDM target is 250 volts, reduced from the previous 500 volts from the early 2000s. A target of 125 volts is needed for a subset of pins already today, primarily driven by the need for very high-performance IOs.

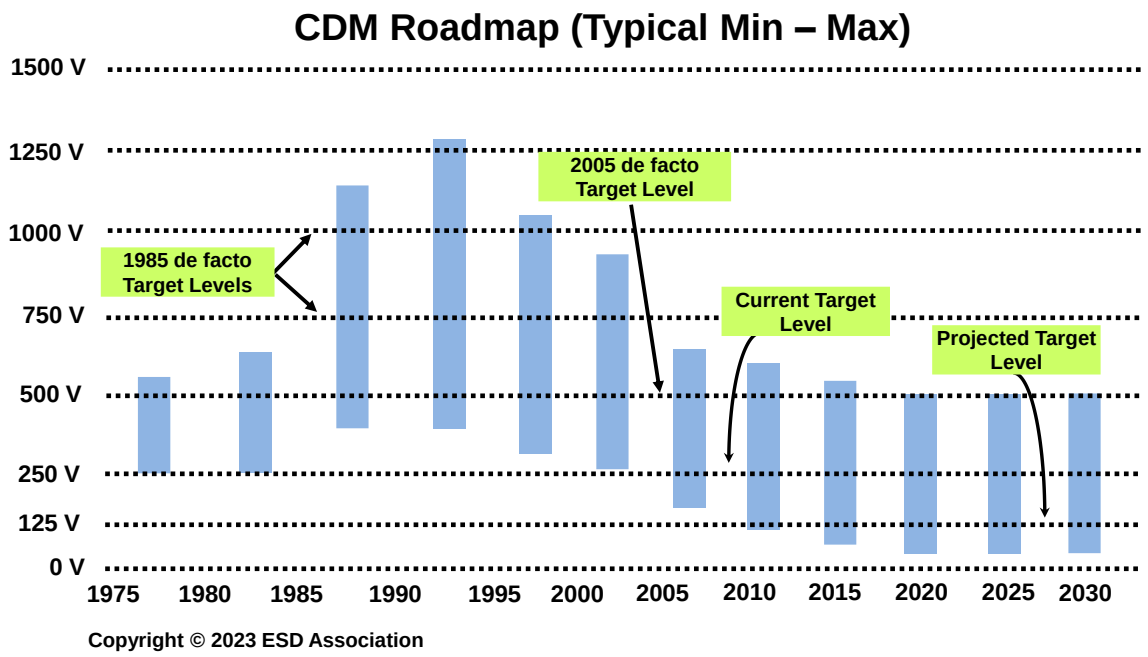

Figure 4: Overall Charged Device Model Sensitivity Limits Projections

As with HBM projections, a magnified look at CDM for 2010 and beyond is presented in Figure 5. The ESD control capability for CDM during the same period is also shown. Implementation of advanced CDM control methods and a more thorough process assessment are not only more critical but have become nearly mandatory for some products.

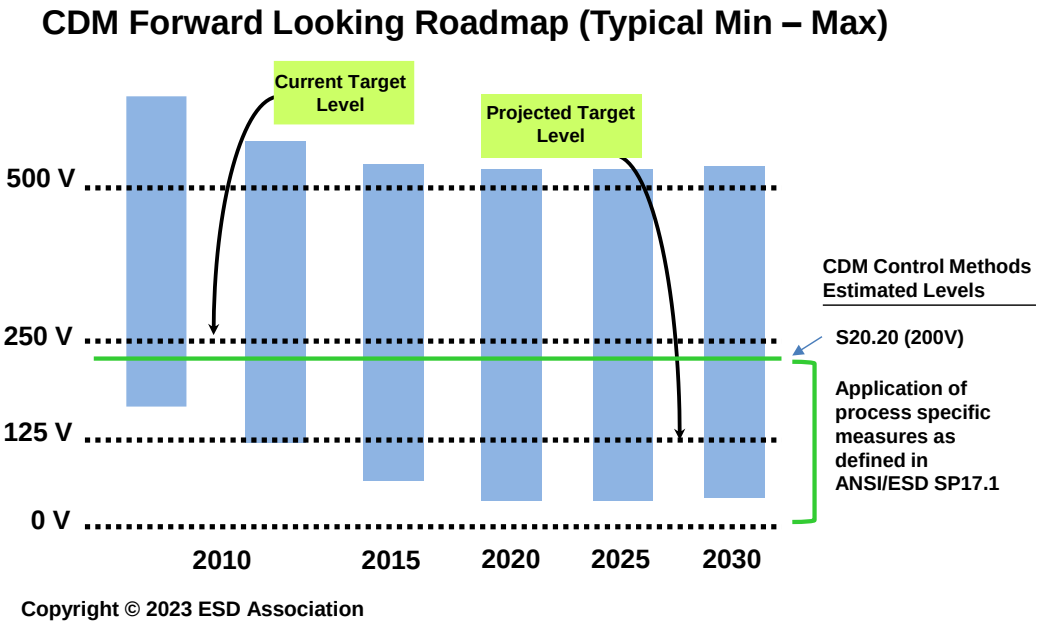

Figure 5: 2010 to 2030 Charged Device Model Sensitivity Limits Projections

NOTE: The current target level is 250 Volts.

A closer observation of Figure 5 might suggest that when looking ahead to 2030, there will be no significant change in the typical range for CDM sensitivity limits compared to 2020 or even 2015. While the belief is that the range may not change dramatically by 2030, the *distribution* of products within this range can vary with a change in the mix of companies remaining on today's traditional technologies. This includes those who continue to push for technological advancements through the need for higher-performance devices and growth in package size/complexity through multichip packages such as 2.5D and 3D.

Figure 6 is a first look into how this distribution of products could conceivably look by 2030. As technology/application-specific IO/package scaling needs constantly change, this updated edition of the roadmap also took a fresh look at the current situation. As such, the 2025 mix has also been modified from the 2020 projections. It is believed that the projections for 2025 did not include sufficiently the increasing number of 2.5D and 3D integrated products. Therefore, the 2025 distributions are adjusted up in the less than 125 volts range.

It is predicted that there will be a larger increase in the number of products in the less than 125 volts range and only small decreases in the number of products in the greater than 500 volts range when looking ahead to 2030. Therefore, the bottom two groups of CDM distributions are of deeper concern. Because of the large number of pins classified as internal, especially chiplets will be designed and manufactured with strongly reduced CDM robustness compared to ICs that only have externally packed exposed pins. The industry needs to continue improving process assessment capabilities to be better prepared for this larger population of sensitive CDM devices by 2030.

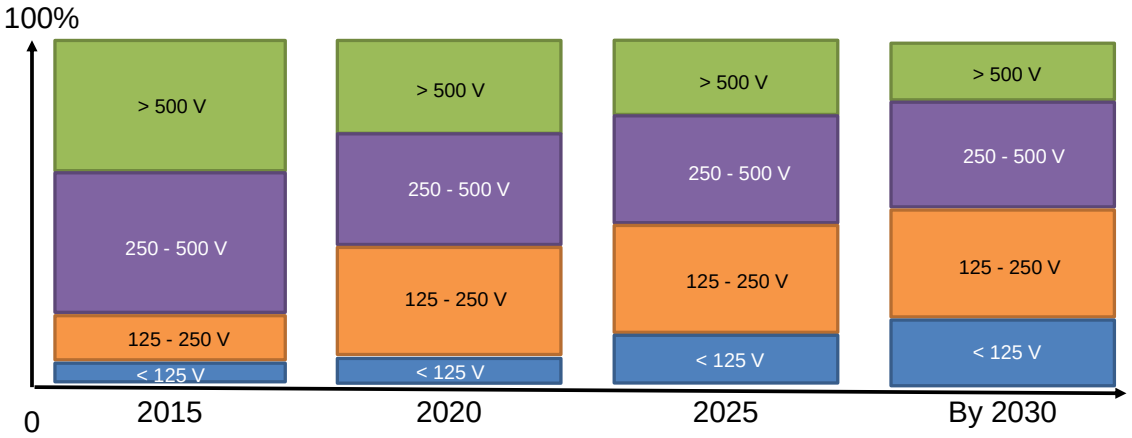

Figure 6: Forward-Looking Charged Device Model Sensitivity Distribution Groups

2.3 Device ESD Thresholds and System Level ESD (IEC 61000-4-2): No Correlation

For several years, there has been a general perception that device-level ESD (for example, HBM) is a predictor or prerequisite for good system-level ESD robustness. This misconception has caused many OEMs to put special increased HBM requirements on devices, thinking it will improve the chances of passing the IEC 61000-4-2 system-level test. This misconception was addressed in Industry Council White Paper 3 Part I [6]. As shown in Figure 7, from that study, it has been demonstrated that the **IEC 61000-4-2 system-level ESD and device-level ESD are not correlated with each other.**

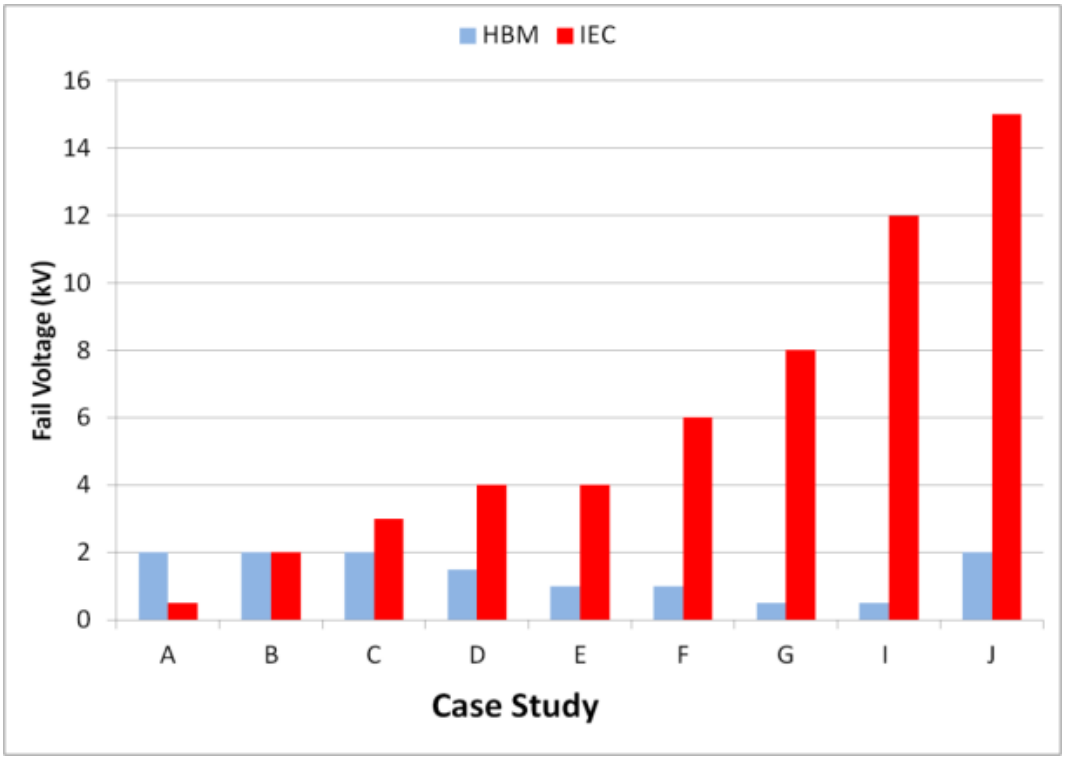

Figure 7: Comparison of IC Device Level and System Level ESD Failure Threshold of Various Systems (A-J) Showing that HBM Protection is not Related to System Level ESD Robustness

At the system level, ESD robustness is a much more complex issue requiring a deeper understanding to address the ESD protection requirements for electronic systems such as laptops, cell phones, printers, home computers, and those in the automotive and industrial segments. These system complexities are due to the protection of external interfaces, such as the universal serial bus (USB), to the outside world. Such systems can lead to hard or soft failures after encountering the more severe ESD pulses, such as those specified by the IEC 61000-4-2 [7] or ISO 10605 [8] test methods.

As introduced in White Paper 3 Part I, a co-design approach is required. A basic version of the so-called system efficient ESD design (SEED) has been proposed, which addresses hard failures related to IC pins with a direct external interface. More advanced co-design approaches are needed for soft (reversible) failures, which are more frequently reported. These are more challenging to understand and overcome and require an extension of the SEED approach to other failure mechanisms, including latch-up and electromagnetic interference (EMI) effects. These challenges and approaches are discussed in Part II of White Paper 3 [9]. The adoption of SEED within the Industry has begun, but adoption has been limited as the industry best determines how to supply the needed data and simulate the events. The trend of adopting SEED, though slower than expected through 2020, is expected to continue to grow as the risk to external IO ports has not changed.

The important point for the present discussion is that none of these system-level failures are improved or reduced by increased HBM or CDM device threshold levels. Thus, the technology scaling effects for both HBM and CDM, as shown in Figures 2 and 6, would not have implications for system-level ESD.

2.4 Process Control

ESD control programs have been in place for many years. One of the earliest programs was implemented to help with the production of gunpowder. This simple program effectively kept the powder wet during manufacturing and handling. This kept the static charge low enough that the gunpowder would not ignite.

In the 1950s and 1960s, electronics were relatively insensitive to ESD events. The devices of the time could withstand most events without a problem. Even if the devices did fail for ESD events, the failures were a very small portion of the overall failure rates.

In the late 1970s, with the introduction of large-scale integration (LSI), ESD became a significant problem. A group of industry experts realized this and organized the first US ESD Symposium in 1978. At the time, technical papers and workshops on problems and solutions were exchanged. Companies also started to implement ESD control programs at this time. Each company had its unique program and did not share the information. The need for standardized programs was not recognized at that time.

The US Military was one of the first organizations to recognize the problems with static electricity and ESD. The first standard to address ESD process control was MIL-STD-1686, released in May 1980. This standard, along with its companion handbook MIL-HDBK-263, represented the first ESD control standard in the industry. All electronics suppliers to the military were required to comply with this standard. However, most of the private sector still followed the company-developed procedures.

These early standards were focused on people and packaging. The controls in place for insulators were left mostly to the end-user without much consideration except for the removal of non-required insulators. Tools, machines, and automated equipment were not addressed or considered, as most processes were manual. The basic instructions were to keep everything and everyone handling the devices at the same potential.

An additional issue with these first ESD control programs was that the materials used to control static electricity did not have standards to qualify the materials. This led to many different types of testing, different methods, and different instrumentation that caused different results. In some cases, materials measured by these methods did not perform well in controlling static. In the early 1980s, a professional association, EOS/ESD Association, Inc. (ESDA), was formed to resolve material testing issues. The first standards from the ESDA were simple material tests for items such as wrist straps, work surfaces, and flooring. The standards created a way to compare one product to another. Suppliers of these materials were able to use the standards to improve products. For example, the simple wrist strap has undergone many industry changes. What started as a simple metal bead band has evolved into a system that makes better contact with a person and, in some cases, allows for continuous monitoring. Wrist straps provide a much more reliable connection than before and last longer. The standards also provide a way to test the wrist straps consistently so that a wrist strap that becomes defective can be removed and replaced. Before this, materials were used until physically damaged without regard to the electrical properties.

In the 1980s and 1990s, the electronics manufacturing industry changed from each company having all manufacturing within the company to a model that included many contract manufacturers (CM) or electronic manufacturing suppliers (EMS). At the same time, the military and the European standard, CECC 00 015:1991, were not evolving with technology and with changes in manufacturing supply chains. The standards were either too restrictive or did not address all aspects of a control program.

In 1995, the ESDA was tasked with replacing Mil-Std-1686 with an industry standard. The standard, ANSI/ESD S20.20-1999, replaced ESD process control. Following the release of this standard, a third-party certification program was established to demonstrate compliance with the standard and has been successfully applied to factory certifications worldwide, as shown in Figure 8. ANSI/ESD S20.20 has been periodically updated to keep pace with device technology, emerging information about ESD failures, and improvements in ESD control technologies and measurement methods, with the latest version being ANSI/ESD S20.20-2021 [2]. In parallel, the IEC has created and periodically updated a similar control document, IEC 61340-5-1 [3], which is equivalent technically to ANSI/ESD S20.20.

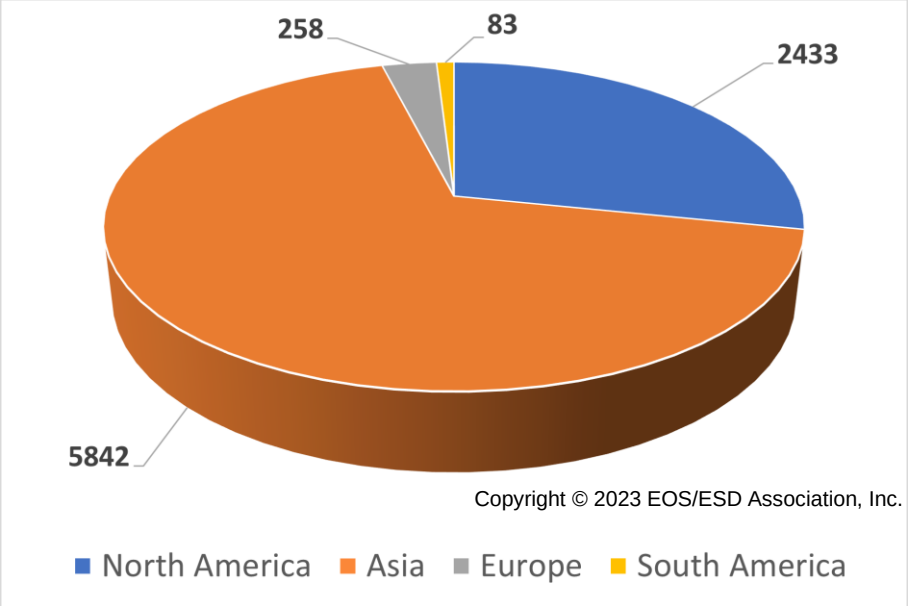

Figure 8: ANSI/ESD S20.20 Certificates Issued Since Inception

2.5 Process Capability Assessment

These ESD sensitivity trends will majorly impact manufacturing process yields over the coming years. Companies must increase efforts to verify that processes can handle these devices and, where necessary, improve ESD control programs. This could include changes in the ESD control item limits, changes in compliance verification frequency, and other ESD monitoring forms, such as ESD event detection.

Recently, the ESD Association released a standard practice on ESD process assessment. ANSI/ESD SP17.1 [10] describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive (ESDS) items are handled. The process assessment in ANSI ESD SP17.1 covers risks by charged personnel, ungrounded conductors, charged ESDS items, and ESDS items in an electrostatic field. The basic approach is to compare parameters measured in the manufacturing process, for example, an electrostatic voltage on an ESDS item, with the limits derived from the HBM or CDM robustness of the ESDS item. The procedures in this document are for use by personnel possessing advanced knowledge and experience with electrostatic measurements. Assessing the results from the measurements described in this document requires significant experience and knowledge of the physics of ESD and the manufacturing process.

2.5.1 Human Body Model (HBM)

It has been shown that a person's resistance to ground is directly correlated to the maximum voltage on a person. Tests on a person wearing a wrist strap using standard shoes on non-ESD flooring have shown that a total resistance to ground through a wrist strap of 40 x 10^6 ohms or less is necessary to limit body voltage to less than 100 volts. Figure 9 shows the relationship between the body voltage of personnel wearing standard shoes on a non-ESD floor connected by a wrist strap to ground as a function of the total resistance to ground through the wrist strap. The limit for wrist straps provided within ANSI/ESD S20.20 is 35 x 10^6 ohms, which is approximately a 10% safety margin.

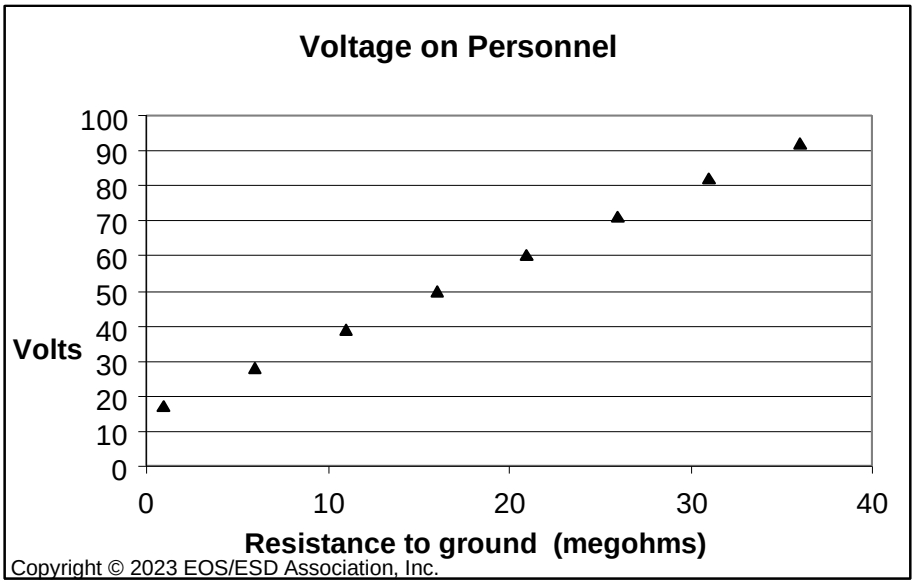

Figure 9: Relationship Between Body Voltage and Resistance to Ground

The situation is more complex for an ESD control program that uses a footwear/flooring system to ground personnel. As people walk across a floor while wearing footwear designed to keep personnel grounded, it is difficult to predict the voltage on a person's body due to the constantly changing body capacitance and the continuous charging and discharging of the person.

ANSI/ESD STM97.2 [11] can be used to determine the process capability of the footwear flooring system. An example of the information provided can be seen in Figure 10.

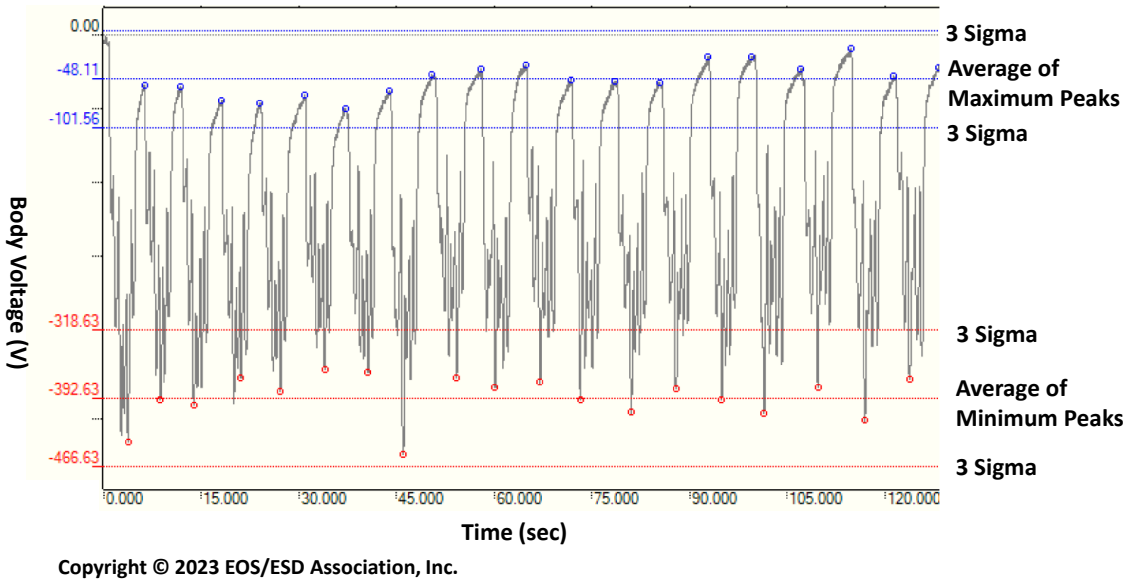

Figure 10: Determining Process Capability of a Footwear/Flooring System using ANSI/ESD STM97.2

2.5.2 Machine Discharge Events

Machine discharges occur when charged conductive surfaces come into contact with ESD sensitive devices. To minimize machine discharges, ensure that all conductive surfaces that come into contact or proximity with ESD sensitive devices are grounded. If it is impossible to ground conductive surfaces, then measurements should be made to ensure that moving parts remain below a threshold voltage throughout the process. In ANSI/ESD S20.20, the threshold is defined at 35 volts.

CAUTION: THIS THRESHOLD LEVEL DOES NOT TRANSLATE INTO ANY MEASURED CHARACTERIZATION WITH AN MM TESTER. THESE MEASUREMENTS MUST BE TAKEN WITH THE PROPER EQUIPMENT, SUCH AS A CONTACT VOLTMETER OR A NON-CONTACT VOLTMETER. MOST FIELD METERS CANNOT MAKE THIS MEASUREMENT.

2.5.3 Events from Charged Devices and Static (Field) Induction (CDM)

In its pure form, a CDM event occurs when a charged ESD sensitive device is grounded or when a neutral device is grounded in the presence of an electrostatic field. A unique characteristic of these events is the involvement of a very fast rise time event between a device pin and another conductor at a different potential. CDM is the most relevant discharge model when single ICs are handled with automated equipment or manually using hand tools. Thus, the CDM test method also indicates the more general cases of conductor-conductor discharges, such as touching a device lead with conductive tweezers. This includes many isolated conductor discharge events mentioned in the previous section.

Effective ESD control programs ensure that the process required insulators will not induce a voltage onto the devices (static induction) being handled or that devices are triboelectrically charged, which could result in a damaging discharge of the device. As CDM thresholds are lowered, it becomes more difficult to depend on voltage control alone to provide adequate device protection. Thus, it is becoming more important to eliminate conductor-conductor contact wherever possible and use dissipative materials to avoid hard grounding.

2.5.4 Charged Board Events (CBE)

ICs and other ESD sensitive devices remain at risk when mounted onto printed circuit boards and other assemblies. Evidence shows that many ESD failures in circuit and system assemblies occur at the board level. These types of failures are due to charged board events (CBE). Most ESD testing and characterization of devices are done on standalone parts. This type of data is summarized in the HBM and CDM roadmaps.

Further, IC failure analysis data, based on knowledge of failure signatures seen in standard HBM and CDM tests, has caused many to conclude that ESD failures are relatively rare compared to other electrical failures commonly classified as electrical overstress (EOS). Recent data and experience reported by several companies and laboratories now suggest that many failures previously classified as EOS may instead result from ESD failures due to CBE (or cable discharge events (CDE) discussed in the next section). A charged board stores more energy than a standalone part because its capacitance is larger. The charge (energy) transferred in the event may be large enough to cause EOS-like failures to the devices on the board.

The previous paragraph implies that some PCBs can have sensitivities outside the scope of ANSI/ESD S20.20. For facilities that find that they are handling parts with sensitivities below those stated in ANSI/ESD S20.20, more controls or tighter limits than those defined may be needed. However, these practices and requirements, in most cases, should be sufficient for protecting circuit boards (PCBs). Problems do arise when specific program implementations do not fully comprehend PCBs as ESD sensitive items. In these cases, the risk of failure due to CBE may be significant. Identifying CBE as the root cause of failure can be difficult. This may require conducting tests that can replicate failures due to CBE and distinguish them from other possible electrical stresses. Methods for conducting CBE tests are currently under development in ESDA WG 25.0 (see Section 3.2.3).

2.5.5 Cable Discharge Events (CDE)

The insulation on a communication cable (USB, Ethernet, etc.) is easily triboelectrically charged by the movement of the cable over surfaces such as desktops, floors, clothing, and work surfaces. This charging will, in turn, induce a potential on the conductors of the cable. When the charged cable is plugged into a system, an ESD event occurs between a cable conductor(s) and one or more of the connector pins of the system receptacle, depending on the connector design. This discharge is referred to as CDE. The resulting current pulse highly depends on the length, impedance, type of connector, and cable quality. Industry reports indicate that CDE can cause an interface device to be damaged, create a system "lock-up," or cause a system upset. CDE is generally considered a charge equalization process between the victim unit or device and a charged cable. Still, a CDE can also occur if the victim unit (laptop, cellphone, etc.) becomes charged by the cable. In the latter case, the victim unit becomes triboelectrically charged via contact with some material or via a charged person. Whether the cable is charged or the victim unit is charged, the result is a discharge involving current flowing into or out of a cable. Like CBE, the root cause of damage to a device from a CDE may be misdiagnosed as coming from some other form of electrical stress. Methods for conducting tests replicating a CDE are under development (see Section 3.2.4).

3.0 TRENDS IN ELECTRICAL STRESS TESTING

Failure of devices due to a wide variety of electrical stresses is a major contributor to yield losses in manufacturing. ESD represents one category of such stresses that can cause large yield loss events and continuous background dropout. The HBM and CDM test methods have been the main enablers in the design of ESD-robust devices and are described in further detail in Section 3.1. These methods are often described as qualification methods because of the key role in the relationship between supplier and user. Stress tests can play other important roles, such as characterization or failure replication; these are discussed in Section 3.2.

3.1 Device-Level ESD Qualification

As described previously, decreasing ESD thresholds will put more pressure on the ESD control program to maintain high yields. To know where special procedures and scrutiny are required, one must know the device's sensitivities. With pin counts increasing and pin spacings decreasing, evaluating devices for ESD thresholds has become more challenging. As a result, the HBM and CDM test methods have continued to change, and additional changes are anticipated to track increasing device complexity. The increasing test costs and time drive changes in these methods as well.

This data is also used in specific ways. ESD control programs, such as ANSI/ESD S20.20, include in the scope minimum withstand threshold values below, suggesting that additional controls may be needed to maintain high yield. Some organizations, such as the US Military and private companies, use the HBM and CDM classification levels in ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 to add further granularity to an ESD control program. HBM and CDM classification levels are used for process assessment, as described in ANSI/ESD SP17.1. Most significantly, device users and suppliers in the electronics industry use the thresholds obtained from HBM and CDM testing as part of the larger set of technical requirements for defining a qualification device. For example, JEDEC JESD47 [12] includes HBM and CDM testing. As a result, these methods are often referred to as qualification test methods. It is also important to note that unlike most other tests required for qualification, ESD testing, and threshold assignment cannot be done on a technology, family, or package basis. Given the important role played by these tests in nearly every new design, considerable effort has been made to provide reproducible, reliable, and efficient methods. Details and trends for these methods are described below.

3.1.1 Human Body Model (HBM)

In 2010, the ESDA and JEDEC HBM test methods were merged into a single document designated ANSI/ESDA/JEDEC JS-001-2010. After this, the joint ESDA/JEDEC working group issued 2011,

2012, 2014, 2017, and 2023 [13] versions. Over the years, many changes have been made to the HBM standard, including some key items below:

- Since its introduction in 2011, Table 2A has been successfully used to reduce device failures due to wear-out from excessive stresses (by hundreds or thousands) that were required by the previous version. Legacy stress combination usage (Table 2B) is still a possible option and can be used in combination with Table 2A. A detailed discussion of these changes is available in the standard or the companion HBM User Guide, ESDA/JEDEC JTR001 [14].
- The focused testing of IO pairs that could be weakly protected can provide an improvement over testing IO pins to all other IO pins tied together. If information is missing, the user can still stress any single IO to all other IOs tied together.
- The concept of a low-impedance above-passivation layer (APL), sometimes also known as a redistribution layer (RDL), was introduced. This allowed representing a supply group or IOs tied together by a single pin, making two-channel testing on high pin count devices feasible.
- The N-channel low-parasitic simulator definition has been improved in the last release. These changes determine when a tester has sufficiently low parasitic to guarantee the same results, stressing two pins in one polarity or reversing both pins' connection and stress polarity.
- Cloned non-supply pins definition and testing methodology have been developed to reduce test time and have the same confidence level.
- Addition of a 50-volt test level in recognition of very low target-level products.
- Introducing an Annex focused on failure windows and the need to understand this in HBM testing.
- The exposed pad has been defined as a pin and shall be stressed according to its classification. The implications of this may require new hardware on the HBM tester to support the testing.
- Full allowance to stress both parts on a package, die, or wafer.

A true statistical sampling scheme standard practice has been developed to reduce the over-stressing of pins relative to real-world environments without compromising the threshold assessment of the product. A similar discussion is ongoing to define statistical testing for supplies connected by APL for test time reduction using a two-channel simulator.

3.1.2 Charged Device Model (CDM)

CDM continues to be recognized in the electronics industry as a valuable ESD model for assessing ESD risk in automated IC handling and manufacturing worldwide. CDM ESD must consider the scaling of the device process – IO pin technology, scaling down of minimum device size – pin pitch achievable in test, and CDM tester metrology limitations in consideration of the CDM roadmap direction over the next five years.

3.1.2.1 Device Thresholds

The continuing trends of integrated circuit process technology advances, increasing package size and complexity, and increasing IO performance requirements all point to lower minimum charged device model withstand thresholds, especially for the high-performance pins. These trends will result in a larger percentage of high-performance pins on products forecasted to be below 125 volts by 2025. These pins may only comprise a small fraction of the total number of pins in any one package.

3.1.2.2 Package Size/Pin Pitch

Two package-related limiting factors to CDM testing are the minimum package size and pin or ball pitch (distance between pins/balls on a package type). Minimum package x-y dimensions in 2020 are on the order of 400 by 600 µm, and this is expected to pose a challenge to small package testing looking out to 2025. A pin pitch of 350 µm (the minimum achievable by CDM testers in 2020) will not allow testing for packages with smaller pin pitch (including bare die pad spacings) for today's pogo-style discharge pin/ground plane style CDM probe assemblies. Thus, future CDM test

capability requires probe technology like automated test equipment (ATE) for those die-form products.

3.1.2.3 CDM Testing Methodology

Two types of CDM testing are in use today. The first type, field induced CDM testing, is used by over 90% of the electronics industry. This is widely based on the harmonized ANSI/ESDA/JEDEC JS-002, published in 2015 and updated in 2022 [15]. This harmonization has helped the industry standardize on a single field induced CDM test platform but is still limited. These limitations include the minimum device size and pin pitch physical limitation of the CDM test equipment (which leads to multiple pin discharges for very small pitches), as well as the environmental variation of the discharge spark, which is dependent on device size, charge voltage, and relative humidity.

The continued reduction in minimum CDM pin thresholds described limits the use of field induced CDM for many devices due to the increased variation in the discharge waveform at low voltage levels. An alternative CDM testing method, low impedance contact CDM (LICCDM), has been shown in early trials to achieve a more accurate discharge pulse, independent of humidity and the varying characteristics of the discharge spark in the field induced CDM event. Research in approximating the impedance of the field-induced discharge spark with a discharge impedance in the contact CDM metrology chain (through the transmission line and relay switching) has shown significant promise to provide repeatable, reproducible discharge waveforms down below 50 volts with no humidity dependence. A standard practice (ANSI/ESD SP5.3.3) was published in 2019, describing this new test method. Testing using this method is expected to yield more accurate CDM testing at lower voltage levels for those devices needing it. This contact approach also eliminates some of the challenges of testing smaller packages/pin pitches by allowing a sharper pogo tip to be used.

A second alternative CDM test method (capacitively coupled TLP (CC-TLP), which also uses a contact approach, has been investigated. The standard practice ANSI/ESD SP5.3.4 was published in 2022, describing this test method. CC-TLP systems have been used much longer than LICCDM and have shown a good correlation with CDM results in many studies. The limitation of being unable to completely match the field induced CDM discharge waveform due to the higher source impedance can be compensated by a shorter pulse width. Thus, CC-TLP is also being considered a possible wafer-level characterization technique that would give important information on protection structures before any packaging and could be used as a solid figure of merit at the wafer level to compare the ESD robustness of various protection structures. This is also a potential solution for the characterization of chiplets that are used to enable more complex package systems.

3.2 Characterization and Replication Methods

Stress tests can play other important roles, such as characterization or failure replication. Characterization using TLP gives ESD protection designers an early indication of the electrical response to ESD-like pulses, informing the ultimate protection strategy. Electrical stress tests can also aid failure analysis and root cause verification and provide comparative evaluations of corrective actions. These can be described as stress *replication* tests. The tests include transient latch-up (TLU), variations of CBE and CDE stresses, and other unintended electrical stresses. These non-qualification methods are discussed in more detail. In the future, some stressing methods may become widespread and reliable enough to evolve into acceptance or compliance tests. Currently, none of the methods are in that category.

3.2.1 Transmission Line Pulse (TLP) Characterization

The TLP method is the de facto standard method for ESD characterization of standalone devices/components and pins of ICs. ANSI/ESD STM5.5.1 [16], fully revised in 2022, is the basis for this work and covers transmission line-based quasi-static characterization with pulse widths in the range of single nanoseconds to several microseconds and appropriate rise times. The User and Application Guide, ESD TR5.5-04-22 [17], provides additional information on the practical use of TLP systems and is extended regularly.

Technical report ESD TR5.5-05-20 [18], released in 2020, addresses using TLP systems for non-quasi-static analysis. The working group has started working on a standard practice, advising on the best-known practices for measurements to support the analysis of the device response to fast transients, such as during CDM or system-level stressing.

With the increased use of automated TLP systems, collecting sufficient data for a statistical analysis becomes feasible. Therefore, the working group started compiling a technical report on using TLP to statistically characterize device behavior under ESD conditions. Examples are methods to characterize the distribution of parameters such as trigger voltage, failure current, and oxide breakdown voltage.

The increased usage of TLP and the use of the results for developing ESD models for the SEED method [6,9] suggests the development of a definition of a (minimum) standard way of characterization and reporting for such applications. This may lead to a new technical report or user and application guide extension.

Finally, the working group may investigate the need to extend the pulse width range and rise time range of the TLP methods.

3.2.2 Transient Latch-Up (TLU) Replication

Integrated circuits can contain latch-up sensitive structures (such as parasitic thyristors), which can cause reliability issues during operation. For this reason, most semiconductor devices must be qualified to a respective latch-up sensitivity. JEDEC JESD78 [19] is the most used latch-up qualification standard. However, this test has a rather slow rise time and long trigger pulse, which does not cover many latch-up events. It is well known that fast transients, such as ESD, can trigger latch-up more efficiently [20].

Per the "static" JEDEC JESD78 latch-up standard, the ESDA WG5.4 "Transient Latch-up "defines transient latch-up as a state in which a low-impedance path resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both, persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is faster than 5 µs.

In 2014, to address industry needs, ESDA WG5.4 started a new standard practice on TLU, which defines a universal TLU methodology that can be used for replicating transient effects seen in the field. The proposed TLU trigger pulses and the setup can be modified to match a specific application's requirements and constraints. The methodology can be applied to various applications, from simple test structures and discrete semiconductor devices to complex integrated circuits as standalone devices or systems. The proposed methodology can reproduce all TLU events discussed in ESD TR5.4-04-13 [20]. An important building block of the document is the verification methodology of the TLU setup, which ensures a correct pulse delivery to the device under test and a sufficiently fast response from the power supply. ESDA WG5.4 released ANSI/ESD SP5.4.1 in 2017 [21], reaffirming the document in 2022.

It must be emphasized that the TLU test methodology proposed in the standard practice is not intended to be used as a qualification methodology, in contrast to the static latch-up test JEDEC JESD78, a mandatory device qualification test. The TLU methodology can be applied to pins, which might be endangered by fast transients in the field, to replicate certain types of electrical overstress.

It intends to establish close cooperation with the JEDEC JESD78 working group, as both standardization committees face similar technical challenges. The relevance of TLU compared to purely "static" latch-up will certainly increase in the future, according to JEDEC JESD78. Therefore, a close link between the JEDEC JESD78 WG and ESDA WG5.4 is planned.

3.2.3 Charged-Board Event (CBE) Replication

The ESDA has published a technical report, ESD TR25.0-01-16, giving general information about CBE phenomena [22]. ESDA published a second technical report, ESD TR25.0-02-23, that guides the industry in replicating CBE threats. It contains examples of how to set up a CBE test bench, carry out testing, and report test results. The document also contains information on estimating

CBE stress levels based on calculated and simulated data. ESD threats due to CBE are case-specific, and the TR does not contain acceptance or target levels for CBE stress. Instead, it instructs how the user can specify the target level and estimate ESD risks based on the observed discharge waveforms in the process area and on the test bench.

3.2.4 Cable Discharge Events (CDE) Replication

ESDA WG14 (System Level ESD) has collected data on real-world CDE events, gathering relevant information from case studies, publications, and industry inputs to create a well-defined test method. This test method is intended to help guide the industry to allow reproducible testing against CDE threats and to help determine the CDE immunity of a system, such as a laptop or handheld device (phones/cameras, etc.). While gathering this data, it became apparent that cable discharge events may only be one of many "events" that may cause operational system failures or hardware failures on individual devices.

Cable discharge events can occur when a charged cable by itself discharges into a system or when a cable attached to another item (which adds additional capacitance) discharges into a system. This discharge can occur between the shell of the cable and the connector on the system or directly between the cable's pins and the pins on the connector on the system. This direct discharge between the cable's pins and the system connector would be a "direct pin discharge". However, this test is not recommended within widely used system level test methods.

The number of variations in discharge events has made it difficult to establish a single representative waveform for a test method. The WG will focus on developing a technical report that will provide information to the industry on the different direct pin injection types, including CDE events. The report will show different levels of events based on cable types for CDE events while offering insight to system designers on possible design and protection recommendations for CDE and other direct pin injection events. The WG has written multiple articles on CDE with an emphasis on educating the industry about CDE but also as a way of gathering information from sources outside of the committee.

3.2.5 Replication of Other Electrical Stresses

The development of defined methods for replicating other electrical stresses is gaining some interest. This arises from the industry-wide initiative to reduce device failures, often characterized as EOS [23]. The main challenge is to find a way to reproduce a wide range of possible stresses systematically. WG 23 collected data and industry practices for producing these stresses based on waveform characteristics and other environmental factors in ESD TR23.0-01-20.

4.0 TECHNOLOGY OUTLOOK

This section focuses on the drivers of the technical advances in the semiconductor industry until 2030. The scaling of CMOS technologies continues, and significant advances in packaging will happen. Another driver will be the broad use of III/V compound semiconductors, particularly in energy conversion and communication. This includes the application of photonic technologies to enable the required huge data bandwidths of the digital society.

4.1 CMOS Technology Scaling – What Comes After FinFET

Soon, the core device architecture will change from FinFET to new device architectures like gate-all-around field-effect transistors (see Figure 11). This technology scaling also requires new materials and interconnect schemes such as backside power delivery networks. These changes will impact both ESD and latch-up protection design. Previously unknown technical limitations in ESD and latch-up protection design could be reached. Implementing ESD and latch-up protection designs at the product level will be more challenging. Because of the complexity of these highly scaled technology platforms, developing and using 3rd-party IP is essential to enable ESD and latch-up robust products in these very advanced technology nodes cost-efficiently.

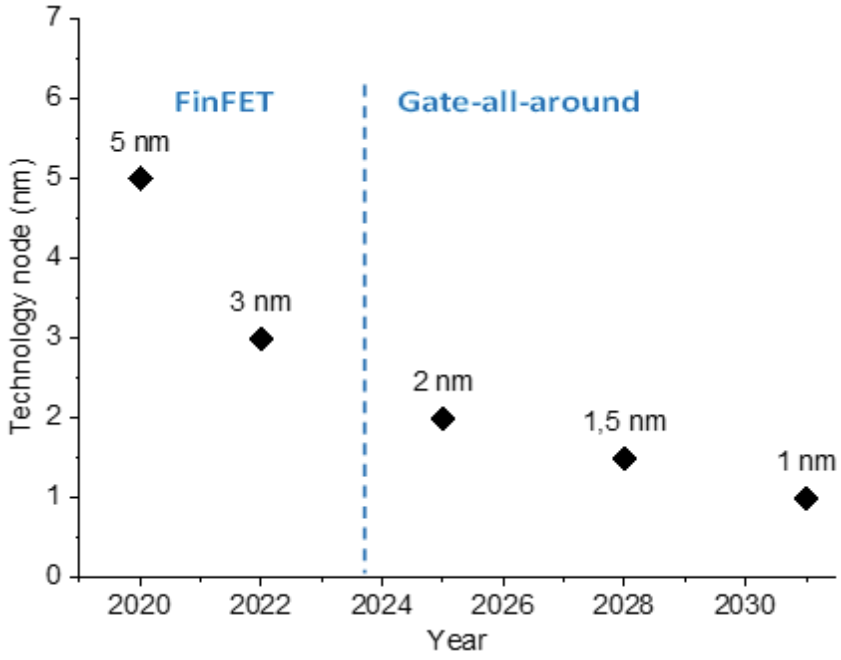

Figure 11: Roadmap for Logic Device Scaling Until 2031
NOTE: Source is IRDS Roadmap 2022 [24]

4.2 Sub-10 nm Technologies for Automotive Applications

It is predicted that the value of ICs in the car will increase by 2026 by 55% compared to 2020 [25]. The value of ICs increases even more in electrified vehicles. This growth in semiconductor content in vehicles is caused by four major trends: electrification, autonomous driving, connectivity, and shared mobility. Besides efficient power conversion, next-generation cars will need much more computational power, enabled by highly scaled CMOS technologies.

The semiconductor industry has long-term experience using highly scaled technologies like FinFET for consumer electronic applications and products. A strong ecosystem of semiconductor foundries, IP block providers, and IC manufacturers has been established and supports the use and further scaling of these technologies. In the automotive industry, autonomous driving and connectivity, particularly, can only be enabled by using these advanced technologies. Advanced driver-assistance systems (ADAS), microcontrollers, and microprocessors are typical applications. The high-reliability requirements of automotive applications conflict with some of the physical limitations of highly scaled technologies. This also opens new challenges for ESD and latch-up protection design because consumer-grade protection solutions must be adapted to the higher requirements of automotive applications. This can lead to some designs not meeting the higher automotive reliability requirements. Therefore, the ESD target level in the Automotive Electronics Council (AEC) Q100 specification is being re-evaluated, and a reduction of the ESD target level in AEC Q100 is being discussed. The same counts for latch-up design and testing, where much lower supply voltages and currents and high-temperature profiles bring additional challenges.

4.3 Heterogenous Integration and Advanced Packaging

Heterogeneous integration is the process of disaggregating the functionality of a system onto separate dies that may come from different technology nodes and even materials and then connecting these in a single package. The individual dies in such systems are also known as chiplets. Both lateral connectivity (2.5D IC stack) and vertical connectivity (3D IC stack) are used (see Figure 12).

Advanced packaging refers to the technologies that enable heterogeneous integration and are a combination of technologies to enable cost, performance, power, and sized optimized interconnection of ICs. It also includes supporting elements to each other and the system, including flip chip, wafer, panel level packaging, and interposer with and without through silicon vias (TSV) [26]. TSV establishes the electrical connection from the bottom to the front side of a die.

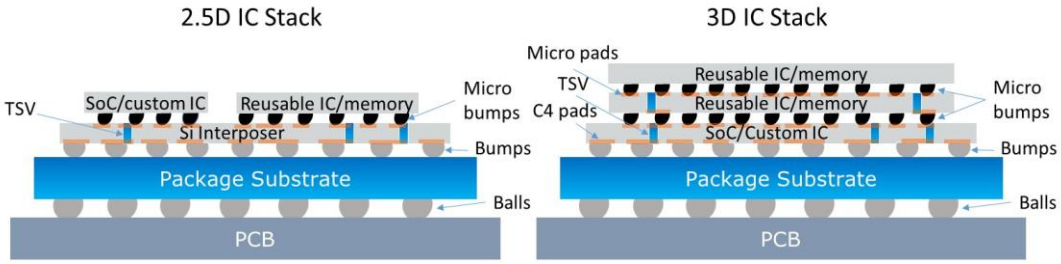

Figure 12: 2.5D Stack (left) and 3D Stack (right) ICs

What are the ESD challenges associated with advanced packaging? The density of micro bumps is expected to increase significantly in the coming years. This is enabled by reducing the bump pitch from more than 25 µm to less than 10 µm. Because of the higher die-to-die interface density, the minimum CDM target level for those interfaces must be reduced (see Figure 13).

The typical area allocated to ESD protection of signals exposed to a package terminal is unacceptable for such dense signal interconnects [28]. Nor is it necessary to manufacture such systems reliably. CDM target levels for die-to-die interfaces described in the literature are below 100 volts [28], for which ANSI/ESD S20.20 adequately describes ESD controls. Below the CDM sensitivity level of 100 volts, ESD is not controlled. Each case must be carefully analyzed to determine the ESD risk and mitigations necessary to ensure manufacturability. Developing ESD control standards below 100 volts is a critical need for the industry to improve this situation.

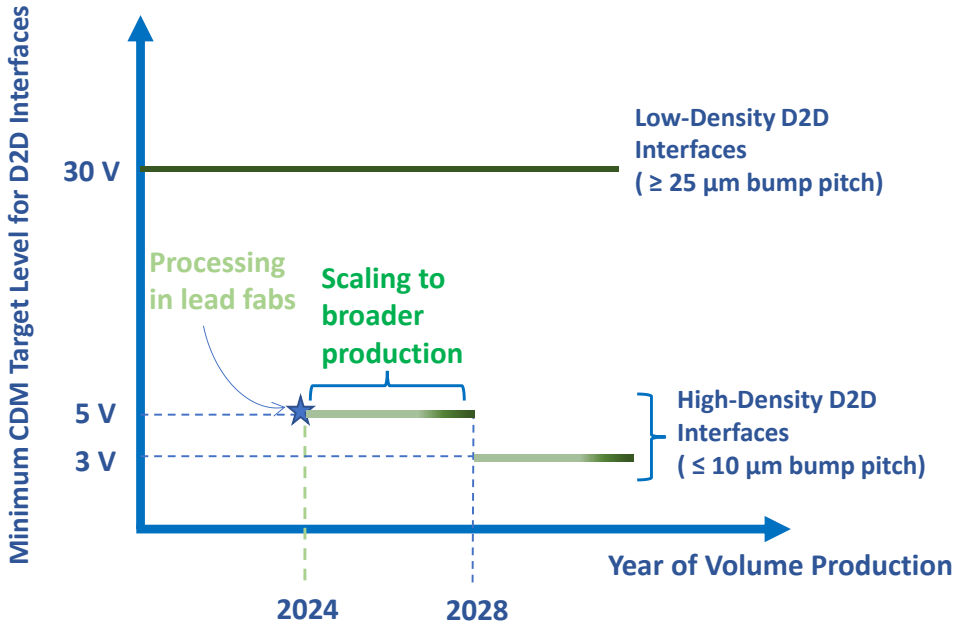

Figure 13: Roadmap of CDM Targets of Die-to-Die Interfaces [27]

4.4 Gallium Nitride for Power and RF Applications

The acceleration of gallium nitride (GaN) technology over the last 2 decades continues to exceed predictions. The applications driving this technology are wireless communication and power conversion. These are also key to energy conversion in electric vehicles. As these GaN technologies mature, the importance of ESD solutions to enable large-scale manufacturing will increase. State-of-the-art GaN technology is built on Si substrates, taking advantage of the mature manufacturing infrastructure in silicon fabs. These state-of-the-art technologies will also allow the design and manufacturing of GaN IC where commonly used ESD target levels must be met. This will also require designing and developing ESD protection circuits for GaN IC.

Different challenges lie in the use of discrete GaN components. In an industry survey in 2021 [29], ten different GaN semiconductor suppliers provided the ESD ratings for selected components, including RF and power transistors. The ESD ratings included several parts with very sensitive ESD ratings of Class 1a (250 volts < 500 volts HBM) and some with high ESD ratings (> 2 kilovolts HBM). This highlights the challenges in meeting safe manufacturing levels for discrete GaN transistors. The GaN devices can withstand high voltage but have little avalanche current robustness. Discrete (non-integrated) GaN FETs have weak, exposed gates and no ESD capability, causing erratic system behavior and device failures. Monolithic integration of GaN drivers [30] and the multi-chip module integration of silicon drivers with GaN FETs [31] in a single package have the opportunity for much higher final product ESD robustness.

4.5 Photonics

Silicon photonics technologies (SPT) are often used for transferring signals between two chips where high bandwidth signal transfer is needed. Two key components are the modulator, which turns the electrical signal into an optical signal, and the photodetector, which converts the optical signal back into an electrical signal, as shown in Figure 14 [32].

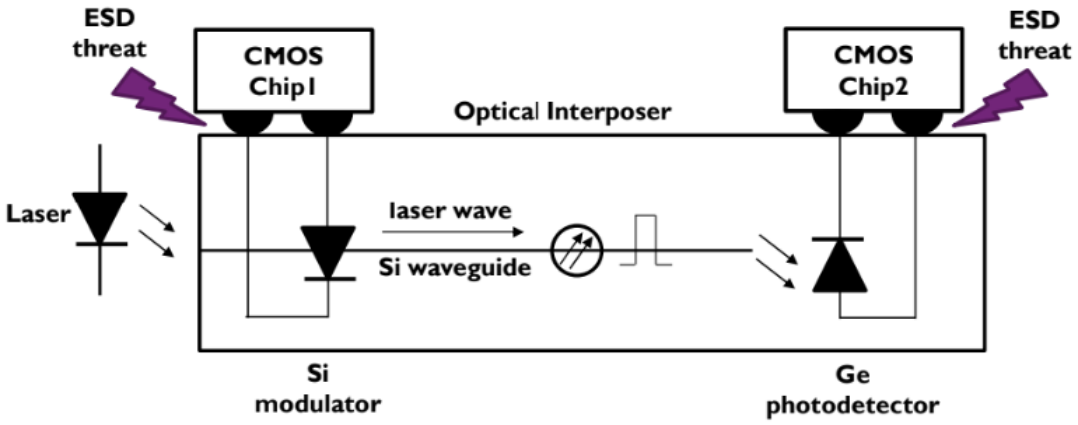

Figure 14: Schematic of Optical Interposer Functionality Containing Si Modulator, Si Waveguide, and Ge Photodetector with ESD Threat at Bond Pads

Typically, these components are integrated into silicon-on-insulator (SOI) technologies. The modulator and photodetector are exposed to ESD during assembly when the photonics chip is connected to a CMOS chip. In an ideal environment with ANSI/ESD S20.20 controls, HBM events are controlled to 100 volts or below.

5.0 COMPUTATIONAL METHODS OUTLOOK

This section focuses on some of the drivers for ESD computational methods. First, there are EDA tools for design verification. Another driver is new machine learning methods. Finally, there is SPICE modeling for ESD design. To give a general overview as a starting point, the history and roadmap of all these different drivers for ESD computational methods are shown in Figure 15.

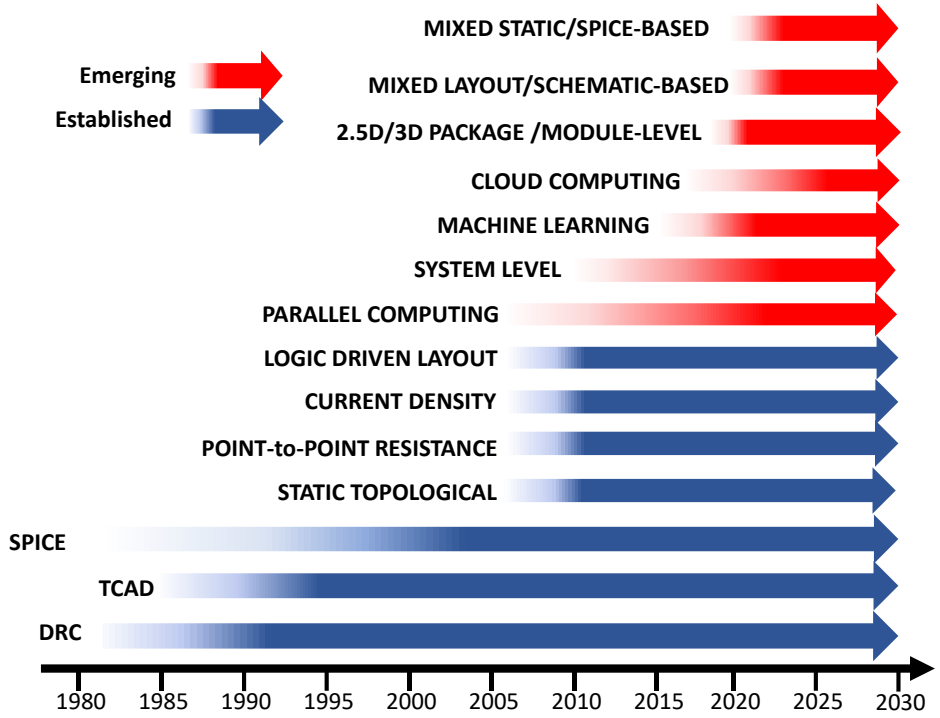

Figure 15: History and Roadmap Electronic Design Automation (EDA) Tools

5.1 Electronic Design Automation (EDA) Tools

Verifying the ESD protection design of a complex IC design with many supply domains and voltage levels, various functional parts (RF, digital, analog), mixed-voltage circuitry, and advanced packaging will remain a challenge and a driver for the development of new EDA tool capabilities [33].

Few EDA tool areas are expected to experience significant development in the next five years. One of these areas is ESD EDA verification based on layout-extracted netlists. Layout-based netlists bring computational challenges since these netlists are significantly larger than the ones based on schematics views and are often only available late in the design cycle. The EDA industry approaches these challenges by introducing parallel, cloud computing, and hardware acceleration (xPU) to execute these checks. Sometimes, breaking the separation between layout-based and schematic-based verification may be necessary. Layout-based information such as parasitic ESD routing resistances and inductances can be extracted from partial layout and introduced inside schematic netlists for a more accurate evaluation of ESD voltage drops in a pure topological environment (arrow named "MIXED LAYOUT/SCHEMATIC-BASED" in Figure 15). These implementations will help to get an effective ESD verification process by using verification as much as possible during the design phase.

2.5D/3D packaging and module-level ESD verification have rapidly become another concern. Conventional ESD EDA tools are IC-focused, and each die technology tool needs a complex set-up. A common format or syntax to set up verification tools must be encouraged to improve the ease of use when dealing with complex IC die, packages, and modules involving multiple technologies

and EDA tools. EDA tools design packages, die and interposer, and modules. An ESD specification format must be further developed to establish seamless communication and set-up of the various ESD EDA verification tools using common netlists and pin/pad definitions.

The boundaries between static and dynamic ESD verifications are disappearing. Existing ESD current density and point-to-point resistance analyses rely on simulation techniques. Full-chip static topological check analyses can be used to create relevant SPICE netlists for complex ESD protection scenarios such as power domain signal crossings. Simple SPICE simulations can be integrated into topological EDA checks to assess better the severity of reported violations (arrow named "MIXED STATIC/SPICE-BASED" in Figure 15). Another development area is to minimize any manual inclusion of initialization information necessary to enable the verification runs, for example, pad functionality definition, ESD stress requirement per pad and pins absolute maximum ratings (AMRs). Moreover, ESD EDA verification flows become more complex, containing sets of heterogeneous rules grouped in different tools (commercial and in-house) and applied to objects like IC schematic, IC layout, package view, etc. There is a rising need to align the ESD verification environments to reach homogeneity and considerably improve usability.

5.2 Machine Learning for ESD Data Analysis

The design and analysis of ESD protections for IC reliability are often done with well-established methods. Various ESD pulses are applied to IC devices for testing. However, the analysis of test results is time-consuming. Although some semi-automated test methods have been developed during the last decade, ESD reliability evaluations still involve highly skilled and senior experts to assess the true impact of the results. Therefore, machine learning applications could be desirable to bring more efficiency to ESD data analysis. The motivation is to develop machine learning approaches that can be implemented during ESD testing, data analysis, and the qualification process.

These new paradigm-shifting approaches would appeal to the IC industry in dealing with the cumbersome ESD evaluation and in reducing uncertainties of the results. As observed in other fields, the first challenge could be creating an open ESD test results dataset to let academics develop and optimize their models.

Machine learning is expected to take place in two different aspects. The first one is diagnosing any failures at the first indication of symptoms and avoiding duplicate tests to uncover the same issues. The urgent need comes here on how to interpret the data. As a next step of this analysis, the efficiency can be realized by applying machine learning to functional parameter shifts. The benefit from this type of practice would have tremendous potential and appeal.

Another application of machine learning would be in IC ESD protection design implementations. This would require establishing certain rules known as "ground truths." The patterns are noted after observing a vast amount of data from ESD testing methods. The learning process will rely on identifying these symptoms with the next ESD data analysis. Once machine learning can identify the root causes with the defined ground truths, it can speed up the data evaluation process. In this manner, the engineer recognizes patterns faster and avoids repeating tests for the same symptoms since the root causes are already addressed.

5.3 SPICE Modeling for ESD Design and Verification

SPICE-based circuit-level simulation is one of the foundations of modern IC design. Efforts to apply SPICE simulation to ESD design and verification have existed for decades. The earliest literature reports appeared in the 1980s when device engineers began creating protection structures to address the emerging ESD problems in the electronics industry. However, up to today, trial-and-error or cookbook approaches based on prior art still dominate ESD protection design. Commercial EDA tools developed in recent years for ESD design verification have mostly focused on design rule check (DRC) and static analysis. Device compact models are the backbone of SPICE simulations. The lack of accurate and easy-to-use ESD-capable compact device models has prevented ESD simulations from wide acceptance.

As ESD protection becomes more challenging in advanced technologies, it becomes a more urgent need to have SPICE simulation in ESD protection design and verification, just like in the regular IC design. ESD-capable compact models constitute the backbone of SPICE ESD simulation. These must be able to reproduce device behavior under high current and high voltage conditions beyond the normal operating region. Snapback in silicon-controlled rectifiers (SCR), bipolar transistors (BJT), and MOS devices is the most important effect of SPICE ESD simulation. No industry standard models can reproduce the snapback phenomenon in SPICE simulations. Therefore, developing customized device models to include the snapback effect has been the focus and one of the most challenging tasks in ESD compact modeling. The snapback ESD models have been implemented in various ways: proprietary C code, behavioral language Verilog-A, macro-models comprised of standard component models, and Verilog-A modules attached to standard devices. Though no snapback is involved, diodes have special physical effects that are important to ESD events but are not included in standard SPICE models. Modeling the voltage overshoot and current saturation in diodes has been another focus in developing the ESD compact model. Compact models predicting thermal ESD failure or dielectric breakdown have also been reported.

The semiconductor industry has increasingly recognized the importance of device compact modeling for SPICE ESD simulation [34,35]. After several years of working, The Silicon Integration Initiative (Si2) Compact Model Coalition (CMC) released the ASM-ESD diode model in February 2023. This diode model is the first industry-standard model to capture device behavior under ESD event conditions. CMC has started the development of an ESD MOSFET model as the second standard ESD modeling project. The project is currently in the definition stage, and the model will be completed in three years. It is expected that there will be multiple standard ESD compact models available by 2030. Those new standard models should not only include fundamental ESD parameters such as turn-on voltage Vt1, holding voltage Vh, and on-resistance Ron but also critical secondary effects like voltage overshoot, pulse rise-time dependence of Vt1, conductivity modulation, self-heating, forward and reverse recovery in diodes, etc.

Industry-standard ESD compact models are intended to be comprehensive. ESD verification with SPICE simulation is a dynamic verification method. As mentioned in Section 5.1, dynamic SPICE simulations can be integrated into topology-based static EDA checks. Accordingly, simplified SPICE models may be developed for such applications.

6.0 REFERENCES

[1] Industry Council on ESD Targets, White Paper 1: "A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," June 2018, http://www.esda.org/white-papers.

[2] ANSI/ESD S20.20, "Development of an Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment", January 2021 http://www.esda.org/standards/esda-documents.

[3] IEC 61340-5-1 "Electrostatics - Part 5-1: Protection of Electronic Devices from Electrostatic Phenomena - General Requirements", August 2007.

[4] JEDEC JESD 625B "Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices", January 2012 http://www.jedec.org.

[5] Industry Council on ESD Targets, White Paper 2: "A Case for Lowering Component Level CDM ESD Specifications and Requirements," April 2010 Revision 2.0, http://www.esda.org/white-papers.

[6] Industry Council on ESD Targets, White Paper 3: System Level ESD, Part I: "Common Misconceptions and Recommended Basic Approaches", December 2010 http://www.esda.org/white-papers.

[7] IEC 61000-4-2 "Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test", 2008

[8] ISO 10605 – "Road vehicles – Test Methods for Electrical Disturbances from Electrostatic Discharge", 2008, http://www.iso.org/iso/iso_catalogue.htm.

[9] Industry Council on ESD Targets, White Paper 3: System Level ESD, Part II: "Implementation of Effective ESD Robust Designs", March 2019 http://www.esda.org/white-papers.

[10] ANSI/ESD SP17.1, "For the Protection of Electrostatic Discharge Susceptible Items – Process Assessment Techniques", December 2020 http://www.esda.org/standards/esda-documents.

[11] ANSI/ESD STM97.2, "Floor Materials and Footwear – Voltage Measurement in Combination with a Person", November 2016 http://www.esda.org/standards/esda-documents.

[12] JEDEC JESD47 "Stress-Test-Driven Qualification of Integrated Circuits", October 2016 http://www.jedec.org.

[13] ANSI/ESDA/JEDEC JS-001, "Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Device Level", May 2023 http://www.esda.org/standards/esda-documents.

[14] ESD JTR001-01-12, "User guide of ANSI/ESDA/JEDEC JS-001 Human Body Model Testing of Integrated Circuits", 2012 http://www.esda.org/standards/esda-documents.

[15] ANSI/ESDA/JEDEC JS-002, "Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level", 2022 http://www.esda.org/standards/esda-documents.

[16] ANSI/ESD STM5.5.1, "Electrostatic Discharge Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level", July 2022. http://www.esda.org/standards/esda-documents.

[17] ESD TR5.5-04-22, "For Electrostatic Discharge Sensitivity Testing - Transmission Line Pulse (TLP) - User and Application Guide", 2022. http://www.esda.org/standards/esda-documents.

[18] ESD TR5.5-05-20, "For Electrostatic Discharge Sensitivity Testing - Transmission Line Pulse (TLP) - Transient Response Evaluation", 2020 http://www.esda.org/standards/esda-documents.

[19] JEDEC JESD78E, "IC Latch-Up Test", April 2016 http://www.jedec.org.

[20] ESD TR5.4-04-13, "Transient Latch-up Testing", 2013 http://www.esda.org/standards/esda-documents.

[21] ANSI/ESD SP5.4.1, "For Latch-up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits – Transient Latch-up Testing Device Level", February 2018 http://www.esda.org/standards/esda-documents.

[22] ESD TR25.0-01-16, "For Electrostatic Discharge Sensitivity Testing - Charged Board Event (CBE)", 2016 http://www.esda.org/standards/esda-documents.

[23] Industry Council on ESD Targets, White Paper 4: Understanding Electrical Overstress - EOS", August 2016 http://www.esda.org/white-papers.

[24] International Roadmap for Devices and Systems 2022 Edition, 2022, IEEE

[25] Automotive Semiconductor Trends 2021, Yole Development

[26] Heterogeneous Integration Roadmap: https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html.

[27] White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements Part II: Die-to-Die Interfaces, 2023

[28] Dina Medhat et al., "A Programmable Checker for Automated 2.5-D/3-D IC ESD Verification", 2021 IEEE Transactions on Components, Packaging and Manufacturing Technology.

[29] https://nepp.nasa.gov/docs/tasks/EEE-Parts-Bulletin/EEE-Parts-Bltn-2021-Vol-13-No1-ESD-Testing-Standards-GaN-Devices-CL22-0048.pdf

[30] Advancing GaN Power ICs: Efficiency, Reliability & Autonomy (navitassemi.com) https://navitassemi.com/download/nv6158/?wpdmdl=44592&ind=1650533643392

[31] Gallium nitride (GaN) ICs | TI.com

[32] Shih-Hung Chen et al., "HBM and CDM ESD Performance of Advanced Silicon Photonic Components", 2021 43rd Annual EOS/ESD Symposium (EOS/ESD), vol.43, pp.1-7, 2021.

[33] ESD TR18.0-01-14, "For ESD Electronic Design Automation Checks," EOS/ESD Association, Inc., http://www.esda.org/standards/esda-documents.

[34] Y. Zhou, J.J. Hajjar, S. Parthasarathy, "Circuit Level ESD Simulation with SPICE: Successes and Challenges", IEEE 14th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018

[35] E. Rosenbaum et al., "Compact Models for Simulation of On-Chip ESD Protection Networks", an invited paper accepted by IEEE Trans. ED, 2023