TABLE OF CONTENTS

1.0 INTRODUCTION 1

2.0 BUILDING MODELS 3

2.1 FAILURE FLAGS 3
2.2 HARDWARE DESCRIPTION LANGUAGES 4
2.2.1 Introduction to HDL 4
2.2.2 Implementation into VHDL-AMS 4

3.0 VERILOG-A 10

3.1 DIODE CLAMP MODEL 10
3.2 CLAMP MODEL WITH SNAPBACK 12
3.3 CLAMP MODEL WITH SNAPBACK AND ADDITIONAL KINK 14
3.4 CLAMP MODEL WITH SNAPBACK AND CURRENT HYSTERESIS 15
3.5 DYNAMIC VOLTAGE OVERSHOOT DURING TRIGGERING 17
3.6 BENEFITS AND LIMITATIONS 17
3.7 MODELING SNAPBACK BASED ON CONTINUOUS INTERNAL STATE VARIABLE 17

4.0 SPICE-LIKE CIRCUIT MODELS 19

4.1 DIODE COMPACT MODEL 19
4.1.1 Ideal Diode Model Details 19
4.1.2 Ideal Diode Model Example 20
4.1.3 Benefits and Limitations 20
4.2 PSPICE TABLE 20
4.2.1 Detailed PSPICE Table Methodology 21
4.2.2 Snapback Example 22
4.2.3 Benefits and Limitations 22
4.3 SPICE MODEL WITH SWITCHES AND CONTROLLED SOURCES 22
4.3.1 Detailed VCS\DCV\CCVS Methodology Shown in an Example 23
4.3.2 Benefits and Limitations 23
4.4 CURRENT-SWITCHED RESISTOR NETWORKS 23
4.4.1 Unit Cell Construction and Assembly 23
4.4.2 Diode Example 27
4.4.3 Snapback Example 28
4.4.4 Benefits and Limitations 30
4.5 SPICE SCR MODEL 31
4.5.1 Detailed PSPICE SCR Model Methodology 31
4.5.2 Curve Matching Snapback Examples 32
4.5.3 Benefits and Limitations 33
4.6 SWITCH-BASED BEHAVIORAL MODEL IN SPICE 33
4.7 SNAPBACK MODEL WITH DIFFUSION LINE 36

5.0 APPLICATION OF DATA EXCHANGE TEMPLATE 38

5.1 VERILOG-A 38
5.2 SWITCH-BASED MODELS 41
5.3 BIPOLAR MODEL USING DIFFUSION LINE 43

6.0 MITIGATING CONVERGENCE CHALLENGES 45

6.1 GENERIC METHODS TO AVOID CONVERGENCE PROBLEMS 45
6.2 SPICE SIMULATION OPTIONS TO AVOID CONVERGENCE CHALLENGES 46

7.0 SUMMARY 47

8.0 OUTLOOK 47

9.0 REFERENCES 48

Annexes

Annex A (Informative): Codes 50
Annex B (Informative): Revision History for ESD TR26.0-02 59

Tables

Table 1: Implementations of Piecewise Linear I-V Models 2
Table 2: Comparison of Models 3
Table 3: Parameters of the Ideal Diode SPICE Model 19

Figures

Figure 1: Piecewise Linear Description of an I-V TLP Measurement 1
Figure 2: Piecewise Linear Diode Implementation into VHDL 5
Figure 3: Piecewise Linear Snapback Device Implementation into VHDL from TLP Measurement to State Machine Diagram 6
Figure 4: Flow Chart-Organigram for the Piecewise Linear Snapback Device 6
Figure 5: Application Where the Described State Machine Model Similar to Figure 4 has been Used; Comparison of Transient Measurement and Simulation Results 7
Figure 6: TLP Characteristic of the Protection Device and Simulation Results from the State Model 8
Figure 7: Simulation Schematic 9
Figure 8: Simulation Results With and Without the On-Chip Decoupling Capacitance – 10-kilovolt TLP Injection, 1 ns Rise-Time 9
Figure 9: Diode Clamp Symbol 10
Figure 10: Piecewise Linear I-V Curve 11
Figure 11: DC Sweep of Diode Clamp 11
Figure 12: Snapback Clamp Symbol 12
Figure 13: Piecewise Linear I-V Curve of Snapback Clamp 12
Figure 14: Modeling of the TLP Measured I-V Curve of an Internal Protection of a TI SN65LVPE502CP USB3 RX I/O 13
Figure 15: Zoom of Figure 13 for Small Currents 13
Figure 16: Piecewise Linear I-V Curve of Snapback Clamp with Additional Inflection Point 14
Figure 17: Modeling of the TLP Measured I-V Curve of an Internal Protection of a TI SN65LVPE502CP USB3 RX I/O With an Extra Kink at About 1.5 Amperes 15

Figure 18: Additional Overshoot at the End of a Simulated TLP Pulse Due to Missing Current . 15
Figure 19: Piecewise Linear I-V Curve of Snapback Clamp with Hysteresis in Current 16
Figure 20: Simulation of Voltage Versus Time 16
Figure 21: 100-ns TLP I-V Curve Measured for Nexperia "device 3" and Modeled Based on Wang's Approach, TLP Current on Linear/Logarithmic Scale 18
Figure 22: Parameter Set to Model Nexperia "device 3" Within Wang's Model Framework 18
Figure 23: Zener Diode Measurement and Models 20
Figure 24: Schematic Showing the TABLE Function in PSPICE 21
Figure 25: Sub-Circuit and TABLE Point Modification 21
Figure 26: Snapback Device - Measurements and Simulation Results 22
Figure 27: VCS DCV & CCVS Based Snapback Model Suitable for Stress With a TLP Stress Model 22
Figure 28: Ideal Diode Circuit and I-V Curve 24
Figure 29: Negative Ideal Diode Circuit and I-V Curve 25
Figure 30: Positive Resistance Cell and Negative Resistance Cell 26
Figure 31: Positive Resistance Cell and Individual Currents 27
Figure 32: 2-Piece Diode Circuit and Curve 28
Figure 33: 3-Segment Snapback Circuit 29
Figure 34: 3-Piece Snapback Curve 29
Figure 35: Regions of Stability 30
Figure 36: PNP NPN (SCR) TLP Model 31
Figure 37: Sub-Circuit Text File – Enhanced 32
Figure 38: Bi-Polar Snapback Model 33
Figure 39: Core of the Switch-Based Behavioral Model in SPICE 34
Figure 40: Extending the Model Core with Additional Switches to Reproduce Kinks in the I-V Curve 34
Figure 41: Modeling Changes in the Dynamic Resistance 35
Figure 42: Failure Detection Inside the Model 35
Figure 43: Simplified Schematic of the Switch-Based Model 36
Figure 44: Schematical Picture of Model Which is Subjected to a TLP Pulse; Reverse Diode and Snapback Representation; Modeling of the Floating Base as a Diffusion Line ... 37
Figure 45: Simulation Results for a Snapback Device 37
Figure 46: Parameters of a Snapback Device Stored in the Data Exchange Format 38
Figure 47: Schematic I-V Curve and Corresponding State Diagram 39
Figure 48: Parameters Used for Describing the Snapback Device and Verilog-A Code Which Describes the State Diagram 40
Figure 49: Transient Voltage Curve and Transient Voltage Curve if a 30 pF Capacitance is Added in Parallel to the DUT Model 41
Figure 50: Circuit That Describes the Snapback Device Using the Approach Described in Section 4.6 41
Figure 51: Resulting TLP Curves of the Circuit Shown in Figure 50 42
Figure 52: Transient Current and Voltage Curves 43
Figure 53: TLP Curve Given by the Data Exchange Template; Fail Current Versus Time 44
Figure 54: Comparison of a Model with Data Given by the Data Exchange Format; Transient Simulation Results at 7A; Magnification on the Overshoot Peak 44
Figure 55: Implementation of the Failure Mechanism 45