The 6th International ESD Workshop (IEW) will be held at the Priory Corsendonk, Oud-Turnhout, Belgium. Located among century-old forests, the historic Priory Corsendonk provides the perfect background for engaging discussions about the latest issues confronting the ESD community.

This workshop provides a unique environment for envisioning, developing, and sharing ESD design and test technology for present and future semiconductor applications. Hence, this year’s technical focus is evolution, organized in three themes: More Moore, More than Moore, and Evolution in Standardization and Characterization (Moore’s law describes a long-term trend in the history of computing hardware: the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years). Linked to each subtheme expect high quality invited seminars, invited talks, discussion groups (DGs) and special interest groups (SIGs) covering ESD on advancing CMOS beyond the silicon roadmap, the relation between EMC and ESD, EOS, and System Level ESD.

The technical program includes advances in system level and high voltage ESD, as well as studies of component protection ESD testing, case studies, and design of ESD protections. An expanded poster format provides an opportunity for deep technical discussions and networking. As an added highlight, Wednesday afternoon is left free for exploration of the local area, extended technical discussions, sports, or relaxation. This exciting and well balanced program was put together specifically to address the needs and interests of those working in the field of ESD and for the benefit of their companies. Both attendees and their organizations gain from this investment in learning.
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Experience the IEW!

A key ingredient of the International ESD Workshop (IEW) is its informal environment, which fosters extensive interactions among the attendees. In the age-old Priory of Corsendonk, which has provided shelter for travelers throughout the centuries, the participants will appreciate the relaxed atmosphere allowing newcomers and seasoned professionals alike to engage in spirited discussions; which may well extend deep into the night.

The IEW provides a unique opportunity to learn first-hand from world-leading experts in carefully selected seminars and invited talks, to engage in lively debates in one of the discussion groups, or to discuss the technical posters with their authors and interested colleagues.

Each of the poster sessions is preceded by a brief introduction by the authors in a plenary session to aid the participants in selecting the posters they want to know more about. In addition to the peer-reviewed poster sessions, there will be a free-format open poster session. You may want to use this opportunity to present your latest developments or try out new ideas on experienced colleagues.

The discussion groups (DGs) on Tuesday and Wednesday evening are a central part of our interactive workshop. Each discussion will be facilitated by an expert on the subject, but the actual discussion will take place between the DG participants. The IEW also provides space for special interest groups (SIGs), which provide a forum on selected subjects that extends beyond the IEW time frame. Some of these groups have been successfully cooperating for several years.

This year’s technical focus is evolution, organized in three themes: More Moore, More than Moore, and Evolution in Standardization and Characterization. Expect seminars, invited talks, and discussion groups on advancing CMOS beyond the silicon roadmap, ESD in SOI technologies, and the relation between EMC and ESD. A new topic this year is EOS, which is rapidly gaining attention in addition to CDM and System Level ESD. Furthermore, there will be technical papers on ESD testing, case studies, and design of ESD protections.

Outside the sessions, there is ample time for one-on-one exchanges in the inter-session breaks and during the family-style meals in the former refectory of the friars of St. Augustine. Wednesday afternoon is reserved for recreation with fellow attendees; a great way to become better acquainted with your ESD colleagues.

Come and listen to experts, share your views, ask questions, extend your network with ESD experts from industry, and academia, and above all learn how to deal with today’s ESD challenges and prepare for tomorrow’s in an informal and interactive atmosphere.

Keep in mind that space at Corsendonk is limited, so register early. Enjoy the 2012 IEW!
Keynote Talk
Game Changing Technologies in Health Care
Jo De Boeck, imec

Summary:
Personalized, preventive, predictive, and participatory (PPPP) health care is on the horizon. Many nano-electronic research groups have entered the quest for more efficient health care in their mission statement. Ambulatory monitoring of so-called ‘markers’ for wellness and health is one of such proposed solutions. The prospect of personal diagnostics and therapy assisting solutions in e.g., the cardiac, neurological, and oncology fields could indeed stir a – desperately needed – revolution. The talk will address some of the exciting trends in ‘PPPP’ health care and relate them to innovation in process technology, electronic circuits, and system concepts.

Presenter Biography:
Jo De Boeck received his engineering degree in 1986 and his PhD degree in 1991 from the University of Leuven. Since 1991, he is a staff member of imec (Leuven). He has been a NATO Science Fellow at Bellcore (USA, 1991-92) and AST-fellow in the Joint Research Center for Atom Technology (Japan, 1998). In his research career, he has been leading activities on integration of novel materials at device level and new functionalities at systems level. In 2003, he became associate vice president at imec for the Microsystems division. In 2005, Jo started Holst Centre (Eindhoven) and became CEO of imec-Netherlands. From 2009 to 2011, he headed imec’s unit Smart Systems and Energy Technology as senior vice president in the imec group. In 2011, he was appointed CTO of imec corporate. He is a part-time professor at the KU Leuven and visiting professor at the TU Delft.
Invited Talk 1
Advancing CMOS Beyond the Si Roadmap: Chronicle of a (R)evolution Foretold
Marc Heyns, imec, Katholieke Universiteit Leuven

Summary:
Over the last years many new materials have been introduced in advanced CMOS processes in order to continue to progress along the scaling roadmap. Replacing the SiO2/poly-Si stack with deposited high-k gate dielectrics and metal gates was a major challenge in this respect. In the near future, even bigger hurdles have to be overcome that will take us beyond the Si roadmap by introducing high mobility channel materials. Materials such as Ge and III/V compounds are used to meet the power and performance specifications of advanced CMOS technologies. This will go together with the introduction of new device concepts, such as implant-free quantum well devices that fully exploit the unique properties of these materials. Tunnel-FETs, where the III/V material may be either introduced only in the source or in the complete device, can provide superior performance at lower power consumption by virtue of their improved subthreshold behavior. Vertical surround gate devices can be produced from III/V nanowires directly grown on silicon, allowing the introduction of a wide range of III/V materials and functionalities on Si. The introduction of new materials and devices also generate exciting possibilities for extended functionalities and new memory concepts.

Presenter Biography:
Marc Heyns was born in Turnhout, Belgium. He received the M.S. degree in Applied Sciences (Electronics) in 1979 and the Ph.D. degree in 1986 from the Katholieke Universiteit Leuven, Belgium. In January 1986, he joined imec, where he became Department Director and Program Director, responsible for a research group working on ultra-clean processing technology, advanced high-k gate stacks, metal gates, epitaxial deposition of materials, environmentally benign processing, and novel high-mobility substrate materials. As program director of the “Explore” program he was responsible for performing exploratory research on nanotechnology, novel materials and devices for ultimate CMOS technology, and novel memory concepts. He became an imec-Fellow in 2001 and a professor at the Katholieke Universiteit Leuven at the Department of Metallurgy and Materials Engineering in 2005. He has authored or co-authored more than 400 publications in scientific peer-reviewed journals, more than 800 contributions at scientific conferences, including more than 80 invited presentations, has edited or contributed to various books, and holds more than 30 patents.

Invited Talk 2
Smart Power Technology on SOI
Piet Wessels, NXP Semiconductors

Summary:
Smart power technologies are widely used in semiconductors. The technologies are derived from baseline CMOS technologies. Most recent smart power technologies are built on 140 nm CMOS. With the help of extra mask-layers, high voltage devices can be built up to 100 V or 200 V. These technologies are being used for power applications like LED control ICs, audio amplifiers, power management units, automotive transceivers, etc. The high voltage transistors support external drive, for example for LEDs. The digital transistors help by adding more functionality. NXP has built smart power technologies on SOI. The SOI enables full electrical isolation of individual devices. Besides robustness improvement, this also improves functionality, for example in EMC for transceivers (in automotive) and THD in audio amplifiers. The full electrical isolation also enables the integration of minority carrier devices like LIGBTs.

Presenter Biography:
Piet Wessels was born in The Hague, Netherlands. He studied physics at the Technical University of Delft. His master thesis was on the topic of titanium silicide multilayered structures. He joined Philips Semiconductors in 1987, where he started as process development engineer on BiMOS processes. In 1991, he led the development of a 700 V embedded BCD technology. In 1995, he was process integration manager at a discrete semiconductor factory. In 2004, he led a process integration and process development department at a 5 inch, 600K wafer factory. In 2006, he became director of process development for high voltage and power technologies within NXP, where his team has to develop technologies for factories internal and external to NXP. One of the recent developments is ABCD9: the first C13 embedded 100 V technology in the world. This is an SOI based technology. Piet also leads NXP’s new technology team in the area of high voltage and power. In this platform all research and development groups, factories, and business development groups within NXP, which work in the HV domain; sit together to define the NXP HVP technology roadmap, initiate new development programs, execute benchmark studies, define R&D roadmaps, etc.
Invited Talk 3
ESDA Advanced Topic Ad-Hoc Working Group on Electrical Overstress EOS
Jean-Luc Lefebvre, Presto Engineering

Summary:
Electrical overstress (EOS) is a major cause of IC failure in manufacturing and in the field. Electrostatic Discharge (ESD) is a subset of EOS which has received significant attention in both factory control and designed-in protection. However, the remaining forms of EOS have not been as systemically studied in spite of continued IC failure. ESDA has convened an ad-hoc working group of 11 members from 9 companies with the goal of publishing an advanced technical report (TR) on EOS in September 2012. This document would point to future work and efforts needed by the industry, as well as provide a resource to discuss and clarify the EOS issues.

The scope of the work for this TR is:

a) Clarification of EOS definitions and allied topics such as absolute maximum ratings (AMR), safe operating area (SOA), and electromagnetic interference (EMI).
b) Reporting the state of the art in EOS abatement.
c) Providing an overall categorizing framework within which to understand the various EOS threats within the manufacturing and product life-cycle.
d) Suggesting a way forward in both research and standards development to better protect against EOS.

Presenter Biography:
Jean-Luc Lefebvre has more than 31 years of experience in the semiconductor industry based in Caen France, mainly focused on testing, quality, reliability, and EOS testing. He started in 1980 as an electronics engineer to implement test programs and hardware product interfaces on high pin-count gate array automated test equipment in Philips Semiconductors. He then worked as customer support for video and audio tuner IC business and provided ESD/EOS audits to in-house and customer sites. In 1990, he created an in-house EOS test service laboratory. For twelve years, he led Philips (now NXP) technical EOS team focusing on test method and equipment. At NXP, he defined a new over voltage stress (OVS) test method and presented a poster at the 2008 IEW, and a paper at the 2009 ESREF. Currently, he is the EOS/EMC field application engineer in Presto-Engineering. He leads the ESDA EOS WG, and is the technical leader of SESAMES European consortium, aiming to standardize an OVS test method to reduce EOS failure rate.

Invited Talk 4
System Level EMC/ESD Design – Challenges and Opportunities
Pasi Tamminen, NOKIA Corporation

Summary:
The trend of smaller and more clever electronic products has always put pressure on EMC/ESD design. However, the worst scenarios with EMC/ESD challenges haven’t been realized and the current products with GHz range frequencies and multiple functions still work pretty well. As the trend continues, the shrinking IC devices, lower operation voltages, and especially the changing economic environment will challenge designers trying to create EMC/ESD robust products. In this presentation, I will give a few examples, to show some limitations and opportunities that consumer electronics manufacturing will see in the near future.

Presenter Biography:
Pasi Tamminen received the M.Sc degree in electronics engineering from Oulu University, Faculty of Technology, Finland, in 1997. He worked for NOKIA Networks for four years with a focus on new electronics production technology, process control, and Design for Manufacturability. In 2001-2004, he was with VTT Technical Research Centre of Finland, where he worked in a group developing risk management and ESD protection control methods for electronics industry. He received iNARTE ESD Engineer certification in 2004 and has more than 15 publications on ESD and cleanroom areas. Since the beginning of 2005, he has worked for NOKIA Corporation, where he is managing ESD, clean manufacturing, and EMC control related activities in manufacturing and product design.

Evening Talk
Belgian Beer Culture: The Biotechnological Art of Beer Creation
Gert De Rouck

Belgian beer is well known nowadays in the whole world. More than 1200 different beers in a wide range of beer styles (beers from Trappist Monks, Abbey beers, high alcohol specialty beers, Lagers, and even spontaneous fermented acidic beers) are available in the international market. During this session, an overview of the history of the Belgian Beer culture will be presented together with the question: what is Belgian Beer culture? Beer is made with only 4 to 6 ingredients. How can Belgian brewers create all these beer styles and varieties with this limited number of raw materials?
Get an Overview of Technology Challenges!

Chairman:
Horst Gieser (Fraunhofer EMFT)

This year’s seminars provide a concise and up to date overview on five complex key themes of the IEW 2012. Three of them are focused on assessing, differentiating, and mitigating the risk of ESD weakness at the device level from system level issues and cases of EOS, which turn out to be the majority of customer complaints. Concise failure analysis is key to understanding the root cause and guiding the effort for failure reproduction in a laboratory. In view of SoC this analysis becomes more and more difficult as feature sizes are shrinking to below tens of nanometers, metallization layers increase, and picosecond variations count, and even worse, several dies will be stacked into 3D systems. One seminar introduces the art of designing robust ESD protection for analog and high voltage technologies to be operated in harsh environments. Another seminar provides a view up the scaling path into the world of multigated FinFETs and their ESD protection. The last seminar will discuss how to bridge the gap between an IC Design and its application in view of ESD and EMC.

Seminar 1
Electrical Overstress (EOS) of Automotive Semiconductors -- Root Causes and Conclusions
Christoph Thienel, Robert Bosch GmbH

Summary:
Electrical Overstress (EOS) is one of the last not yet fully understood root causes for failing semiconductors in the automotive area. It often is misleadingly mixed up with Electrostatic Discharge (ESD). Sometimes it is wrongly assumed EOS may be caused by a weak design or a weak technology. On the contrary, it is a very common out of spec operation mode, which may destroy semiconductors. In the vast majority of cases there is no ESD event ahead of EOS pulse. Normally, it is difficult to clarify the root causes, but often EOS simply is caused by mechanical reasons or plugging under voltage (hot plugging). So, EOS should be investigated and cared about much more.

Presenter Biography:
Christoph Thienel was born in Bamberg, Bavaria, Germany. He earned a Physics Diploma (Dipl.-Phys, Univ.) from the Friedrich-Alexander-Universität of Erlangen. Since 1984, Christoph has worked with Robert Bosch GmbH in Reutlingen, testing, releasing, and analyzing Bosch semiconductors. Since 2005, he has done intensive studies of EOS in the automotive industry, and in July 2011, published the ZVEI White Paper: “First-Mate Last-Break Grounding Contacts in the Automotive Industry.”

Seminar 2
EOS / ESD Related Product Failure Analysis
Peter Egger, Infineon Technologies AG

Summary:
Physical root cause finding is an essential part in understanding the behavior of failing products and the development of appropriate countermeasures. Especially in advanced technologies with up to 12 metal layers and structure sizes below the spacial resolution of FA tools, product failure analysis on ESD or EOS fails is no longer a simple task. This seminar will give a brief overview about standard tools used for global fault isolation (lock-in IR thermography, emission microscopy, laser based techniques), their advantages and limitations. Dependent on the structure size of the product and failure mode, these techniques cannot provide the exact localization of the fail. Additional methods on transistor level (micro- and nano-probing) are necessary to generate a reliable failure hypothesis for successful physical preparation. Case studies will be presented covering unusual failure modes and ‘non visual defects’ caused by ESD stress. Finally, ESD versus EOS aspects, as well as the FA contribution on these issues are discussed.

Presenter Biography:
Peter Egger received his diploma in electrical engineering in 1992 from the Technical University Munich (TUM). He joined the ATIS-Group as the chair for Integrated Circuits at the TUM and worked several years on ESD protection schemes and failure analysis. Between 1994 and 1999, he worked at the Fraunhofer Institute for Solid State Technology (FhG IFT) in the field of CMOS process transfer, product engineering, and failure analysis. In 1999, he joined the failure analysis department of Infineon Technologies AG. His main focus is failure analysis of highly integrated semiconductor circuits for product and technology ramp-up.
Seminar 3
ESD Protection in FinFET Technologies
Steven Thijs, imec

Summary:
FinFET technology is widely accepted as being one of the main candidates to continue device scaling according to Moore’s law beyond the 16 nm node. FinFET devices indeed have superior scalability and very good channel control. FinFETs can be processed both on Silicon-On-Insulator (SOI) or on bulk substrates. Last year, Intel announced first mass production of Bulk-FinFET for their 22 nm processors. This seminar presents an overview of 6 years of ESD research on both SOI- and Bulk-FinFET technology. Basic ESD protection devices are investigated and the influence of FinFET specific parameters is highlighted.

Presenter Biography:
Steven received his M.Sc. and Ph.D. degrees in Electrotechnical engineering from the Katholieke Universiteit Leuven (KUL), Belgium, in 2001 and 2009, respectively. He joined the Silicon Processing and Device Reliability group of imec in 2001, where he was involved in ESD protection design, layout, simulation and characterization on CMOS and BiCMOS technologies, and in RF circuit design with ESD protection. In 2006, he started working in the field of ESD protection for FinFET devices and for RF CMOS circuits. He received the best paper and best student paper award from the EOS/ESD Symposium in 2004 and 2008, respectively; the Jan Van Vessem award at ISSCC 2011, and the best paper award at the ESD Forum 2011. He served as a member of the technical program committee of the EOS/ESD Symposia 2007-2010, IRPS 2009, and IEW 2011-2012. He is a member of IEEE and a peer reviewer for various IEEE journals. He authored and co-authored over 100 publications and holds several US patents in the field. In 2011, he moved to the Printed Board Assembly group in imec, where he is R&D project leader aiming to provide scientifically sound methodologies to develop high quality, reliable, and cost-effective electronic modules.

Seminar 4
ESD Design in High Voltage Technologies
Joost Willemen, Infineon Technologies AG; Lorenzo Cerati, STMicroelectronics

Summary:
This seminar gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 V upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback, active clamps, etc.). Finally, HV-technology and design related challenges regarding ESD protection are discussed, with a special focus on parasitic bipolar formation and their impact on device performance.

Presenter Biographies:
Joost Willemen received his master’s and PhD degree in Electrical Engineering from the DIMES Institute, Delft University of Technology, in 1993 and 1998, respectively. From 1998 to 2005, he was with the automotive electronics division of Robert Bosch GmbH in Reutlingen, Germany. At Bosch he developed methodologies for HBM and CDM circuit level simulation, high-current ESD device models, and a simulation environment for fully-coupled electro-thermal circuit simulations. In 2005, he joined Infineon Technologies AG in Munich, Germany. Until recently, his main responsibilities were the development of ESD concepts and devices in BCD technologies for automotive applications and ESD consultancy for automotive IC design. Since the end of 2011, he is with the RF and Protection development group at Infineon, working on discrete ESD devices and interface products for system level ESD protection. Joost’s research interests are in the field of physics of ESD devices and advanced ESD characterization methods. He authored and co-authored various papers on ESD device and modeling topics. He is member of the Industry Council on ESD Target Levels and served on the IEW 2012 organization committee.

Lorenzo Cerati graduated in telecommunication engineering at the “Politecnico di Milano” Technical University in 1998, discussing a thesis on a CdZnTe cross-connect for optical networks. Since 2000, he has been working at STMicroelectronics in the ESD protections development team for Smart power technologies. He is now the manager of the group responsible for ESD protections development, latch-up immunity, and bipolar parasitic analysis in BCD processes. His responsibilities include the simulation of new solutions (both device and circuit-level), the definition of layout and design rules and their validation on silicon. He is in charge of design teams support to define, implement and debug complex ESD architectures. Since 2006, he is also coordinating a team working on Front-End/Back-End compatibility assessment for Smart-Power technologies. Lorenzo represents STMicroelectronics in the ESDA standardization committees and authored several papers on ESD presented at the major conferences, including EOS/ESD Symposium, IEW, and ESREF where he is currently serving on the Technical Program Committees.
Seminar 5
Bridging the Gap Between IC Design and its Application
Mart Coenen, EMCMCC

Summary:
IC ESD protection measures need to combine the handling constraints effectively without causing any functional drawback to its foreseen application. With today’s nanometer processes, the vulnerability of the circuits to be protected increases, though on the opposite side the RF immunity requirements, are enhanced for the so called ‘global’ pins at the application level. Questions need to be answered on what can and has to be done at the application, in the package and on-silicon to close this gap efficiently while being able to demonstrate compliance to the ESD standards applicable at the various verification levels concerned.

Presenter Biography:
Mart Coenen (BSc ‘79) has over 32 years experience in EMC in various fields, has published books, and many national and international papers. Since 1988, he is actively involved in international EMC standardization. He is the former project leader of the standards: IEC 61000-4-6 (Immunity to conducted disturbances induced by radio-frequency fields) and IEC 61000-4-2 (Electrostatic discharge immunity test), but moved his focus towards EMC in integrated circuits. He has been the convener of IEC TC47A/WG9 and member of WG2 for which he was given the IEC 1906 award in 2006 after publishing various parts of the IEC 61967-x, IEC 62132-x and IEC 62215-x series. He is co-founder of the Dutch EMC/ESD Society and part-time lecturer at Post Academic EMC courses. Since 1994, he has owned his private consulting company EMCMCC, where he focuses on EMC and system integration issues in e-Hardware.
Discussion Group A.1
The First Thing Industry Needs is a Test Standard for EOS Besides ESD and Latch-Up
Moderator: Jean Luc Lefebvre, Presto Engineering
jean-luc.lefebvre@presto-eng.com

EOS currently is a loosely defined category of electrical stress. Does EOS relate to a failure signature or the root cause of the failure? Do ESD and latch-up events form subsets of the whole range of EOS events? If so, what ‘other EOS events’ are there? Which part of the failures do these ‘other EOS events’ constitute? How is IC component robustness determined and guaranteed and how do absolute maximum rating (AMR) levels relate to this? Would a test standard method for EOS, in addition to those for ESD and Latch-up, help to improve robustness levels of ICs, components and boards? This should be an excellent meeting to share your EOS, besides ESD and Latch-up, experiences in quality and reliability test scope.

Discussion Group A.2
ESD Thresholds and Actual Risk of Failure
Moderator: Terry Welsher, Dangelmayer Associates
terry@dangelmayer.com

How can we change the current way of working to include statistics of ESD events and product failure? HBM and CDM ESD thresholds have been useful as “figures of merit” to drive improvements in protection circuits. However, the relationship of these thresholds to actual quality or reliability risks is not well-understood. Many users believe that the risk of failure rises dramatically when the threshold falls even a small amount below the usual threshold requirements. This discussion group will explore better ways of communicating the risk of failure to users, better measures of ESD robustness than the simple threshold value and whether it is possible to characterize an ESD manufacturing process based on measurements (auditing).

Discussion Group A.3
System Level ESD
Moderator: Fabrice Caignet, LAAS-CNRS
fcaignet@laas.fr

ESD system level prediction has become a challenging issue for both IC suppliers and Equipment Manufacturers (EMs). Do you think that ESD protections can be described with only a few parameters? Do you think that IC suppliers can use a shared model to ensure that ICs can handle system level ESD events? Can such a model help the EMs to optimize their systems? Can such models be exchanged between suppliers and EMs? The question of the relevant parameters for system level simulation that can be used by suppliers and/or EMs will be addressed at this meeting.
Discussion Group A.4
Does Standard ESD Qualification Testing Have Any Real-World Relevance?
Moderator: James W. Miller, Freescale Semiconductor
rvkg60@freescale.com

ESD qualification success on IC products is often based solely on performance to the venerable industry standard component level HBM and CDM stress tests. But the stress events which the HBM/CDM simulators attempt to reproduce represents only a tiny part of the range of real-world powered and un-powered, as well as component and system level EOS/ESD stress events an IC may suffer during test, system assembly, and in the field. Further, it can be argued that for most products, the vast majority of EOS/ESD failures are not due to classical HBM/CDM stress events. If the above statements are true, then why do ESD designers often focus their efforts on passing just HBM/CDM? Our design goal should be products robust to real-world EOS/ESD stress events. How relevant is HBM/CDM testing today? What types of EOS/ESD fails are you seeing on products today? Are you designing products to be robust for these failure modes and adding tests in your qualification plans? Moving forward, how do we (the industry) define an appropriate set of EOS/ESD stress events to put real-world relevance back into ESD qualification?

Discussion Group B.1
The Industry Should Focus on ESD Control Since all Measures Taken There are More Effective and Cheaper Than Design Solutions
Moderator: Yorgos Christoforou, NXP Semiconductors
yorgos.christoforou@nxp.com

How much of the EOS/ESD issues in your industry can be solved by (a) improving EOS/ESD robustness of the designs or (b) removing, through better control, the EOS/ESD root cause or latent failures? This is the topic of this discussion. Several questions can be addressed: Which control methods do you use in your industry? Which design methods do you use in your industry? What is the Return-on-Investment for each approach? Have you encountered cases where weak products can have an excellent performance in the final product thanks to robust control techniques? Do you think the two approaches correlate (e.g. more design needs less control and vice versa)? Does the choice of the approach depend on the type of the market/industry addressed? What is the preferred approach of the management in your industry? Will the industry direction, with respect to this topic, have to change in the future with the development of new technologies? The flow of the discussion will mainly depend on your participation.

Discussion Group B.2
ESD Testing: Is it Time for a Revolutionary Change in Test Methods/Testers, Rather than Small Evolutions?
Moderator: Tom Meuse, Thermo Fisher Scientific
tom.meuse@thermofisher.com

ESD testing, being device level or system level, HBM, CDM or the now “obsolete” MM test methods have evolved over the years to incorporate knowledge gained from continued use of the present standards. Testers have also evolved to incorporate changes made to the standards or to eliminate findings during usage, such as the

Discussion Group B.2 Continued
Trailing Pulse phenomena. The question today is: do we need to rethink ESD testing all together? CDM testing may take another direction, away from field induced testing, to allow testing of smaller devices and to improve testing repeatability. Should HBM and System Level (or HMM) move away from today’s testing requirements? And if so, what are your suggestions?

Discussion Group B.3
Everything You Always Wanted to Know About the Secrets of a Successful Cooperation Between Academia and Industry
Moderators: Marise Bafleur, LAAS-CNRS; Patrice Besse, Freescale Semiconductor
marise@laas.fr • pbes01@freescale.com

There are many barriers (cultural, institutional, operational) that could make cooperation between academia and industry partners difficult. However, overcoming these barriers can result in a fruitful cross-fertilization that can lead to innovation. In the field of EOS/ESD, over the last ten years, more and more papers presented at the IEW and EOS/ESD Symposium are issued from academia-industry cooperative projects. We invite you to share your experience in bridging these cultural gaps and also discuss problems that are still pending. We will open the discussion with the example of a sustainable partnering in the field of ESD between LAAS-CNRS and Freescale Semiconductor.

Discussion Group B.4
ESD verification tools: will we get to push-button solutions?
Moderator: Matthew Hogan, Mentor Graphics
matthew_hogan@mentor.com

There has been a surge in development of newly designed EDA verification tools over the past few years. For ESD applications, much of the previous best practices included visual inspection, home-grown tools, SPICE simulations and flows that were put together using traditional DRC, LVS and ERC solutions. Designers expect ESD verification tools to provide a push button use model where the result provides a clear indication of where a certain rule has violated the constraint, and how this should be fixed. Much like how DRC checks operate today, the designer then makes the change, re-runs the design and repeats until all violations are removed. Can this goal be achieved for general purpose ESD verification tools as well? Or should we accept that ESD verification tools cannot be made as general as DRC verification tools? What level of use model and debugging is suitable? The same as DRC? LVS? Or something else? Are the expectations for topological and layout checks different? Is it inevitable that results need interpretation? That checks which are tailored for the design styles of one company require modification for a different design style at another? Can all aspects of an ESD network be checked by software? What is your experience in practice, when using currently available tools? This should be an excellent meeting to share your lessons learned and pick up ideas for improved ESD design verification at your company and/or insights to improved ESD verification software offered by EDA vendors.
Special Interest Groups
Cooperating on Important ESD Topics!

Chairman: Bart Keppens, Sofics

Similar to previous years, the IEW workshop provides an opportunity for special interest groups (SIGs) to meet. These SIGs are teams focused on one compelling topic of mutual interest. Some of these groups have been successfully cooperating for several years on important ESD topics – with continued momentum stimulated at the IEW! Six SIGs are scheduled for IEW 2012 as outlined here. Attendees are also encouraged to form new SIGs as they see fit. If you would like to form a new SIG please contact Bart Keppens at bkeppens@sofics.com.

Special Interest Group A.1
ESD Data Analysis Tools
Coordinator: David Tremouilles, LAAS-CNRS
david.tremouilles@laas.fr

Frequently ESD engineers must analyze measurement results from different test methods. They extract the most relevant ESD parameters from a large set of test structures and use it to select the appropriate ESD clamp devices and full chip protection concepts. Currently, a lot of that analysis is being handled by general purpose spreadsheets. However, to cope with the growing amount of data a dedicated analysis tool is needed that has import functions for all kinds of ESD test equipment and industry standardized parameter extraction procedures. In the last year, an open source project has been started to develop such a tool for and by ESD engineers: http://code.google.com/p/esdanalysistools/.

ESD engineers involved in ESD analysis, data manipulation, and with an interest to support this tool creation are invited to join our SIG discussion. Programming skills are not required to join!

Special Interest Group A.2
Transient Latch-up (TLU)
Coordinator: Wolfgang Stadler, Intel Mobile Communications
wolfgang.stadler@intel.com

Transients are becoming increasingly important for systems and there is no doubt that those transients can trigger latch-up or functional upsets. Therefore, meaningful tests for transient latch-up (TLU) robustness of products are inevitable. However, the former TLU standard practice ANSI/ESD SP5.4, which is the only standard covering TLU, is hardly used today and does not fulfill the current requirements on a TLU test. Therefore, ESDA Working Group 5.4 has decided to re-designate ANSI/ESD SP5.4 as a technical report (TR). Work on a further TR has started that may lead to a “new” TLU standard. A significant amount of examples on TLU “real-world” events is already collected in the TR. In this SIG we will discuss the latest activities in the standardization committees and continue to collect early inputs to those activities from industry experts to support and impact these standardization activities.

Everyone is invited to join this SIG and provide input on appropriate measurement techniques, pulse characteristics or field experiences with TLU.
Special Interest Group A.3
ESD Parameters for ESD EDA Flow
Coordinator: Harald Gossner, Intel Mobile Communications
harald.gossner@intel.com

Today, IC designers are collaborating with many IP vendors and several foundries. Therefore, for a comprehensive ESD concept and easy verification, information from the internal design team, IP vendors, and foundries must be combined. A special interest group of foundries, IP vendors, and IC suppliers was created to summarize the set of models and input parameters required from the different partners involved. If we can reach an agreement about the relevant parameters and set of data to be provided by foundries and IP vendors, then this would be a win/win/win for all. The ramp to volume production can be reduced and additional flexibility in design-in of 3rd party IP will be possible.

Peers from foundries, IP and EDA vendors, and IC suppliers are invited to join this SIG. Together we will review and align on the required parameters for a consistent ESD design and ESD verification flow.

Special Interest Group B.1
Non-ESD Requirements that are Relevant for ESD Protection
Coordinator: Benjamin Van Camp, Sofics
bvancamp@sofics.com

For ESD and latch-up requirements it is easy to translate the specifications to expected behavior during standalone clamp analysis. However, for a number of functional requirements this is not so easy and additional analysis approaches must be added. For instance, DPI tests performed on automotive parts require ESD clamps that do not rely on RC effects. For the design of clamps that comply with ISO 7637-2 load dump pulses, it is unclear if it is sufficient to increase the trigger voltage. For IEC 61000-4-4 and IEC 61000-4-5 that describe burst and long duration pulses, long duration TLP, and/or DC analysis is required.

The people in this SIG want to summarize the different requirements and look forward to hearing from experts in the field how functional aspects can be translated into requirements for ESD clamps.

Special Interest Group B.2
Electrical Overstress
Coordinator: Jean-Luc Lefebvre, Presto Engineering Europe
jean-luc.lefebvre@presto-eng.com

It is well-known that electrical overstress (EOS) is a major cause of IC failure in manufacturing and in the field. Events such as ESD,Latch-up, EMI and other phenomena are sub-groups of EOS events. Specifically ESD has received significant attention in both factory control and designed-in protection. However, the remaining forms of EOS have not been studied as systemically in spite of continued IC failure due to the non-ESD causes. ESDA has convened an ad-hoc working group (WG) of 11 members from 9 companies with the goal of publishing an advanced (high level) Technical Report (TR) by Sept 2012.

ESD engineers involved in EOS analysis and debugging are invited to join our SIG discussion and help drive the Technical Report.

Special Interest Group B.3
Charged Board Event
Coordinator: Pasi.K. Tamminen, Nokia
pasi.k.tamminen@nokia.com

CBE (Charged Board Event) is related to a system board getting charged and then discharged through a variety of means while creating a strong CDM like event on of the IC pins. The CBE working group is tasked with writing a technical report (TR) on this subject. It is not recommended to make CBE as a standard similar to HBM or CDM since it will not be practical or realistic in light of too many variables. However, the technical report is meant to provide a guideline to debug customer issues related to CBE for ESD and FA engineers.

Attendees interested in CBE are invited to join the SIG discussion and support the technical report.
Technical Program

Chairman: Guido Notermans, ST-Ericsson

The technical program consists of a discussion of peer-reviewed posters in three sessions. You may expect a wide range of current ESD subjects, ranging from hot topics like CDM and system level testing, to mysterious HBM fails, and new GaAs protection devices. The presentations are preceded by a brief podium introduction by each author. These presentations can be used by the workshop participants to select the posters for discussion.

Technical Session A

A.1 - Transient Latch-up in Large NFET Switch Arrays
Nathaniel Peachey, RFMD; Rick Phelps, IBM
Power management circuits often employ large switching arrays to provide a stable voltage output. The displacement currents can be large enough to trigger snapback during operation and the NMOS array can latch on and sustain damage. A particular example of this type of transient latch-up phenomena is described.

A.2 - ESD Induced Latch-Up Case and Prevention Measures
Andy Noiret, Micronas
The poster presents a case of ESD stress induced latch-up found in an late stage of an integrated circuit development. The Failure Analysis led to more robust layout design rules in the mixed signal high voltage technology C45 (0.45μm).

A.3 - About the ESD Sensitivity Classification According to HBM
Tilo Brodbeck, Adrien Ille, Jan Weigmann, Infineon Technologies AG; Wolfgang Stadler, Intel Mobile Communication
The limits of HBM device classification will be investigated. The present HBM standard cannot guarantee clear results without ambiguity regarding the pin-combination sets, the HBM classification procedure, and the coverage of the statistical aspect of the failing modes.

A.4 - Design and Performance of GaAs Schottky Diodes for On-Chip IC Device ESD Protection
Frank Gao, David Whitefield, David Petzold, Dylan Bartle, Skyworks Solutions
GaAs devices are typically used when there is an RF performance advantage over standard silicon processes. Traditional ESD protection methods degrade RF performance and are often not used. Therefore, few characterization data are available. In this work, GaAs FETs and capacitors have been characterized, and an array of ESD protection diodes were analyzed.

A.5 - Improving IBIS for System Level ESD Simulation
Fabrice Caignet, Nicolas Monnereau, Nicolas Nolhier, David Trémoilles, Marise Bafleur, LAAS-CNRS
An extended and improved IBIS model is presented. Including information extracted from TLP measurements that allow Equipment Manufacturers to predict the ESD performance of their circuit by accurate simulations during the design phase, and yet protect the intellectual property of semiconductor manufacturers.

A.6 - Design Considerations to Reduce Process Sensitivity for Transient-Triggered Active Rail Clamps in Advanced CMOS Technologies
Sunitha Venkataraman, Cynthia Torres, David Catlett, Tim Rost, Chris Barr, Keith Burgess, Texas Instruments
As technologies advance, transient-triggered active MOSFET rail clamps can be more sensitive, not only to age related effects but also to process variations. This work offers a case study in the use of existing industry simulation tools to optimize ESD trigger circuits to make them less sensitive to parameter shifts due to aging and process variation.
Technical Session B

B.1 - Full TLP/vf-TLP Characterization of ESD Network Protection Based on Beta-Matrix Concept
Johan Bourgeat, Philippe Galy, Jean Jimenez, David Marin-Cudraz, STMicroelectronics

A Beta-Matrix is a new concept which integrates six SCRs in a common structure using a single triggering gate. This work introduces a trigger circuit able to turn on one of SCRs depending on which pins are stressed with which polarity, in a 32nm high-k metal-gate CMOS technology.

B.2 - Impact of Tester Source Impedance on HBM Failure Level
M. Scholz, imec, Vrije Universiteit Brussels; S.-H. Chen, G. Groeseneken, imec, Katholieke Universiteit Leuven; D. Linten, S. Thijs, imec; M. Sawada, HANWA; D. Johnsson, HPPI

The same device under test is stressed with a HBM tester and a so-called HBM-500 ESD tester. Although the current waveforms into a short are very similar, the different source impedances and discharge circuits cause a clear miscorrelation when connecting a device under test.

B.3 - Low Pin-Count Unexplained HBM Cumulative Effect
Andrea Boroni, Lorenzo Cerati, Leonardo Di Bicca, Gianluca D'Alesio, Fabio Quintana, Alberto Mena Hernandez, Laura Solevi, STMicroelectronics

The number of false failures in ESD qualification due to testing and IC parasitics is growing. This work presents an investigation of spurious cumulative effects due to zap on different pins, even when stressing a very limited number of pads.

B.4 - Bipolar ESD Structures for the System Level Timeframe
Jean-Philippe Laine, Patrice Besse, Alain Salles, Freescale Semiconductor

ESD system-level requirements imply design efforts to achieve fast and robust ESD structures. Several active bipolar ESD structures are tested with TLP measurement from 20 ns up to 1 us. Results show how its robustness depends on the concept configuration. A trade-off between size and concept is found.

B.5 - Low Voltage Diodes Metal Layout Optimization to Sustain System Level ESD Current Stress
Leonardo Di Bicca, Lorenzo Cerati, STMicroelectronics

The high current densities required by system level ESD standards are becoming difficult to reach in new Smart-Power technologies due to the use of thin metals. In this work a metal layout optimization using R3D simulations is presented to increase the current capability of ESD diodes in BCD8 technology.

B.6 - An SCR Clamp with a Dual-base ESD Detection Driver
A.A. Shibkov, Angstrom; V.A. Vashchenko, Maxim

A novel small footprint, low voltage, SCR clamp is proposed and validated using mixed-mode numerical simulations. The clamp combines a transient voltage detection circuit to control a dual-base triggered SCR.

Technical Session C

C.1 - ESD Solution for NC Pin of a Smart Card IC
Chang-Su Kim, Jae-Hyok Ko, Sung-Pil Jang, Kyoung-Soon Cho, Han-Gu Kim, Samsung

An ESD protection methodology for NC pins on smart card ICs is discussed. The failure mechanism is analyzed through discharge waveform measurement for a regular I/O pin during an ESD event at a neighboring NC pin. In addition, on- and off-chip ESD solutions are proposed.

C.2 - Utilizing a Keep-Out Zone of Through Silicon Vias for ESD Protection Devices in 3D Stacked ICs
Shih-Hung Chen, Steven Thijs, Dimitri Linten, Guido Groeseneken, imec

3D stacking of ICs connected with Through-Silicon-Vias (TSV) is a promising candidate for real systems-on-chip applications. However, mechanical strain induced by the TSV can impact MOSFET Vth and mobility. Therefore, a Keep-Out Zone (KOZ) is defined, which implies that active devices are forbidden in this area. This paper investigates the placement of ESD protection devices inside this KOZ.

C.3 - Pitfalls When Using the SEED Methodology
M. Scholz, imec, Vrije Universiteit Brussels; S.-H. Chen, G. Groeseneken, imec, Katholieke Universiteit Leuven; D. Linten, S. Thijs, imec; M. Sawada, HANWA

The SEED methodology is applied for comparison of two ESD protection clamps under system level ESD stress. It is shown that SEED cannot be used as a general design methodology. Instead the transient interaction between on-chip and off-chip ESD protection needs to be carefully studied to prevent an unexpected failure of the on-chip ESD protection during system level ESD stress.

C.4 - Contributions to the Variation of HMM Test Results
Richard Derlix, Theo Smedes, Rudolf Velghe, Maarten Swanenberg, NXP Semiconductors

An ESD gun test setup, including PCB/socket design and package selection, is presented. ESD tests with this setup give stable results although case studies demonstrate that small details may have significant effect on the results. Improvement of the setup is presented, by characterization of the effects of certain parameters.

C.5 - Understanding vf-TLP and TLP Stress-Induced Failure Mechanisms of ESD Devices in a 28nm Bulk CMOS Technology
Rahul Mishra, Junjun Li, James Di Sarro, Robert Gauthier, IBM

Physical failure analysis of 28nm bulk ESD devices shows different failure mechanisms depending on device design parameters and TLP testing type. The devices being studied are n+/pw diode and ESD silicide-blocked nMOSFET. It is shown that failure mode changes when devices are stressed with vf-TLP pulses. Two unexpected failure modes are uncovered in this paper.

C.6 - A Study of the TLP Voltage-Step Dependency of It2 in a 16V DDDMOS Process
Chia-Tsen Dai, Po-Yen Chiu, Ming-Dou Ker, National Chiao-Tung University; Fu-Yi Tsai, Yan-Hua Pan, Chia-Ku Tsai, Faraday Technology Corporation

In this work, the measured results of TLP tests of a traditional RC-triggered ESD clamp have different It2 levels when using different voltage steps in the TLP tester. Thus, in order to get a reasonable It2 result, the voltage-step dependency should be taken into consideration, especially in HV CMOS processes.
Call for Open Posters

In parallel to our reviewed poster sessions, all workshop participants are allowed to present open posters to discuss the latest developments in their work. Use this opportunity to discuss new results with your peers before they are in publishable form. Note that the open posters will not be published by the IEW organization in any form. Therefore, discussing your open poster does not impact later publication in any way.

Please indicate on the registration form your intention to bring a poster and send your draft by April 30, 2012, to the TPC Chair at guido.notermans@stericsson.com. Updates and late submissions are possible until the start of the workshop.

For more details on posters at the IEW, see the open-posters section of the IEW website: http://www.esda.org/IEW.htm.
### Monday, May 14, 2012

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
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<tr>
<td>12:00 PM-6:00 PM</td>
<td>Registration: Pick up badges and handouts.</td>
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<tr>
<td>12:00 PM-10:00 PM</td>
<td>Hotel check-in: Get room assignment &amp; room key.</td>
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</table>
| 1:30 PM-2:50 PM | Seminar 1: Electrical Overstress (EOS) of Automotive Semiconductors - Root Causes and Conclusions  
Christoph Thienel, Robert Bosch GmbH |
| 2:50 PM-4:10 PM | Seminar 2: EOS / ESD Related Product Failure Analysis  
Peter Egger, Infineon Technologies AG |
| 4:10 PM-4:40 PM | Break                                                                |
| 4:40 PM-6:00 PM | Seminar 3: ESD Protection in FinFET Technologies  
Steven Thijs, imec |
| 6:00 PM-7:30 PM | Dinner                                                               |
| 7:30 PM-8:30 PM | Evening Talk: The Biotechnological Art of Beer Creation             |

### Tuesday, May 15, 2012

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<tr>
<th>Time</th>
<th>Event</th>
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<tr>
<td>8:00 AM-8:10 AM</td>
<td>Welcome - Technical Program Introduction</td>
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| 8:10 AM-9:05 AM | Keynote: Game Changing Technologies in Health Care  
Jo De Boeck, imec |
| 9:05 AM-9:50 AM | Invited Talk #1: Advancing CMOS Beyond the Si Roadmap: Chronicle of a (R)evolution Foretold  
Marc Heyns, imec, Katholieke Universiteit Leuven |
| 9:50 AM-10:10 AM | Break                                                                |
| 10:10 AM-11:00 AM | Technical Session A:  
A.1 - Transient Latch-Up in Large NFET Switch Arrays  
Nathaniel Peachey, RFMD; Rick Phelps, IBM  
A.2 - ESD Induced Latch-Up Case and Prevention Measures  
Andy Noiret, Micronas  
A.3 - About the ESD Sensitivity Classification According to HBM  
Tilo Brodbeck, Adrien Ille, Wolfgang Stadler, Jan Weigmann, Infineon Technologies AG, Intel Mobile Communication  
A.4 - Design and Performance of GaAs Schottky Diodes for On-Chip IC Device ESD Protection  
Frank Gao, David Whitefield, David Petzold, Dylan Bartle, Skyworks Solutions  
A.5 - Improving IBIS for System Level ESD Simulation  
Fabrice Caignet, Nicolas Monnereau, Nicolas Nolhier, David Trémouilles, Marise Bafleur, LAAS-CNRS  
A.6 - Design Considerations to Reduce Process Sensitivity for Transient-Triggered Active Rail Clamps in Advanced CMOS Technologies  
Sunitha Venkataraman, Cynthia Torres, David Catlett, Tim Rost, Chris Barr, and Keith Burgess, Texas Instruments |
| 11:00 AM-12:00 PM | Poster Discussion Session A                                       |
| 12:00 PM-1:30 PM | Lunch                                                               |
| 1:30 PM-1:35 PM | Announcements                                                      |
**Tuesday, May 15, 2012 - continued**

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<th>Time</th>
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<tr>
<td>1:35 PM-2:20 PM</td>
<td>Invited Talk #2: Smart Power Technology on SOI&lt;br&gt;Piet Wessels, NXP Semiconductors</td>
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<td>2:20 PM-3:05 PM</td>
<td>Invited Talk #3: ESDA Advanced Topic Ad-hoc Working Group on Electrical Overstress (EOS)&lt;br&gt;Jean-Luc Lefebvre, Presto Engineering</td>
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<td>3:05 PM-3:25 PM</td>
<td>Break</td>
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<tr>
<td>4:15 PM-5:30 PM</td>
<td>Poster Discussion Session B</td>
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<tr>
<td>5:30 PM-7:00 PM</td>
<td>Dinner</td>
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<td>7:00 PM-8:00 PM</td>
<td>Discussion Group Session A: Parallel Groups&lt;br&gt;DG A.1 - The First Thing Industry Needs is a Test Standard for EOS Besides ESD andLatch-Up&lt;br&gt;DG A.2 - ESD Thresholds and Actual Risk of Failure&lt;br&gt;DG A.3 - System Level ESD&lt;br&gt;DG A.4 - Does Standard ESD Qualification Testing Have Any Real-World Relevance?</td>
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<td>8:00 PM-9:00 PM</td>
<td>Special Interest Group Session A: Parallel Groups&lt;br&gt;SIG A.1 - ESD Data Analysis Tools&lt;br&gt;SIG A.2 - Transient Latch-Up (TLU)&lt;br&gt;SIG A.3 - ESD Parameters for ESD EDA Flow</td>
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**Wednesday, May 16, 2012**

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<tr>
<td>8:00 AM-8:05 AM</td>
<td>Announcements</td>
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<td>8:05 AM-8:35 AM</td>
<td>Reports on DG &amp; SIG Session A</td>
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<td>8:35 AM-9:55 AM</td>
<td>Seminar 4: ESD Design in High Voltage Technologies&lt;br&gt;Joost Willemen, Infineon Technologies AG; Lorenzo Cerati, STMicroelectronics</td>
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<td>9:55 AM-10:10 AM</td>
<td>Group Picture</td>
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<td>10:10 AM-10:40 AM</td>
<td>Break</td>
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<td>10:40 AM-12:00 PM</td>
<td>Seminar 5: Bridging the Gap Between IC Design and its Application&lt;br&gt;Mart Coenen, EMCMCC</td>
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<td><strong>Wednesday, May 16, 2012 continued</strong></td>
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<tr>
<td>12:00 PM-1:00 PM</td>
<td>Lunch</td>
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<td>1:00 PM-5:00 PM</td>
<td>Free Time</td>
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<td>5:00 PM-6:00 PM</td>
<td><strong>Discussion Group Session B: Parallel Groups</strong></td>
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<td>DG B.1 - The Industry Should Focus on ESD Control Since all Measures Taken there are More Effective and Cheaper than Design Solutions</td>
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<td>DG B.2 - ESD Testing: Is it Time for a Revolutionary Change in Test Methods/testers, Rather than Small Evolutions?</td>
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<td>DG B.3 - Everything You Always Wanted to Know About the Secrets of a Successful Cooperation Between Academia and Industry</td>
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<td>DG B.4 - ESD Verification Tools: Will We Get to Push-button Solutions?</td>
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<td>6:00 PM-7:00 PM</td>
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<td>SIG B.2 - Electrical Overstress</td>
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<td>SIG B.3 - Charged Board Event</td>
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<td>Dinner</td>
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<td><strong>Thursday, May 17, 2012</strong></td>
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<td>8:00 AM-8:05 AM</td>
<td>Announcements</td>
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<td>8:05 AM-8:35 AM</td>
<td>Reports on DG &amp; SIG Sessions B</td>
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<td>8:35 AM-8:55 AM</td>
<td>Industry Council Report</td>
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<td>8:55 AM-9:40 AM</td>
<td><strong>Invited Talk 4: System Level EMC/ESD Design – Challenges and Opportunities</strong></td>
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<td>9:40 AM-9:55 AM</td>
<td>Break</td>
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<tr>
<td>9:55 AM-10:45 AM</td>
<td><strong>Technical Session C:</strong></td>
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<td>C.1 - ESD Solution for NC Pin of a Smart Card IC</td>
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<td>Chang-Su Kim, Jae-Hyok Ko, Sung-Pil Jang, Kyoung-Soon Cho, Han-Gu Kim, Samsung</td>
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<td>C.4 - Contributions to the Variation of HMM Test Results</td>
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<td>Richard Derikx, Theo Smedes, Rudolf Velghe, Maarten Swanenberg, NXP Semiconductors</td>
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<td>C.5 - Understanding vt-TLP and TLP Stress-Induced Failure Mechanisms of ESD Devices in a 28nm Bulk CMOS Technology</td>
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<td>Chia-Tsen Dai, Po-Yen Chiu, Ming-Dou Ker, National Chiao-Tung University; Fu-Yi Tsai, Yan-Hua Pan, Chia-Ku Tsai, Faraday Technology Corporation</td>
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<tr>
<td>10:45 AM-10:55 AM</td>
<td>2013 Announcements and Closing</td>
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<td>10:55 AM-12:00 PM</td>
<td><strong>Poster Discussion Session C</strong></td>
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<tr>
<td>12:00 PM-1:00 PM</td>
<td>Lunch</td>
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IEW ACCOMMODATIONS:
The IEW will retreat in a priory founded in 1395 in Corsendonk, Belgium. The Priory of Corsendonk is hidden in the green woods of Oud-Turnhout and is surrounded by centuries-old trees and pastures. On this territory a Guesthouse - next to the Women’s House and the Laymen’s House - used to serve as residence of travellers who had not yet found a place to stay at dusk. There are spacious standard rooms and small but charming monk rooms, each equipped with private bathroom facilities, telephone and internet access. The physical isolation of the location and the absence of distractions encourage extensive interaction among the workshop attendees. Lodging and all meals are included in the registration costs for the workshop.

● Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 1-315-339-6937.
● Please have lunch before you arrive at the Conference Center on Monday; there is no lunch available on Monday.

GUESTS AND SPOUSES:
You are welcome to bring a guest to IEW. Accomodations are available for spouses and guests in the same room for an extra 30 Euro a night, which includes breakfast. Guest fees will be charged separately and must be paid directly to the hotel. Attendees must list guests with their initial registration to allow for room arrangements.

RESPONSIBILITIES OF ATTENDEES:
Please come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IEW!

In keeping with the relaxed and informal atmosphere of the Workshop, we ask that attendees not overtly solicit, promote, or attempt to sell a commercial product or service at the The Priory of Corsendonk Conference Center. On the other hand, we strongly encourage making business acquaintances and arranging meetings to be held after the workshop.

SURROUNDING AREA:
The Priory of Corsendonk is hidden in the green woods of Oud-Turnhout and is surrounded by centuries-old trees and pastures. You can see and experience the beauty of the area along several different hiking routes. Each route shows another aspect of the nature of the “Kempen.” In the surrounding area of the Priory, you can also walk along the idyllic “Corsendonkroute.”

You can rent a bicycle and with the local cycling junctions network, you can set up your own cycling tour. You determine yourself the number of kilometers through woods or through meadows, how many attractions or pubs you would like to visit, etc.

The center of Turnhout is about 15 kilometres from the Priory. Turnhout offers a variety of possibilities to experience including museums, architecture such as the old city hall, the 12th century castle of the Dukes of Brabant, the Church of Saint Peter, the 13th beguinage (one of the most beautiful in Belgium and UNESCO World Heritage), or the old cemetery located in the street “Kwakkelstraat”.

Enjoy your “Free Time” and explore the surrounding area!
TRANSPORTATION

For complete information please visit http://www.esda.org/IEW_Travel_Accomodations.html

The Corsendonk Priory is located near the Dutch border, 45 km east of Antwerp, 90 km northeast of Brussels Airport, 40 km west of Eindhoven, and a few minutes from the E34 highway.

Priorij Corsendonk
Corsendonk 5
2360 Oud-Turnhout
BELGIE
Phone: +32 (0) 14 46 28 00
Fax : +32 (0) 14 39 02 60
E-mail : info.priorij@corsendonkhotels.com

Train Service:
There are 17 trains a day from the Brussels Airport. It will take two hours to reach Turnhout, and you will have to change trains twice. First you take the train to Brussel Nord, there you take the train to Antwerpen –Berchem, then the train to turnhout.
For train schedules and information visit http://hari.b-rail.be/HAFAS/bin/query.exe/en

Shuttle Service:
Shuttle services will be available for IEW attendees from the Brussels Airport and the train station in Turnhout.
For shuttle information please visit http://www.esda.org/IEW_Travel_Accomodations.html

By Car:
It takes approximately 1 hour 20 minutes to travel from Brussels Airport to the Corsendonk Priory by rental car.
International ESD Workshop Registration Form  
May 14-17, 2012 Priory Corsendonk, Oud-Turnhout, Belgium

Workshop registration includes a room reservation and provided meals.

Attendee: ____________________________________________

Company: ____________________________________________

Address: ____________________________________________

City: ___________________________ State: _____________ Zip: _____________ Country: _____________

Phone: (____) _____________ E-mail: ____________________________ Fax: (____) _____________

Address is: (Please check one) □ home or □ office

Please check here if you do not wish to receive mail other than from ESDA: □ Check if, under the Americans with Disabilities Act, you require any auxiliary aids or services.

• Please List Your Guests: Adults (Name) ____________________________ Children – under 3 ___ 3-12 ___

Guests staying in the room of a registered attendee will be charged 30 Euro per night (90 Euro for a separate room) payable directly to the Hotel. Fee covers room and breakfast. Lunch and dinner will be available for purchase.

• Please indicate any special dietary needs.

Arrival: Date _________ Time _________  • Departure: Date _________ Time _________

Advanced Registration Fees                      Cost after March 27, 2012
ESDA or IEEE Member  $1,595                      ESDA or IEEE Member   $1,995
Non-ESDA or IEEE Member  $1,795                   Non-ESDA or IEEE Member   $1,995

The registration fee includes full workshop attendance and handout materials, seminar attendance, three nights’ lodging (Mon-Wed), nine meals (dinner Monday through lunch Thursday), as well as morning and afternoon snacks and drinks.

Students wishing to apply for reduced registration visit http://esda.org/IEW_registration.html. Application deadline: March 27, 2012

Cancellation & refund requests will be honored if received in writing no later than March 27th 2012, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Register Online at http://esda.org/onlineregistrations.html

Method of Payment

☐ Check Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve will be accepted.

Credit Card (check one) □ AMEX® □ Visa® □ MasterCard® □ Discover®

Card Number: ________________________________

Exp. Date: ____________________________ Security Code: _____________

Name on Card: ____________________________ Signature: ____________________________

Discussion Groups

I am interested in the following discussion group(s)

☐ DG A.1          ☐ DG B.1
☐ DG A.2          ☐ DG B.2
☐ DG A.3          ☐ DG B.3
☐ DG A.4          ☐ DG B.4

Special Interest Groups

I am interested in the following special interest group(s):

☐ SIG A.1          ☐ SIG B.1
☐ SIG A.2          ☐ SIG B.2
☐ SIG A.3          ☐ SIG B.3

Posters

Will you be bringing a poster to the open poster session? ☐ Yes ☐ No

If yes, what is the title of your poster? ____________________________

Special Interest Groups

Would you like to form a new SIG? ☐ Yes ☐ No

If yes, what is the proposed topic for your group? ____________________________

Send this completed form and payment to:
ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069
Phone: 315-339-6937 ▲ Fax 315-339-6793 ▲ info@esda.org ▲ www.esda.org
ESD ASSOCIATION SEMINAR
MAY 11, 2012 • 9:00 AM - 6:00 PM (9:00 – 18:00)
On-Chip ESD Protection Design Overview and Practical Examples
Imec, Kapeldreef 75 B-3001, Heverlee, Belgium
Lunch and refreshments provided
Register online at www.esda.org

Instructors: Charvaka Duvvury, Texas Instruments; James W. Miller, Freescale Semiconductor

Objective: The course objective is to give an overview about the importance of ESD to the electronics industry; review the protection design techniques based on device understanding and circuit performance impact, define options for protection designs, provide simulation methods, and summarize the state-of-the-art technology trends and the challenges for maintaining ESD reliability. Part I will establish the fundamental ESD aspects followed by an overview of ESD design techniques and device effects leading to the latest technologies. Part II will address more practical design methods with a focus on active rail clamp based ESD protection.

Cost on or before 3/27/12 | Cost after 3/27/12
--- | ---
Members | Non-Members | Members | Non-Members
$750 | $850 | $950 | $950

Cosponsored by imec http://www.imec.be/

2012 IEW
International Electrostatic Discharge Workshop
May 14-17, 2012
Priory Corsendonk, Oud-Turnhout, Belgium

2012 IEW Highlights
Five in-depth Seminars by Industry Leading Experts
- Electrical Overstress (EOS) of Automotive Semiconductors
- EOS / ESD Related Product Failure Analysis
- ESD Protection in FinFET Technologies
- ESD Design in High Voltage Technologies
- Bridging the Gap Between IC Design and its Application

Keynote Presentation
Game Changing Technologies in Health Care

Invited Talks
- Advancing CMOS Beyond the Si Roadmap: Chronicle of a (R)evolution Foretold
- Smart Power Technology on SOI
- ESDA Advanced Topic Ad-hoc Working Group on Electrical Overstress (EOS)
- System Level EMC/ESD Design – Challenges and Opportunities

Eighteen Technical Presentations and Posters
Eight Discussion Groups (DG)
Six Special Interest Group (SIG) Meetings

Register early for discounted prices!