SEARCH and RETRIEVAL INDEX

to

EOS/ESD SYMPOSIUM
PROCEEDINGS
1979 to 2014

(A GUIDE TO THE KNOWLEDGE BASE OF THE
EOS/ESD SYMPOSIUM PROCEEDINGS)

Published by
ESD ASSOCIATION
TABLE OF CONTENTS

INTRODUCTION

SECTION 1: AUTHOR INDEX

SECTION 2: PAPER AWARDS

SECTION 3: CHRONOLOGICAL CITATIONS OF PAPERS
Web link to ESD Association Home page

http://www.esda.org
INTRODUCTION

The EOS/ESD Symposium annual proceedings are a major source of information on electrostatic discharge. The proceedings also cover electrical overstress in general and, to a lesser extent, EMI. The first symposium was held in 1979 in Denver, Colorado. It was sponsored by ITT Research Institute and managed by a Steering Committee of individuals from industry and government organizations interested in EOS/ESD. The Symposium has been held every year since 1979. In 1983 the EOS/ESD Association became a cosponsor with IITRI until 1989.

Starting in 1990 the EOS/ESD Symposium became sponsored by the EOS/ESD Association in cooperation with the IEEE Electron Devices Society.

The EOS/ESD Association in 1994 expanded its area of interest to non-electronic concerns of ESD and started to be known as the ESD Association. The symposium started to publish a few papers from other fields.

Paper number references for this index consist of 5 digit numbers. The first two digits are the proceeding’s year where the paper can be found. The last three digits are the proceedings page number on which the paper starts.

97298

proceeding’s year

starting page number

There are some workshop reports and summaries at the back of the proceedings. The workshop information was not included in this index.

Starting in 1991 the proceedings was handed out at the Symposium. This is discernible by the paper awards photographs, since the awards for 1989 appear in both the 1990 and 1991 proceedings. So before 1991, to look at award photos for papers given a certain year you looked in the next year’s proceedings. For the awards from 1990 on, you look in the second year’s proceedings after the paper was given.
AVAILABILITY

The proceedings are generally available from ESD Association Headquarters. (Some earlier years are no longer available.)

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<table>
<thead>
<tr>
<th>CATALOG NUMBER</th>
<th>YEAR HELD</th>
<th>RANGE OF PAPER NUMBERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EOS-1</td>
<td>1979</td>
<td>79001 – 79205</td>
</tr>
<tr>
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<td>1980</td>
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</tr>
<tr>
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<td>1981</td>
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</tr>
<tr>
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<td>82001 – 82190</td>
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<tr>
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<td>1983</td>
<td>83001 – 83198</td>
</tr>
<tr>
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<td>1984</td>
<td>84001 – 84202</td>
</tr>
<tr>
<td>EOS-7</td>
<td>1985</td>
<td>85001 – 85175</td>
</tr>
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<td>EOS-8</td>
<td>1986</td>
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<tr>
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<td>1987</td>
<td>87001 – 87280</td>
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<td>88001 – 88228</td>
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<tr>
<td>EOS-11</td>
<td>1989</td>
<td>89001 – 89190</td>
</tr>
<tr>
<td>EOS-12</td>
<td>1990</td>
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<td>EOS-13</td>
<td>1991</td>
<td>91001 – 91224</td>
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<td>EOS-14</td>
<td>1992</td>
<td>92001 – 92277</td>
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<td>EOS-15</td>
<td>1993</td>
<td>93001 – 93251</td>
</tr>
<tr>
<td>EOS-16</td>
<td>1994</td>
<td>94001 – 94324</td>
</tr>
<tr>
<td>EOS-17</td>
<td>1995</td>
<td>95001 – 95338</td>
</tr>
<tr>
<td>EOS-18</td>
<td>1996</td>
<td>96001 – 96365</td>
</tr>
<tr>
<td>EOS-19</td>
<td>1997</td>
<td>97001 – 97412</td>
</tr>
<tr>
<td>EOS-20</td>
<td>1998</td>
<td>98001 – 98375</td>
</tr>
<tr>
<td>EOS-21</td>
<td>1999</td>
<td>99001 – 99391</td>
</tr>
<tr>
<td>EOS-22</td>
<td>2000</td>
<td>2000001 – 2000505</td>
</tr>
<tr>
<td>EOS-23</td>
<td>2001</td>
<td>2001001 – 2001461</td>
</tr>
<tr>
<td>EOS-24</td>
<td>2002</td>
<td>2002001 – 2002387</td>
</tr>
<tr>
<td>EOS-25</td>
<td>2003</td>
<td>2003001 – 2003426</td>
</tr>
<tr>
<td>EOS-26</td>
<td>2004</td>
<td>2004001 – 2004384</td>
</tr>
<tr>
<td>EOS-27</td>
<td>2005</td>
<td>2005001 – 2005421</td>
</tr>
<tr>
<td>EOS-28</td>
<td>2006</td>
<td>2006001 – 2006353</td>
</tr>
<tr>
<td>EOS-29</td>
<td>2007</td>
<td>2007001 – 2007408</td>
</tr>
<tr>
<td>EOS-30</td>
<td>2008</td>
<td>2008001 – 2008332</td>
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<td>2009</td>
<td>2009001 – 2009419</td>
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<tr>
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<td>2010</td>
<td>2010001 – 2010473</td>
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<td>2011</td>
<td>2011001 – 2011395</td>
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<tr>
<td>EOS-34</td>
<td>2012</td>
<td>2012001 – 2012414</td>
</tr>
<tr>
<td>EOS-35</td>
<td>2013</td>
<td>2013001 – 2013397</td>
</tr>
<tr>
<td>EOS-36</td>
<td>2014</td>
<td>2014001 – 2013400</td>
</tr>
</tbody>
</table>
SECTION 1
AUTHOR INDEX
Abderhaiden, J.
90143 An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes

Abessolo-Bidzo, D.
2011163 Predictive CDM Simulation Approach Based on Tester, Package and Full Integrated Circuit Modeling
2013283 ESD Protection Circuit for a Sub-1 dB Noise Figure LNA in a SiGe:C BiCMOS Technology

Abou-Khalil, M.J.
2007028 Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology
2007385 Process and Design Optimization of a Protection Scheme Based on NMOSFETs with ESD Implant in 65nm and 45nm CMOS
2008228 Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies
2008304 Investigation of ESD Performance of Silicide-Blocked Stacked NMOSFETs in a 45nm Bulk CMOS Technology
2008312 ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology
2009334 Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line

Aburano, R.
2005178 Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices

Acevedo, M.
2001262 The Purity, Wetting, and Electrical Properties of Static-Dissipative Surfactant Coatings Versus Inherently-Dissipative Polymer Alloys

Adams, C.S.
87028 Thermoplastic Composites for ESD Protection

Adams, J.
2012191 Test Method Recommendations for the Evaluation of Packaging Materials Used for Small Static Sensitive Electronic Components

Adams, O.E.
81151 EOS/ESD Failure Threshold Analysis Errors, Their Source, Size and Control
82019 Limitations in Modeling Electrical Overstress Failure in Semiconductor Devices
88053 Photoemission Testing for ESD Failures Advantages and Limitations

Adkisson, J.W.
96101 Linewidth Control Effects on MOSFET ESD Robustness

Adriano, C.
2000060 Detecting ESD Events using a Loop Antenna

Adris, M-F
2012129 Implementing Air Ionizing Blower at KLA Tencor 2401 Metrology Tool Reduce Visual Inspection Failure for Semiconductor Wafers
Agneray, A.  
2003161. A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach

Aidam, M.  
95095. Calculation and Measurement of Transient Fields of Voluminous Objects  
95101. To What Extent Do Contact-Mode and Indirect ESD Test Methods Reproduce Reality?  
96203. Numerical Calculation of ESD

Ainsworth, G.F.  
88195. Hood Ionization in Semiconductor Wafer Processing: An Evaluation

Akers, M.D.  
2001082. Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies  
2003017. Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies

Akram, A.S.  
2008235. ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology

Akrout, Y.  
2009091. CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps

Alanzo, A.  
2000111. TLP Measurements for Verification of ESD Protection Device Response

Albano, T.  
99168. Test Methodologies for Detecting ESD Events in Automated Processing Equipment

Alexander, D.R.  
80059. Failure Threshold Distributions in Bipolar Transistors  
81114. Electrical Overstress Investigations in Modern Integrated Circuit Technologies

Alexander, P.H.  
97107. Fast Fourier Transform Analysis of Published ESD Waveforms and Narrowband Frequency Domain Measurement of Human ESD

Aliaj, B.  
2009204. 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses  
2010301. Study of Power Arrays in ESD Operation Regimes  
2014342. Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting

Allen, J.  
2001044. An Analysis of ESD Packaging Systems Through Thermoforming

Almazar, R.  
95118. Sporadic Effect of Leadscan Machine To CMOS ESD Low Yielding Lots  
96110. Immediate Elimination of Gross ESD Failures in PLCC MECL Product Line Through Innovative Techniques
Alvarez, D.

2005413 PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latchup Robustness
2007028 Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress
2007385 Process and Design Optimization of a Protection Scheme Based on NMOSFETs with ESD Implant in 65nm and 45nm CMOS
2008304 Investigation of ESD Performance of Silicide-Blocked Stacked NMOSFETs in a 45nm Bulk CMOS Technology
2013174 Optimized Netlist Checks – Full Chip ESD Verification
2013305 CDM Single Power Domain Failures in 90 nm

Alves, S.

2004174 ESD Induced Latent Defects in CMOS ICs and Reliability Impact

Amarnath, J.

2011230 Movement of Metallic Particles in a 3-Phase Common Enclosure Gas Insulated Substations

Amerasekera, A.

86208 ESD Pulse and Continuous Voltage Breakdown in MOS Capacitor Structures
90119 Standard ESD Testing of Integrated Circuits
90143 An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes
92265 An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies
94237 The Impact of Technology Scaling On ESD Robustness and Protection Circuit Design
95162 Advanced CMOS Protection Device Trigger Mechanisms During CDM
96285 EOS/ESD Analysis of High-Density Logic Chips
97230 Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes
98161 ESD-Related Process Effects in Mixed-Voltage Sub-0.5 µm Technologies
2001071 Modeling Substrate Diodes under Ultra High ESD Injection Conditions

Ames, S.

2002092 Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

Amoruso, V.

99335 An Improved Model of Man for ESD Applications

Amos, C.T.

85163 A Technique for Real Time Examination of Sub-System ESD/EOS Damage in Integrated Circuits
86219 A Study of EOS in Microcircuits Using the Infra-Red Microscope

Anaf, L.J.

93177 Selecting Materials for Protection Against ESD Using an ESD Shielding Effectiveness Meter
Anand, Y.
79097 Electrostatic Failure of X-Band Silicon Schottky Barrier Diodes
93103 Electrostatic Failure of GaAs Planar Doped Barrier Diodes
99160 Latent ESD Failures in Schottky Barrier Diodes
200037 Random GaAs IC’s ESD Failures Caused by RF Test Handler

Anderson Jr., W.T.
87205 Electrostatic Discharge Effects in GaAs FETs and MODFETS

Anderson, B.J.
91199 The Chemistry of Antistatic Additives

Anderson, J.W.
87036 Contaminated Antistatic Polyethylene

Anderson, R.E.
2001238 Human Body Model, Machine Model, and Charged Device Model ESD Testing of Surface Micromachined Microelectromechanical

Anderson, W.E.
81075 Selection of Packaging Materials for Electrostatic Discharge-Sensitive (ESDS) Items
83087 Permanence of the Antistatic Property of Commercial Antistatic Bags and Tote Boxes
84007 Hazards of Static Charges and Fields at the Work Station
85111 Perforated Foil Bags: Partial Transparency and Excellent ESD Protection
87041 Electrostatic Discharge (ESD) Control in an Automated Process
89023 Controlling Voltage on Personnel

Anderson, W.R
98054 ESD Protection for Mixed Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration
98086 Cross Reference ESD Protection for Power Supplies
99088 ESD Protection under Wire Bonding Pads
99212 A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies
2003059 ESD Protection Design Challenges for a High Pin-Count Alpha Microprocessor in a 0.13µm CMOS SOI Technology
2009101 Metal and Silicon Burnout Failures from CDM ESD Testing
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Ando, K.
92076 An Advanced ESD Test Method for Charged Device Model

Andreini, A.
2001102 Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology
2003088 Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2003328  A Traceable Method for the Arc-free Characterization and Modeling of CDM-Testers and Pulse Metrology Chains
2004107  Study of CDM Specific Effects for a Smart Power Input Protection Structure
2006032  Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies
2006274  Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
2007058  CDM Circuit Simulation of a HV Operational Amplifier Realized in 0.35μm Smart Power Technology
2008211  Novel 190V LIGBT-Based ESD Protection for 0.35μm Smart Power Technology Realized on SOI Substrate
2013105  Power-to-Failure Investigation for PNP-based ESD Protections: From ns to ms
2013164  HBM ESD EDA Check Method Applied to Complete Smart Power IC’s – Functional Initialization and Implementation

Andresen, B.

92234  A Successful HBM ESD Protection Circuit for Micron and Sub-Micron Level CMOS

Andrieu, F.

2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Angelopoulos, M.

94226  Electrically Conducting Polyanilines for Electrostatic Dissipation
95225  Cross-Linkable Conducting Polymer Coatings

Ansari, S.

2002382  Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD

Antinone, R.J.

80184  Microcircuit Electrical Overstress Tolerance Testing and Qualification

Antonevich, J.N.

83076  Measuring Effectiveness of Air Ionizers

Aoki, O.

2006152  Radiated ESD Noise of 5GHz-band from Walkers

Arbess, H.

2011045  High Temperature Operation MOS-IGBT Power Clamp for Improved ESD Protection in Smart Power SOI Technology
2013258  Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement

Argard, P.V.

87164  A New TTL-CMOS Input Buffer and an Inverter with Process Independent Threshold Voltage

Arifin, S.

2009055  Space Charge Balance Sensing for Static Control

Arimura, M.

2008174  Electrostatic Control System Using Ceramic Transformer
Armendariz, M.G.
80104 Surprising Patterns of CMOS Susceptibility to ESD and Implications on Long-Term Reliability

Armer, J.
2001001 Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling
2001022 GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes
2002010 High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
2003250 Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

Arnould, J-D.
2010021 A Novel Physical Model for the SCR ESD Protection Device
2011179 Scalable Modeling Studies on the SCR ESD Protection Device

Ash, M.S.
81242 Non-Linear Kinetics of Semiconductor Junction Thermal Failure
83122 Semiconductor Junction Non-Linear Failure Power Thresholds: Wunsch-Bell Revisited

Ashby, P.
90119 Standard ESD Testing of Integrated Circuits

Asheghi, M.
2004356 Comparison of Thermal Response of GMR Sensor Subjected to HBM and CDM Transients

Ashton, R.A.
99212 A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies
2001435 Characterization of a 0.16µm CMOS Technology using SEMATECH ESD Benchmarking Structures
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004153 Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps
2005141 Voltages Before and After Current in HBM Testers and Real HBM
2006325 Pre Pulse Voltage in the Human Body Model
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
2008021 Characterization of Off Chip ESD Protection Devices
2008040 VF-TLP Round Robin Study, Analysis and Results
2009188 FCDM Measurements of Small Devices
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2012060 HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform
2013268 Activities Towards a New Transient Latch-up Standard

Aslett, R.
93239 Designing On-Chip Power Supply Coupling Diodes for ESD Protection and Noise Immunity
94141 Core Clamps for Low Voltage Technologies
Assaderaghi, F.

96291 CMOS-ON-SOI ESD Protection Networks
97210 Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks
99105 Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips
200029 Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

Atwood, B.C

2007273 Effect of Large Device Capacitance on FICDM Peak Current

Autizi, E.

2008272 EOS/ESD Sensitivity of Functional RF-MEMS Switches

Averill, J.A.

86188 Design and Test Results for a Robust CMOS VLSI Input Protection Network

Avery, L.R.

83177 Using SCR's as Transient Protection Structures in Integrated Circuits
85001 IC Technology: Where it is Going and What it Means for the ESD Industry
86156 Study of Antistatically Coated Shipping Tubes Using Static Decay and Triboelectric Tests
87088 Charged Device Model Testing: Trying to Duplicate Reality
87186 ESD Protection Structures to Survive the Charged Device Model (CDM)
91120 Beyond MIL HBM Testing: How To Evaluate the Real Capability of Protection Structures
98301 Investigation into Socketed CDM (SDM) Tester Parasitics
2001001 Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling
2001022 GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes

Avlyanov, J.

99268 Processable ESD Control Materials Filled With Tunable Intrinsically Conductive Polymer Nanocomposites

Axelrad, V.

2005100 Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies

Axelrod, V.

2008030 HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike

Azaïs, F.

2003233 STMSCR: A New Multi-Finger SCR-Based Protection Structure Against ESD
2005053 Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology
2006166 Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection
2007165 Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain
2008067 A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients
Baba, S.
2004125  ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices

Backers, I.
2010167  On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8 kV Contact System Level

Bade, L.
2008076  Discrete ESD Protection Diode During a System Level Pulse: Comparison of Simulation With Measurements

Badenes, G.
97308   Influence of Well Profile and Gate Length on the ESD Performance of a Fully Silicided 0.25 um CMOS Technology

Baelde, W.
90119   Standard ESD Testing of Integrated Circuits

Bafleur, M.
2002281  Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN
2002348  Investigations for a Smart Power and Self-Protected Device Under ESD Stress Through Geometry and Design Considerations for
2004174  ESD Induced Latent Defects in CMOS ICs and Reliability Impact
2006069  Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology
2007304  Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester
2009165  Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
2009314  Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage
2010011  TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior
2011045  High Temperature Operation MOS-IGBT Power Clamp for Improved ESD Protection in Smart Power SOI Technology
2011241  Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection
2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
2011343  Investigating the Probability of Susceptibility Failure Within ESD System Level Consideration
2013258  Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement
2014053  Novel 3D Back--to--Back Diodes ESD Protection

Baghini, M.S.
2009221  IGBT Plugged in SCR Device for ESD Protection in Advanced CMOS Technology

Baglee, D.A.
85045   ESD Design Considerations for ULSI

Bai, W.
2011323  Machine Model Evaluation and Interconnect Effect Study for TMR HGA
Bailey, R.

98328 Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing

Baird, M.

2000465 Verify ESD: A Tool for Efficient Circuit Level ESD Simulations of Mixed-Signal ICs
2010151 Correlation between System Level and TLP Tests Applied to Stand-Alone ESD Protections and Commercial Products

Baker, L.

89175 A "Waffle" Layout Technique Strengthens the ESD Hardness of the NMOS Output Transistor

Baker, R.P.

80104 Surprising Patterns of CMOS Susceptibility to ESD and Implications on Long-Term Reliability

Bakulin, A.

2002062 Optimization of Input Protection Diode for High Speed Applications

Bala, W.

2003080 Transient Latch-up:Experimental Analysis and Device Simulation
2004299 Development Strategy for TLU-Robust Products

Balevsky, A.

2014359 Over-Voltage Protection Strategies for LED Based Light Source Systems and other Applications

Baliga, B.J.

93001 Smart Power Technology: An Elephantine Opportunity

Ball, A.

96241 Antistatic Masking Tapes for Solder Flux Reflow Processing of Printed Circuit Boards

Balmain, K.G.

95066 Spacecraft and Human Electrostatic Discharge: A Comparison of the Two Phenomena
95090 Human Hand/Metal ESD and Its Physical Simulation

Ban, T.

2011197 Capturing Real World ESD Stress with Event Detector

Bandy, W.

2012120 ESD Protection of MR Sensors Using a Dissipative Shunt

Banerjee, K.

2001191 Invited Paper: Interconnect Reliability Under ESD Conditions: Physics, Models, and Design Guidelines
2001355 Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF Applications
2009001 Prospects of Carbon Nanomaterials in VLSI for Interconnections and Energy Storage
2012304 ESD Characterization of Atomically-Thin Graphene
Barbato, M.

2010433 A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic

Bardy, S.

2001110 Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test

Bargstädt-Franke, S.

2003080 Transient Latch-up: Experimental Analysis and Device Simulation
2004067 From the ESD Robustness of Products to the System ESD Robustness
2004299 Development Strategy for TLU-Robust Products

Baril, L.

2002306 Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads I
2002315 Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads II
2003419 Effect of ESD Transients on Noise in GMR Recording Heads
2004001 Electromagnetic Field Induced Degradation of Magnetic Recording Heads in a GTEM Cell
2004352 Effects of ESD Transients on Noise in Tunneling Recording Heads

Barker, P

2012414 Characterizing Devices Using the IEC 61000-4-5 Surge Stress

Barnett, H.

99043 A Study of ESD Induced Lockups in a Semiconductor Photolithography Area

Barnum, J.R.

81229 Electrical Overstress Damage in Silicon Solar Cells
91026 Sandia's Severe Human-Body Electrostatic Discharge Tester (SSET)

Barrett, R.

2004141 Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

Barth, J.E.

96167 Charged Device Model (CDM) Metrology: Limitations and Problems
96211 Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics Toward Creating a More Repeatable Simulation or;
98029 Metrology and Methodology of System Level ESD Testing
98290 Characterization and Optimization of a Bipolar ESD – Device by Measurements and Simulations
98301 Investigation into Socketed CDM (SDM) Tester Parasitics
99178 Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
99203 Issues Concerning CDM ESD Verification Modules-The Need to Move to Alumina
2000072 The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation
2000085 TLP Calibration, Correlation, Standards, and New Techniques
2001453  Correlation Considerations: Real HBM to TLP and HBM Testers
2002155  Correlation Considerations II: Real HBM to HBM testers
2003179  Real HBM & MM - The dV/dt Threat
2003372  Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2005141  Voltages Before and After Current in HBM Testers and Real HBM
2006353  HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
2008040  VF-TLP Round Robin Study, Analysis and Results
2009286  Using VFTLP Data to Design for CDM Robustness
2012032  Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2012060  HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform
2013140  On-Chip System Level ESD Protection for Class G Audio Power Amplifiers

Baruah, A.

79126  An Electrothermal Model for Current Filamentation in Second Breakdown of Silicon-on Sapphire Diodes

Batchelder, J.S.

91038  Technique for Generating Contamination-Free Ionized Air Using Focused Laser Light

Bauduin, B.

94301  A Comparative Study of "Low Cost" 1.3 µm Laser Diodes: ESD Performance

Baum, K.

91151  Detection of ESD-Induced NonCatastrophic Damage in P-Channel Power MOSFETs

Baumann, C.

2010049  Triggering of Transient Latch-up (TLU) by System Level ESD

Baumgartner, G.

84025  Electrostatic Measurement for Process Control
84097  Testing of Electrostatic Materials Fed. Std. 101C, Method 4046.1
85124  ESD Analysis of Masking Tape Operations
87018  A Method to Improve Measurements of ESD Dissipative Materials
90097  Electrostatic Discharge Protective Bag Test - Analysis of EIA Standard 541
92009  The Misconceptions of Air Flow as a Tribocharging Source
95262  Electrostatic Decay Measurement Theory and Applications
96156  ESD Demonstrations to Increase Engineering & Manufacturing Awareness
97068  Analysis of ESD Glove Use
98224  EOS Analysis of Soldering Iron Tip Voltage
2001281  A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

Bayer, M.J.

2003017  Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
Baynes, C.C.
90151 Failure Analysis of Electrostatic Sensitive ECL Gate Arrays

Bazarian, A.
80044 Gas Tube Surge Arresters for Control of Transient Voltages

Beall, J.R.
83198 A Study of ESD Latent Defects in Semiconductors

Beamer, B.
91210 A New Permanent ESD and Corrosion Resistant Material

Beaudoin, F.
2004174 ESD Induced Latent Defects in CMOS ICs and Reliability Impact

Beckrich-Ros, H.
2008067 A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients
2008088 A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology
2010021 A Novel Physical Model for the SCR ESD Protection Device
2011179 Scalable Modeling Studies on the SCR ESD Protection Device
2012015 ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

Beebe, S.G.
96265 Methodology for Layout Design and Optimization of ESD Protection Transistors
98259 Simulation of Complete CMOS I/O Circuit Response to CDM Stress
2004248 ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure
2005421 SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies
2007185 Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI
2008235 ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2009101 Metal and Silicon Burnout Failures from CDM ESD Testing
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Belisle, D.
2002163 A New ESD Model: The Charged Strip Model

Bell, D.A.
2010097 Hierarchical Verification of Chip-Level ESD Design Rules

Bellen, R.
97240 Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 μm CMOS Technology

Bellev, P.
2000041 Optimizing The Performance of a Composite ESD Circuit Protection Device
2000111 TLP Measurements for Verification of ESD Protection Device Response
Bellmore, D.G.

2001141  Anodized Aluminum Alloys, Insulator or Not?
2002223  Controlling ESD in Automated Handling Equipment
2004200  CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2004219  Characterizing Automated Handling Equipment Using Discharge Current Measurements
2005195  Characterizing Automated Handling Equipment Using Discharge Current Measurements II
2006240  Trends in External Ionizer Monitoring and Control

Beloni, E.

2010325  ESD Stimulated Ignition of Metal Powders

Beltman, R.A.M.

90157    Simulation of Thermal Runaway During ESD Events
91098    Physics of Electro-Thermal Effects in ESD Protection Devices

Bendix, P.

2000456  Chip-Level Simulation for CDM Failures in Multi-Power ICs
2005100  Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies

Bennett, D.

2003372  Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004141  Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

Benoist, T.

2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration
2012015  ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

Berbeco, G.R.

80001    Passive Static Protection: Theory and Practice
82124    Characterization of ESD Safe Requirements for Floor Surfaces

Berkowitz, M.B.

89032    Modular ESD Certification Training Program
90027    ESD Controls in Hazardous High Voltage Environments

Berndt, H.

2001267  A Study of the Variables of Electrodes Used in the Measurement of Table and Floor Materials and How They Affect the Test Results

Bernett, M.K.

82115    Electroactive Polymers as Alternate ESD Protective Materials

Bernier, J.C.

94214    CDM Events in Automated Test Handlers and Environmental Testing - A Case History
95110    ESD Improvements for Familiar Automated Handlers
Die Level CDM Testing Duplicates Assembly Operation Failures

ESD Sources Pinpointed by Analysis of Radio Wave Emissions

Test Methodologies for Detecting ESD Events in Automated Processing Equipment

A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods

Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

Characterizing Automated Handling Equipment Using Discharge Current Measurements II

Berning, D.W.

Reverse-Bias Second Breakdown in Power Transistors

Berthet, F.

Electrical Overstress Robustness and Test Method for ICs

Bertonnaud, Stephane

IEC System Level ESD Challenges and Effective Protection Strategy for USB2 Interface

Bertrand, G.

Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN

Besse, P.

Investigations for a Smart Power and Self-Protected Device Under ESD Stress Through Geometry and Design Considerations for

Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology

Correlation between System Level and TLP Tests Applied to Stand-Alone ESD Protections and Commercial Products

ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver

Impact of Snapback Behavior on System Level ESD Performance with Single and Double Stack of Bipolar ESD Structures

Bhar, T.N.

Proposed MIL-STD and MIL-HDBK for an Electrostatic Discharge Control Program -- Background and Status

Bhatia, K.

Layout Guidelines for Optimized ESD Protection Diodes

A Kelvin Transmission Line Pulsing System with Optimized Oscilloscope Ranging

Biegel, M.G.

Charged Device Damage of PLCCs Inside an Antistatic Shipping Tube - A Case History

Biermann, G.

A Statistical Method for the Detection of Gate Oxide Breakdowns Due To Fast EOS Events, Such As ESD, On Power DIMOS Devices

Grounding Personnel via the Floor/Footwear System

Bigaouette, R.J.

Degraded Device Detection
Bilodeau, T.M.
88147  A Novel High Fidelity Technique to View In-Situ ESD Stress Voltage Waveforms
89043  Theoretical and Empirical Analyses of the Effects of Circuit Parasitics on the Calibration of HBM ESD
90131  The Electrostatic Discharge Sensitivity of GaAs MMIC Amplifiers

Bin, L.
98135  Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Bingold, B.
91144  Package Effects On Human Body and Charged Device ESD Tests

Birk, M.
97027  Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs

Black, E.P.
91015  Real Circuit Performance of ESD Protection Devices

Blackburn, D.L.
79116  Reverse-Bias Second Breakdown in Power Transistors

Blanc, D.
201305  Power-to-Failure Investigation for PNP-based ESD Protections: From ns to ms

Blanc, F.
2001110  Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test
2006077  ESD Protection for the High-Voltage CMOS Technologies
2007047  Designing HV Active Clamps for HBM Robustness
2008099  A Methodology for the ESD Test Reduction for Complex Devices

Blankenagel, J.
89050  A High Voltage Pulse Generator for ESD Simulation

Blankstein, S.
98124  Outgassing, Volatile Organic Content, and Contamination Content of Materials Used in Today’s Electronics Workplace

Blinde, D.R.
81009  Quantitative Effects of Relative & Absolute Humidity on ESD Generation/Suppression
83067  The Room Air Ionization System, a Better Alternative than 40% Relative Humidity

Blitshteyn, M.
83076  Measuring Effectiveness of Air Ionizers

Blore, R.A.
79041  Reliability of EOS Screened Gold Doped 4002 CMOS Devices

Bobde, M.
2008083  Potential Barrier Based Clamp: A New Device Structure For Low Voltage Triggering
<table>
<thead>
<tr>
<th>Author</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bock, K.H.</td>
<td>Improved ESD-Protection of GaAs-FET Microwave Devices by New Metallization Strategy</td>
</tr>
<tr>
<td></td>
<td>Fieldemitter-Based ESD-Protection Circuits for High Frequency Devices and IC’s</td>
</tr>
<tr>
<td></td>
<td>A Compact Model for the Grounded-Gate NMOS Behaviour Under CDM ESD Stress</td>
</tr>
<tr>
<td></td>
<td>ESD Issues in Compound Semiconductor High-Frequency Devices and Circuits</td>
</tr>
<tr>
<td></td>
<td>Influence of Well Profile and Gate Length on the ESD Performance of a Fully Silicided 0.25 um CMOS Technology</td>
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<tr>
<td></td>
<td>Non-Uniform Triggering of gg-nMOS Investigated by Combined Emission Microscopy and Transmission Line Testing</td>
</tr>
<tr>
<td></td>
<td>Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations</td>
</tr>
<tr>
<td></td>
<td>Investigation into Socketed CDM (SDM) Tester Parasitics</td>
</tr>
<tr>
<td></td>
<td>Influence of gate length on ESD-performance for deep sub micron CMOS technology</td>
</tr>
<tr>
<td></td>
<td>Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM</td>
</tr>
<tr>
<td>Boday, D</td>
<td>ESD Protection of MR Sensors Using a Dissipative Shunt</td>
</tr>
<tr>
<td>Boehm, D.</td>
<td>Magneto Optical Static Event Detector</td>
</tr>
<tr>
<td></td>
<td>Test Methodologies for Detecting ESD Events in Automated Processing Equipment</td>
</tr>
<tr>
<td></td>
<td>Advances in Magneto Optical Static Event Detector Technology</td>
</tr>
<tr>
<td>Bogani, A</td>
<td>HBM ESD EDA Check Method Applied to Complete Smart Power IC’s – Functional Initialization and Implementation</td>
</tr>
<tr>
<td>Bolasny, R.E.</td>
<td>Static Control Systems</td>
</tr>
<tr>
<td>Bonfert, D.</td>
<td>Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits</td>
</tr>
<tr>
<td>Bönisch, S.</td>
<td>Broadband Measurement of ESD Risetimes to Distinguish between Different Discharge Mechanisms</td>
</tr>
<tr>
<td>Bontekoe, F.</td>
<td>Standard ESD Testing of Integrated Circuits</td>
</tr>
<tr>
<td>Bookin, W.</td>
<td>ESD Damage and Solutions in Tape Head Manufacturing</td>
</tr>
<tr>
<td>Boone, W.</td>
<td>Evaluation of Cleanroom/ESD Garment Fabrics: Test methods and Results</td>
</tr>
<tr>
<td></td>
<td>Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing</td>
</tr>
<tr>
<td></td>
<td>Using HGA Antennas to Measure EMI; Establishing and Correlating Damage Thresholds of GMR Heads</td>
</tr>
<tr>
<td></td>
<td>A Study of Head Stack Assembly Sensitivity to ESD</td>
</tr>
</tbody>
</table>
2002326 Impact of Insulating “Conductive” Materials on Disk Drive ESD Robustness
2004008 Wire Bonding Tip Study for Extremely ESD Sensitive Devices

Bordeos, R.

2000184 A Case Study on Hidden ESD Events of GMR HGA Dynamic Test Fixture
2000485 Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach
2001175 A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)
2002147 Magnetoresistive Sensitivity Mapping (MSM) and Dynamic Electrical Test (DET) Correlation Study on GMR Sensor Induced by Low
2002321 The Practical Approach of ESD Control Solution in Headstack Assembly (HSA) Manufacturing

Bordoloi, B.K.

88113 Characterization of Corrosivity of Antistatic Packaging Materials

Borgmans, C.

93177 Selecting Materials for Protection Against ESD Using an ESD Shielding Effectiveness Meter

Borjesson, A.

95253 A Method for Measurement of Triboelectric Charging

Borlongan, M.A.

2007222 Preventing Arcing Damage on Radio Frequency Device Wafer by Controlling ESD Resistively Level of Water for Saw and Wash

Borremans, J.

2007242 T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology
2009352 A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS

Bos, P.

90119 Standard ESD Testing of Integrated Circuits

Bosch, W.

2013191 Powered System-Level Conductive TLP Probing Method for ESD/EMI Hard Fail and Soft Fail Threshold Evaluation

Boselli, G.

99011 Investigations on Double-Diffused MOS (DMOS) transistors under ESD zap conditions
2001071 Modeling Substrate Diodes under Ultra High ESD Injection Conditions
2002257 Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 μm ESD Protection Circuits
2003008 A MOSFET Power Supply Clamp with Feedback Enhanced Triggering for ESD Protection in Advanced CMOS Technologies
2004132 Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers
2004146 The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps
2005043 Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window
2005298 A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65nm CMOS Technologies
2010031 The Relevance of Long-Duration TLP Stress on System Level ESD Design
2010103 An Automated ESD Verification Tool for Analog Design
2010309 Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies
2011069 Novel Technologies to Modulate the Holding Voltage in High Voltage ESD Protections
2012373 A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting
2013133 Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications
2013292 The Very Unusual Case of the IEC-Robust IC with Low HBM Performance
2013383 Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components

Bossard, P.R.

80017 ESD Damage From Triboelectrically Charged IC Pins
81057 Evaluation of Integrated Circuit Shipping Tubes
83029 ESD by Static Induction
84040 A Room Ionization System for Electrostatic Charge and Dust Control
87214 Room Ionization: Can It Significantly Reduce Particle Contamination?

Bossche, M.V.

2009158 The Application of Large-Signal Calibration Techniques Yields Unprecedented Insight During TLP and ESD Testing

Botula, A.

2001326 Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit

Bouangeune, D.

2012396 Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Bouchard, S.

92039 ESD - A Problem Beyond the Discrete Component

Bourgeat, J.

2009314 Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage
2010011 TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior
2011082 β Matriz Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology
2013199 Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology

Bouyssou, E.

2011241 Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection

Boverie, B.

88173 Coupling of ESD-Generated EMP to Electronics
89145 Simulation of the EMP From ESD
Bowers, J.S.
83198  A Study of ESD Latent Defects in Semiconductors

Boxleitner, W.
90054  ESD Stress on PCB Mounted ICs Caused by Charged Boards and Personnel
93139  Coaxial Probe To Measure ESD Voltage Waveforms with One Nanosecond Risetimes

Bradford, J.
93201  ESD Packaging: An Environmental Perspective

Bradza, E.
97170  Grounding Personnel via the Floor/Footwear System

Branberg, G.A.
79055  Electro-Static Discharge and CMOS Logic

Brandt, M.T.
90255  A Proposed Test Methodology for Evaluating the ESD Control Characteristics of Floor Materials

Brankov, A.
2009396 Failure Detection With HMM Waveforms

Braude, R.
93035  Setting Up an Effective Corporate ESD Program

Bravaix, A.
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress

Brennan, C.J.
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors
2004166 ESD Design Automation for a 90nm ASIC Design System
2004182 CDM Failure Modes in a 130nm ASIC Technology
2005126 Design Automation to Suppress Cable Discharge Event (CDE) Induced Latchup in 90nm CMOS ASICs
2005380 Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90nm CMOS ASICs

Brennan, T.F.
83158  Invisible EOS/ESD Damage: How to Find it?

Bridgwood, M.A.
85084  Modeling the Effects of Narrow Impulsive Overstress on Capacitive Test Structures
86200  Breakdown Mechanisms in MOS Capacitors Following Electrical Overstress
88129  A Comparison of Threshold Damage Processes in Thick Field Oxide Protection Devices Following Square Pulse and Human Body

Briggs Jr., C.
79007  Electrostatic Conductivity Characteristics of Workbench-Top Surface Materials
Brin, R.A.
93041 You've Implemented an ESD Program - What's Next?
97188 ESD Program Auditing: The Auditor's Perspective

Brodbeck, J.
2004205 Humidity Effects on Laminated ESD Worksurface Resistance and Charge Dissipation Properties

Brodbeck, T.
98290 Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
98301 Investigation into Socketed CDM (SDM) Tester Parasitics
98320 Influence of the Device Package on the Results of CDM Tests – Consequences for Tester Characterization and Test Procedure
2000066 Influence of the Charging Effect on HBM ESD Device Testing
2004067 From the ESD Robustness of Products to the System ESD Robustness
2005178 Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices
2005184 Experience in HBM ESD Testing of High Pin Count Devices
2006136 Relations Between System Level ESD and (vf-) TLP
2006144 Cable Discharges into Communication Interfaces
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
2007001 CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress
2008106 Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests
2009419 Characterization and Simulation of Real-World Cable Discharge Events
2010049 Triggering of TransientLatch-up (TLU) by System Level ESD

Brodsky, J.S.
2003098 Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2010031 The Relevance of Long-Duration TLP Stress on System Level ESD Design
2010103 An Automated ESD Verification Tool for Analog Design
2010309 Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies
2011197 Capturing Real World ESD Stress with Event Detector
2013292 The Very Unusual Case of the IEC-Robust IC with Low HBM Performance
2014289 Identification of Two-Probe TLP Contact Resistance Issues and Proposed Solutions

Brooke, L.C.
86188 Design and Test Results for a Robust CMOS VLSI Input Protection Network

Brossier, J.
85100 A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models with
Bruin, P.

2003051  Transmission Line Pulsed Photo Emission Microscopy as an ESD Troubleshooting Method

Bruines, J.

90143   An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes
93117   Suppression of Soft Failures in a Submicron CMOS Process

Bryant, N.

2012186  Carbon Nanotube Based Thermoplastic Lightning Strike Isolators

Bucha, R.M.

2001262  The Purity, Wetting, and Electrical Properties of Static-Dissipative Surfactant Coatings Versus Inherently-Dissipative Polymer Alloys

Buden, B.N.

83056   Power Failure Modeling of Integrated Circuits

Budenstein, P.P.

79126   An Electrothermal Model for Current Filamentation in Second Breakdown of-Silicon-on Sapphire Diodes
80122   Effect of Junction Spikes and Doping Level on the Second Breakdown Susceptibility of Silicon-On-Sapphire Diodes

Buhler, C.

2005212  Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Bui, A.

97346   Unique ESD Failure Mechanisms During Negative to Vcc HBM Tests

Buj, C.

2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Bulach, S.

96193   Non-invasive Detection and Characterization of ESD Induced Phenomena in Electronic Systems

Burgess, K.

2010417  Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing
2011197  Capturing Real World ESD Stress with Event Detector
2011379  Two New Unexplained and Unresolved HBM Tester Related Failures

Burke, J.J.

90010   The Effect of Lightning on the Utility Distribution System

Burnett, E.S.

82131   ESD & Contamination from Clean Room Garments - Problems and Solutions

Burroughs, J.E.

82185   Electrostatic Discharge Immunity in Computer Systems

Bychikhin, S.

2002387  Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometery
2003116  Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness
2006274  Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
2009358  IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements
2011059  ESD Robust DeMOS Devices in Advanced CMOS Technologies
2011147  HBM ESD Robustness of GaN-on-Si Schottky Diodes

Cabayan, H.S.
    79198  Statistical Failure Analysis of Military Systems for High Altitude EMP

Cadjan, M.
    2013367  EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level

Caignet, F.
    2007304  Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester
    2010127  Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation
    2010137  Impact of the Power Supply on the ESD System Level Robustness
    2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
    2011343  Investigating the Probability of Susceptibility Failure Within ESD System Level Consideration
    2013155  20GHz On-Chip Measurement of ESD Waveform for System Level Analysis
    2014053  Novel 3D Back-to-Back Diodes ESD Protection

Caikang, S.
    98135  Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Caillard, B.
    2003233  STMSCR: A New Multi-Finger SCR-Based Protection Structure Against ESD

Calabrese, G.M.
    94315  Root Cause Analysis and Packaging Enhancements To Improve Processor ESD Susceptibility

Calcatera, M.C.
    79147  Microwave Nanosecond Pulse Burnout Properties of One Micron MESFETS

Calderbank, J.M.
    80012  The Effects of High Humidity Environments on Electrostatic Generation and Discharge

Calle, C.
    2005212  Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Calvin, H.
    80225  Measurement of Fast Transients and Application to Human ESD
    81001  A Closer Look at the Human ESD Event

Cambieri, J.
    2012298  ESD Induced Leakage Current Increase of Diffused Diodes
Camp, D.
2012402 A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 6100-4-2 Robustness Without on Board Suppressors

Campbell, D.S.
86208 ESD Pulse and Continuous Voltage Breakdown in MOS Capacitor Structures
90162 Experimental & Theoretical Studies of EOS/ESD Oxide Breakdown in Unprotected MOS Structures
92112 Parametric Drift in Electrostatically Damaged MOS Transistors

Campbell, R.W.
95218 Use of Static-Safe Polymers in Automated Handling Equipment

Campi, J.
2012319 Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers

Cao, J.
2013056 Design and Verification of a Novel Multi-RC-Triggered Power Clamp Circuit for On-Chip ESD Protection
2013248 Photon Accelerated Turn-on of High-Voltage ESD Diode Breakdown

Cao, S.
2008235 ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Cao, Y.
2008221 ESD Concept for High-Frequency Circuits
2010239 A TLP-Based Characterization Method for Transient Gate Biasing of MOS Devices in High-Voltage Technologies
2010283 On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD
2011187 ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology
2012353 Statically Triggered Active ESD Clamps for High-Voltage Applications
2014268 TLP Failure Level Extraction Despite Reflected Waves
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<td>A New ESD Model: The Charged Strip Model</td>
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<td>Basic Characteristics of the Field Assisted Air Ionizer</td>
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<td>PIN Photodetectors-The ESD Bottleneck in Laser Packages</td>
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<td>A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices</td>
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<td>Novel 190V LIGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate</td>
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<td>Calculation and Measurement of Transient Fields of Voluminous Objects</td>
<td>Djobava, R.</td>
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<td>2011076</td>
<td>When Good Trigger Circuits Go Bad: A Case History</td>
<td>Dobbin, A.</td>
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<td>2013313</td>
<td>Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps</td>
<td></td>
</tr>
</tbody>
</table>
Dobbs, B.

83021  Air Force Maintenance Program for Electrical Overstress/Electrostatic Discharge (EOS/ESD) Control

Dobson, J.

2012254  Sampling Pin Approaches for ESD Test Applications

Dodson, G.A.

79188  The Phantom Emitter - an ESD-Resistant Bipolar Transistor Design and its Applications to Linear Integrated Circuits

Dolby, D.

92136  ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Domanski, K.

2003080  Transient Latch-up: Experimental Analysis and Device Simulation
2004299  Development Strategy for TLU-Robust Products
2004322  Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
2005060  SCR Operation Mode of Diode Strings for ESD Protection
2005245  SoC-A Real Challenge for ESD Protection?
2007347  External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique
2010049  Triggering of Transient Latch-up (TLU) by System Level ESD
2012085  Topology-Aware ESD Checking: A New Approach to ESD Protection
2013268  Activities Towards a New Transient Latch-up Standard

Domengès, B.

2014393  Electrical Overstress Robustness and Test Method for ICs

Domingos, H.

79140  Square Pulse and RF Pulse Overstressing of UHF Transistors
80206  Basic Considerations in Electro-Thermal Overstress in Electronic Components
82169  Circuit Design for EOS/ESD Protection
85024  A Design Methodology for ESD Protection Networks
86173  Thick Oxide Device ESD Performance Under Process Variations
87265  Electrical Overstress in NMOS Silicided Devices
87280  Conduction Mechanisms in BJT's During Electrical Overstress
88070  Effect of Graded Collector Doping on Current Mode Second Breakdown in Bipolar Transistors
89072  Analysis of ESD Protection on Vendor Parts
89127  The Double Graded Transistor and its Beneficial Effect on Resistance to Current Mode Second Breakdown

Dong, L.

2003280  Flue Gas Cleaning Using Wet-Type Electrostatic Precipitator

Donner, J.C.

91059  Reducing Field Failure Rate with Improved EOS/ESD Design
Doucette, R.E.
85055 The Elimination of Electrostatic Discharge Failures From Silicon Gate Logic Technologies

Dournelle, S.
2003233 STMSCR: A New Multi-Finger SCR-Based Protection Structure Against ESD

Downing, M.H.
83006 ESD Control Implementation and Cost Avoidance Analysis

Dray, A.
2011082 β Matriz Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology
2012015 ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process
2013199 Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology

Dreibelbis, D.H.
83154 EOS or ESD: Can Failure Analysis Tell the Difference?

Dreizin, E.
2010325 ESD Stimulated Ignition of Metal Powders

Dreps, D.
2000029 Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

Drew, B.
2009091 CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps

Drüen, S.
2003122 High Abstraction Level Permutational ESD Concept Analysis
2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
2005245 SoC-A Real Challenge for ESD Protection?

Dubec, V.
2002387 Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometery
2006274 Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices

Dudek, V.
2003116 Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness

Dugan, M.P.
86182 Design and Characterization of Input Protection Networks for CMOS/SOS Applications

Duncan, W.
92175 Shrink Film Packaging Evaluation

Dundigal, S.
2010381 CDM Effect on a 65 nm SOC LNA
Dunn, C.
92136  ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Dunn, P.
2005126  Design Automation to Suppress Cable Discharge Event (CDE) Induced Latchup in 90nm CMOS ASICs

Dunniho, J.
2009396  Failure Detection With HMM Waveforms
2010145  Effects of TVS Integration on System Level ESD Robustness

Durgin, D.L.
80154  An Overview of the Sources and Effects of Electrical Overstress
81120  An Overview of Electrical Overstress Effects on Semiconductor Devices
82049  A Survey of EOS/ESD Data Sources

Dutton, R.W.
2001355  Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF Applications
2005033  RF ESD Protection Strategies: Codesign vs. Low-C Protection
2006317  A Frequency-Domain VFTLP Pulse Characterization Methodology and its Application to CDM ESD Modeling
2007102  Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System
2008235  ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2008258  Ultra-Fast Transmission Line Pulse Testing of Tunneling and Giant Magnetoresistive Recording Heads
2010203  Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Duvanaud, C.
98118  Electrostatic Discharges from Charged Particles Approaching a Grounded Surface

Duvvury, C.
83181  A Summary of Most Effective Electrostatic Discharge Protection Circuits for MOS Memories and their Observed Failure Modes
85045  ESD Design Considerations for ULSI
86173  Thick Oxide Device ESD Performance Under Process Variations
88053  Photoemission Testing for ESD Failures Advantages and Limitations
88201  A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes
88206  Output ESD Protection Techniques for Advanced CMOS Processes
89190  Input Protection Design for Overall Chip Reliability
91088  A Synthesis of ESD Input Protection Scheme
92088  Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices
93083  Studies of EOS Susceptibility in 0.6 mm nMOS ESD I/O Protection Structures
94237  The Impact of Technology Scaling On ESD Robustness and Protection Circuit Design
95162  Advanced CMOS Protection Device Trigger Mechanisms During CDM
96285 EOS/ESD Analysis of High-Density Logic Chips
97230 Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes
98104 A Simulation Study of HBM Failure in an Internal Clock Buffer and the Design Issues for Efficient Power Pin Protection Strategy
98208 An Automated Tool for Detecting ESD Design Errors
99212 A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies
2001012 5-V Tolerant Fail-Safe ESD Solutions for a 0.18µm Logic CMOS Process
2001192 Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology
2001445 Integration of TLP Analysis for ESD Troubleshooting
2002257 Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 µm ESD Protection Circuits
2004132 Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers
2004141 Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
2004146 The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps
2005043 Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window
2005280 ESD Evaluation of the Emerging MuGFET Technology
2005307 Problems with IO to all Other IOs ESD Stress Test: Two Case Studies
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2006222 High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies
2007283 CDM Peak Current Variations and Impact Upon CDM Performance Thresholds
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications
2008094 Single Pulse CDM Testing and its Relevance to IC Reliability
2008106 Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests
2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design
2009135 Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM
2009183 Influence of CDM Tester Plate Size on Discharge Current
2009322 Diode Isolation Concept for Low Voltage and High Voltage Protection Applications
2009377 Protecting Circuits From the Transient Voltage Suppressor's Residual Pulse During IEC 61000-4-2 Stress
2010065 SPICE Simulation Methodology for System Level ESD Design
2010075 TLP Characterization for Testing System Level ESD Performance
2010417 Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing
2011197 Capturing Real World ESD Stress with Event Detector
2011379 Two New Unexplained and Unresolved HBM Tester Related Failures
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Parametric Drift in Electrostatically Damaged MOS Transistors

Dyer, M.J.D.
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Test Procedures for Predicting Surface Voltages on Inhabited Garments

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Eaton, J.
Tribocharging of Materials Used In Tape Heads and Associated ESD Damage

Eberhardt, E.P.
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Edwards, H
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Egger, P.
Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model
Influence of Tester, Test Method and Device Type On CDM ESD Testing
Influence of Tester Parasitics On "Charged Device Model" Failure Thresholds
Does the ESD-Failure Current Obtained by Transmission Line Pulsing Always Correlate to Human Body Model Tests?

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Some Results in Measuring Static Decay

Eklof, P.
Studies and Revelation of Latent ESD-Failures

Elder, R.A.
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Ellis, D.
Transient Safe Operating Area (TSOA) Definition for ESD Applications
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Ellis, E.B.
Electrostatic Discharge at the Product Level
Enders, J.
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Eng, D.C.
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Englisch, A.
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Enlow, E.W.
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Enoch, D.R.
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83185 ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics
84165 Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
85132 An Experimental Investigation of ESD-Induced Damage to Integrated Circuits on Printed Circuit Boards
86224 An Experimental Validation of the Field-Induced ESD Model

Enokizono, M.
2010273 Neutralizing Current Sensor for AC Corona Ionizer

Entringer, C.
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2006166 Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection
2009314 Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage
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Eppes, D.
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Ershov, M.
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2010301 Study of Power Arrays in ESD Operation Regimes
2013367 EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level

Esmark, K.
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2000420 Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase
2001205 Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13µm CMOS Logic
2001216 Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric
Thermal Mapping

2002073 Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies

2002387 Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry

2003080 Transient Latch-up: Experimental Analysis and Device Simulation

2003088 Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress

2003122 High Abstraction Level Permutational ESD Concept Analysis

2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations

2005060 SCR Operation Mode of Diode Strings for ESD Protection

2005245 SoC-A Real Challenge for ESD Protection?

2006214 Tunable Bipolar Transistor for ESD Protection of HV CMOS Applications

2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain

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2007028 Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology

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2007347 External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique

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Etherton, M.

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2004107 Study of CDM Specific Effects for a Smart Power Input Protection Structure

2005080 Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit

2006186 Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology

2008030 HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike

2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

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Euker, R.

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Eun Kim, J.

2008191 Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer

Euzent, B.L.

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Exstrand, C.

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Mechanical and Electrical Properties of Poly (ether ether ketone) (PEEK) with Various Conductive Fillers

Fahey, T.

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Advancements in Inherently Dissipative Polymer (IDP) Alloys Provide New Levels of Clean, Consistent ESD Protection

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ESD Protection Circuit Schemes for DDR3 DQ Drivers

Fang, Q.

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Farbiz, F.

Analytical Modeling of External Latchup
Novel Technologies to Modulate the Holding Voltage in High Voltage ESD Protections
Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications
Multi-Reflection TLP: A New Measurement Technique for System-Level Automotive ESD/EMC Characterization

Farris, M.

Recommendations to Further Improvements of HBM ESD Component Level Test Specifications
Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results

Farwell, W.

EOS from Soldering Irons Connected to Faulty 120VAC Receptacles

Fattori, F.

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Faust, A.C.

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Faynot, O.

Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Feasey, P.R.

A Failure Analysis Methodology for Revealing ESD Damage to Integrated Circuits
Deficiencies in ESD Testing Methodology Highlighted by Failure Analysis
Feddeler

2013214 An Active MOSFET Rail Clamp Network for Component and System Level Protection

Feeney, M.D.

91158 Mechanically Relay Induced EOS From Wire Bonding Machines

Fehrenbach, D.M.

92019 An Evaluation of Air Ionizers for Static Charge Reduction and Particle Emission

Feilchenfeld, N.

2004361 Electrostatic Discharge (ESD) Protection of Giant Magneto-resistive (GMR) Recording Heads with a Silicon Germanium Technology

Feinberg, A.

2000387 Random GaAs IC’s ESD Failures Caused by RF Test Handler

Feinberg, Y

2013367 EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level

Felder, G.

2006240 Trends in External Ionizer Monitoring and Control

Felt, F.S.

83095 Coplanar Triboelectrification of Selected Materials

Fenouillet-Beranger, C.

2010185 Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

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Ferguson, R.E.

88033 Resolving ESD Incidents in Spacecraft Production Systems

Ferrari, P.

2010021 A Novel Physical Model for the SCR ESD Protection Device

2011179 Scalable Modeling Studies on the SCR ESD Protection Device

Ferru, G.

2014053 Novel 3D Back-to-Back Diodes ESD Protection

Fichtner, W.

95205 Layout Optimization of an ESD-Protection N-MOSFET By Simulation and Measurement

98290 Characterization and Optimization of a Bipolar ESD – Device by Measurements and Simulations

99001 Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions

2000420 Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase

2000446 ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior

2004107 Study of CDM Specific Effects for a Smart Power Input Protection Structure

2005060 SCR Operation Mode of Diode Strings for ESD Protection
<table>
<thead>
<tr>
<th>No</th>
<th>Title</th>
<th>Authors</th>
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<tbody>
<tr>
<td>2005080</td>
<td>Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit</td>
<td>Finkelshtein, J.</td>
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<td>98139</td>
<td>Electrostatic Hazards of Explosive, Propellant and Pyrotechnic Powders</td>
<td>Fish, A</td>
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<tr>
<td>2012402</td>
<td>A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 6100-4-2 Robustness Without on Board Suppressors</td>
<td>Fisher, R.J.</td>
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<td>89055</td>
<td>A Severe Human ESD Model for Safety and High Reliability System Qualification Testing</td>
<td>Fishman, A.</td>
</tr>
<tr>
<td>98328</td>
<td>Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing</td>
<td>Flatley, M.W.</td>
</tr>
<tr>
<td>96193</td>
<td>Non-invasive Detection and Characterization of ESD Induced Phenomena in Electronic Systems</td>
<td>Flatresse, P.</td>
</tr>
<tr>
<td>2005053</td>
<td>Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology</td>
<td>Fledderman, C.B.</td>
</tr>
<tr>
<td>2006166</td>
<td>Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection</td>
<td>Fledderman, C.B.</td>
</tr>
<tr>
<td>87252</td>
<td>The Effects of High Electric Field Transients on Thin Gate Oxide MOSFETs</td>
<td>Fong, Y.</td>
</tr>
<tr>
<td>2009292</td>
<td>A DRC-Based Check Tool for ESD Layout Verification</td>
<td>Fleurimont, J.</td>
</tr>
<tr>
<td>2007165</td>
<td>Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>2008067</td>
<td>A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>2008088</td>
<td>A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>2009314</td>
<td>Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>2010021</td>
<td>A Novel Physical Model for the SCR ESD Protection Device</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
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<td>Scalable Modeling Studies on the SCR ESD Protection Device</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>2012015</td>
<td>ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process</td>
<td>Fonteneau, P.</td>
</tr>
<tr>
<td>89084</td>
<td>Electrostatic-Discharge Detectors</td>
<td>Fordemwalt, J.N.</td>
</tr>
<tr>
<td>99043</td>
<td>A Study of ESD Induced Lockups in a Semiconductor Photolithography Area</td>
<td>Ford-Smith, R.</td>
</tr>
<tr>
<td>79158</td>
<td>Damage Response of Selected Interface Integrated Circuits to a Simulated EMP Waveform</td>
<td>Formanek, V.C.</td>
</tr>
</tbody>
</table>
Forster, G.
84136 Protection of Components Against Electrical Overstress (EOS) and Transients in Monitors

Foss, C.
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Foucher, B.
2001110 Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test

Fowler, S.L.
88103 Triboelectricity and Surface Resistivity do not Correlate
89007 Surface Resistivity and Static Decay Do Not Correlate
92027 Static Phenomena and Test Methods for Static Controlled Floors
97033 Procedures for the Design, Analysis and Auditing of Static Control Flooring/Footwear Systems

Fowler, W.
99088 ESD Protection under Wire Bonding Pads

Fragnoli, M
2013164 HBM ESD EDA Check Method Applied to Complete Smart Power IC’s – Functional Initialization and Implementation

Franey, J.P.
91210 A New Permanent ESD and Corrosion Resistant Material
94042 Field-Induced ESD From CRTs: Its Cause and Cure
2000375 Corrosion Induced Electrostatic Damage

Frank, D.E.
81021 The Perfect '10' - Can You Really Have One?

Frank, M.
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Freeman, P.S.
91216 Sources of Error in Resistance Measurements On Conductive Flooring

Frei, S.
97099 An Analysis of the Fields on the Horizontal Coupling Plane in ESD Testing
97117 About the Different Methods of Observing ESD
2010283 On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD
2011187 ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology
2014368 Analysis of ESD-Robustness of Multi-Layer Ceramic Capacitors in System Applications ESD German Forum Invited Paper

Freund, R.S.
91210 A New Permanent ESD and Corrosion Resistant Material
Fricke, K.
90193  Improved ESD-Protection of GaAs-FET Microwave Devices by New Metallization Strategy

Fromm, L.J.
97033  Procedures for the Design, Analysis and Auditing of Static Control Flooring/Footwear Systems
99145  A Study of ESD Corrugated
2003271 Using Electrostatic Discharge Test Method for Full Characterization of Dissipative and Conductive Materials

Fu, K.
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Fu, Y.
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Fujibayashi, K.
87227  Electromagnetic Wave Generation From Electrostatic Discharge Between Charged Human's Body and Earthed Electrode

Fujie, A.
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Fujikawa, H.
2011338 Characteristic of Radiated Electromagnetic Wave by ON/OFF Discharge on Sub-Micron Gap

Fujisawa, S.
2010369 Anomalous ESD Failures in MLDMOS during Reverse Recovery
2011053 Source Engineering for ESD Robust NLDMOS

Fukasaku, K.
2011088 Origin of It2 Drop Depending on Process and Layout with Fully Silicided ggMOS

Fukuda, K.
2004125 ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices

Fukuda, Y.
86193  ESD Protection Network Evaluation by HBM and CDM (Charged Package Method)
88228  VLSI ESD Phenomenon and Protection
96076  ESD and Latch Up Phenomena on Advanced Technology LSI
2001419 Invited Paper: ESD Evaluation by TLP Method on Advanced Semiconductor Devices
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Fung, R
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Fuqua, N.B.
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An ESD Expert System

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- Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric Thermal Mapping

Furkay, S.S.

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- Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors

Furusawa, K.

- Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group
- Study for Recovery Process of Damaged Al2O3 during Ion Milling to Increase Tolerance to ESD

Gaertner, R.

- Testing ESD Shielding Bags with an improved Bag Tester According to EIA-541
- Grounding Personnel via the Floor/Footwear System
- An Effective ESD Protection System in the Back End (BE) Semiconductor Manufacturing Facility
- From the ESD Robustness of Products to the System ESD Robustness
- Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices
- Experience in HBM ESD Testing of High Pin Count Devices
- An Alternative Method to Verify The Quality of Equipment Grounding
- Cable Discharges into Communication Interfaces
- Is CO2 Bubbling (Carbonization) a Requirement at Semiconductor Wafer Sawing Process
- HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
- Do We Expect ESD-failures in an EPA Designed According to International Standards? The need for a Process-Related Risk Analysis
- ESD Concerns in Sawing Wafers with Discrete Semiconductor Devices
- Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests
- Experiences with an Alternative Method for Grounding Personnel During Sitting Operation
- Automatic Handling Equipment - The Role of Equipment Maker on ESD Protection
- Characterization and Simulation of Real-World Cable Discharge Events
- ESD Protection Program at Electronics Industry - Areas for Improvement
- The Impact of Electrical Overstress on the Design, Handling, and Application of Integrated Circuits
- Is There Correlation Between ESD Qualification Values and the Voltages Measured in the Field?
- Poor Grounding – Major Contributor to EOS
- Sampling Pin Approaches for ESD Test Applications
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<th>Date</th>
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<td>Semiconductor Back End Manufacturing Process – ESD Capability Analysis</td>
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<td>On the Characterization of ESD Properties of JEDEC Trays</td>
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<td>An Effective ESD Program Management Based on S20.20 Plus ESD Capability/Risk Analysis</td>
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<td>Do Devices on PCBs Really See a Higher CDM-like ESD Risk?</td>
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**Gagnon, P.**

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<td>Creating and Measuring Photomask Damage</td>
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**Gajewski, A.**

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**Gale, E.**

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<td>A Study of ESD Protection Means of Cabled GMR Sensors</td>
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<td>Using VFTLP Data to Design for CDM Robustness</td>
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<td>HBM ESD Robustness of GaN-on-Si Schottky Diodes</td>
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<td>Misocorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester</td>
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<td>ESD Effects on the Radiation Response of Power VDMOS Transistors</td>
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<td>Detection of ESD-Induced NonCatastrophic Damage in P-Channel Power MOSFETs</td>
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<td>Annealing of ESD-induced Damage in Power MOSFETs</td>
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**Galy, P.**

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<td>Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection</td>
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<td>Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration</td>
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<td>ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process</td>
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<td>Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology</td>
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<td>86075</td>
<td>Latent Failures Due to Electrostatic Discharge in CMOS Integrated Circuits</td>
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<th>Date</th>
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2012254  Sampling Pin Approaches for ESD Test Applications
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2008148 Process Capability & Transitional Analysis

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2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices During HBM ESD Stress
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness
2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design
2009152 Calibration of Very Fast TLP Transients
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2008132 Delivering IEC 61000-4-2 Current Pulses Through Transmission Lines at 100 and 330 Ohm System Impedances

2009125 Two-Pin Human Body Model Testing

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<table>
<thead>
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<th>Year</th>
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<thead>
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<th>Paper Title</th>
</tr>
</thead>
<tbody>
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</tr>
<tr>
<td>Hao, J.</td>
<td>Engineering Fully Silicided Large MOSFET Driver for Maximum It1 Performance</td>
</tr>
<tr>
<td>Harame, D.</td>
<td>Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors</td>
</tr>
<tr>
<td>Hardwick, N.</td>
<td>Advancements in Inherently Dissipative Polymer (IDP) Alloys Provide New Levels of Clean, Consistent ESD Protection</td>
</tr>
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<td>Harford, J.R.</td>
<td>Powerline Disturbances - A Primer</td>
</tr>
<tr>
<td>Harris, C.C.</td>
<td>Input Structure Evaluation Using Specifically Designed Test Structures</td>
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<td>Harris, J.</td>
<td>Optimizing The Performance of a Composite ESD Circuit Protection Device</td>
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<td>TLP Measurements for Verification of ESD Protection Device Response</td>
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<td>Comparison of Solutions to Minimize Voltages Induced by ESD Events on Adjacent Microstrips</td>
</tr>
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<td>Capturing Real World ESD Stress with Event Detector</td>
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<td>Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature</td>
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<td>LSI Design Considerations for ESD Protection Structures Related to Process and Layout Variations</td>
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<td>Triboelectric Characterization of Packaging Materials</td>
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<td>Sheet Resistance Measurement of Buried Shielding Layers</td>
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2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
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An Investigation of Input Protection for CDM Robustness in 40 nm CMOS Technology

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Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
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Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model

Havens, M.R.

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Inherently Static Dissipative Packaging Films

Havermann, R.L.

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Helali, M.

An Improved Model of Man for ESD Applications

Helling, K.H.

ESD Protection Measures Return on Investment Calculation and Case Study
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Henderson, K.

<table>
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Jo, C.

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Johari, P.

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<table>
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Kelly, M.A.
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99178  Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
99203  Issues Concerning CDM ESD Verification Modules-The Need to Move to Alumina
200072  The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation
2002155  Correlation Considerations II: Real HBM to HBM testers
2003179  Real HBM & MM - The dV/dt Threat
2006353  HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
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90231  The Versatility of Electron Beam Processing, and the Conversion of Medium and High Performance Polymeric Films for ESD Protection
Keppens, B.
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2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design
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2005372  SCR Based ESD Protection in Nanometer SOI Technologies
2005393  Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies Avoiding Competitive
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2001032 ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device
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2003204 ESD Protection Design for Giga-Hz RF CMOS LNA with Novel Impedance-Isolation Technique
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2004160 Latchup Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product
2004265 Design on Latchup-Free Power-Rail ESD Clamp Circuit in High-Voltage CMOS ICs
2005118 ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process
2005262 Dependences of Damping Frequency and Damping Factor of Bi-Polar Trigger Waveforms on Transient-Induced Latchup
2005262 Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup Under System-Level ESD Test
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<td>The ARC Problem and Voltage Scaling in ESD Human Body Model</td>
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<td>Model of Leakage Current in LDD Output MOSFET Due to Low-Level ESD Stress</td>
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<td>An Active ESD Protection Technique for the Power Domain Boundary in a Deep Submicron IC</td>
<td>Kitayama, T.</td>
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<td>Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation</td>
<td>Kitlas, K.C.</td>
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<td>Electrostatic Discharge (ESD) Response Measurements in a Satellite Environment</td>
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<td>Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junctions</td>
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<td>EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level</td>
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<td>Performance-Oriented Design and Test Procedures for Static Control Footwear</td>
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PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latchup Robustness

Design and Characterization of a Multi-RC-Triggered MOSFET-based Power Clamp for On-Chip ESD Protection

Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology

Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies

Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies

Investigation of ESD Performance of Silicide-Blocked Stacked NMOSFETs in a 45nm Bulk CMOS Technology

ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology

Technology Scaling of Advanced Bulk CMOS On-Chip ESD Protection

ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology

Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line

An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies

Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation

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Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies

Technology Scaling Effects on the ESD Performance of Silicide-Blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies

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Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers

Investigation of SOI SCR Triggering and Current Sustaining under DC and TLP Conditions

Maximizing ESD Robustness of Current-Mode-Logic (CML) Driver with Internal Gate Bias Network

Junction Engineering for Soi Scr Triggering and Performance Improvement

ESD Device Performance Analysis in a 14nm FinFET Soi Cmos Technology: Fin-based versus Planar-based

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Li, Y-S.
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2012076 ESD Dynamic Methodology for Diagnosis and Predictive Simulation of HBM/CDM Events

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Liang, Y-C.
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Lianzhu, Z.
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Liao, W-M
2014304 Metal Routing Induced Burn Out in GGNMOS ESD Protection for Low-Power DRAM Application

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Liauh, H.
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Lidor, G.
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99251 Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing
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Lim, C-B
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Lim, S-H
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Lin, C-Y
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Lin, D.L.

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88162  A Microwave-Bandwidth Waveform Monitor for Charged-Device Model Simulators
89059  A Field-induced Charged-Device Model Simulator
90061  ESD Stressing of Simulated Circuit Packs
90114  A Comparison of ESD Failure Thresholds of CMOS I/O Buffers Using Real Human Body and Human Body Model Simulators
92068  From Lightning to Charged-Device Model Electrostatic Discharges
93073  ESD Sensitivity and VLSI Technology Trends: Thermal Breakdown and Dielectric Breakdown
94279  Off-Chip Protection: Shunting of ESD Current By Metal Fingers On Integrated Circuits and Printed Circuit Boards
95175  A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices
96040  Recommendations to Further Improvements of HBM ESD Component Level Test Specifications
97088  A Robust ESD Event Locator System With Event Characterization
98029  Metrology and Methodology of System Level ESD Testing

Lin, I.C.

2004160  Latchup Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

Lin, J-P

2014304  Metal Routing Induced Burn Out in GGNMOS ESD Protection for Low-Power DRAM Application

Lin, K.H.

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Lin, KS

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Lin, L.

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Lin, S.T.

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Lindholm, A.W.  
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Lindorfer, P.  
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2010301 Study of Power Arrays in ESD Operation Regimes  

Lingousky, J.E.  
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Linke, R.C.  
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Linten, D.  
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2007158 Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions  
2007242 T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology  
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications  
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2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors  
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CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS

A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS

Self-Protection Capability of Power Arrays

Center Balanced Distributed ESD Protection for 1-110 GHz Distributed Amplifier in 45 nm CMOS Technology

On-Wafer Human Metal Model Measurements for System-Level ESD Analysis

SCCF-System to Component Level Correlation Factor

Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays

HBM Parameter Extraction and Transient Safe Operating Area

Behavior of RF MEMS Switches under ESD Stress

On Gated Diodes for ESD Protection in Bulk FinFET CMOS Technology

CDM Protection for Millimeter-Wave Circuits

A SCR-Based ESD Protection for MEMS-Merits and Challenges

HBM ESD Robustness of GaN-on-Si Schottky Diodes

ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling

ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits

Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester

Mixed-Mode Simulations for Power-on ESD Analysis

Exploring ESD Challenges in Sub-20-nm Bulk FinFET CMOS Technology Nodes

ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices

Impact of the On-Chip and Off-Chip ESD Protection Network on Transient-Induced Latch-up in CMOS IC

CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus

Anti-Series Ggnmos ESD Clamp for Space Application IC’s

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Liong, C.T.

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Liou, J.

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Transient Safe Operating Area (TSOA) Definition for ESD Applications

2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses

A New ESD Design Methodology for High Voltage DMOS Applications

Study of Power Arrays in ESD Operation Regimes

A New Method to Evaluate Effectiveness of CDM ESD Protection
2014342  Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting

Lipka, K.M.

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Lisenker, B.

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2002373  Process Influence on Product CDM ESD Sensitivity

Lisiak, K.P.

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Littau, W.R.

81192  Prediction of Thin-Film Resistor Burnout

Litzenberger, M.

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2002387  Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Liu, C.

2000105  Comparison and Correlation of ESD HBM (Human Body Model) Obtained Between TLP, Wafer-Level, and Package-Level Tests

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Liu, F-W

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2013056  Design and Verification of a Novel Multi-RC-Triggered Power Clamp Circuit for On-Chip ESD Protection

Liu, R.

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2011323  Machine Model Evaluation and Interconnect Effect Study for TMR HGA

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97135  Why the Human Body Capacitance is So Large

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Liu, X.F.
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Lonborg, J.O.
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Lorenzini, M.
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2014336 A Non-Typical Latch-up Event on HV ESD Protection

Lu, G
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Lu, T-C
2012342 PMOS-Triggered PMLSCR for High Voltage Application
2014336 A Non-Typical Latch-up Event on HV ESD Protection

Lu, T-F
2014304 Metal Routing Induced Burn Out in GGNMOS ESD Protection for Low-Power DRAM Application

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2013361 Using Static Voltage Analysis and Voltage-Aware DRC to Identify EOS and Oxide Breakdown Reliability Issues

Lucas, G.H.
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94266 Fast Turn-On of an NMOS ESD Protection Transistor; Measurements and Simulations

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<table>
<thead>
<tr>
<th>Author</th>
<th>Publication Date</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Luo, J.S.</td>
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<td>GMR Heads as ESD Detectors-A Direct Assessment of Subtle ESD</td>
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<td>2004361</td>
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</tr>
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<td></td>
<td>2006100</td>
<td>ESD Induced Instability of Pinned Layer in GMR Head</td>
</tr>
<tr>
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<td>Study on High Field Transfer Curves of GMR Heads with Damaged Pinned Layer by ESD</td>
</tr>
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<td>The Effect of ESD on CCD Reliability</td>
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<td>A Novel On-Chip ESD Protection Circuit for GaAs HBT RF Power Amplifiers</td>
</tr>
<tr>
<td></td>
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</tr>
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<td>Maas, J.S.</td>
<td>90092</td>
<td>Testing Electronic Products for Susceptibility to Electrostatic Discharge</td>
</tr>
<tr>
<td>Mabboux, G.</td>
<td>97240</td>
<td>Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 µm CMOS Technology</td>
</tr>
<tr>
<td></td>
<td>2000251</td>
<td>Investigation on Different ESD Protection Strategies Devoted to 3.3 V RFApplications (2 GHz) in a 0.18 µm CMOS Process</td>
</tr>
<tr>
<td>Machida, K.</td>
<td>2004075</td>
<td>Evaluation of ESD Hardness of Fingerprint Sensor LSIs</td>
</tr>
<tr>
<td>MacWilliams, K.P.</td>
<td>95304</td>
<td>Quantifying ESD/EOS Latent Damage and Integrated Circuit Leakage Currents</td>
</tr>
<tr>
<td>Madden, P.G.</td>
<td>87241</td>
<td>Selection and Applications for Ionization Equipment</td>
</tr>
<tr>
<td>Madison, J.A.</td>
<td>79205</td>
<td>The Analysis and Elimination of EOS Induced Secondary Failure Mechanisms</td>
</tr>
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<td>Madzy, T.M.</td>
<td>79036</td>
<td>Module Electrostatic Discharge Simulator</td>
</tr>
<tr>
<td>Maeda, H.</td>
<td>2013091</td>
<td>Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate</td>
</tr>
<tr>
<td>Maene, N.</td>
<td>89157</td>
<td>The Dependence of Electrostatic Destruction Voltage on Device Structures of P-N Junctions and Insulated Films</td>
</tr>
<tr>
<td></td>
<td>92228</td>
<td>On Chip Electrostatic Discharge Protections for Inputs, Outputs and Supplies of CMOS Circuits</td>
</tr>
<tr>
<td></td>
<td>94307</td>
<td>Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit</td>
</tr>
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<td>Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 µm CMOS Technology</td>
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</tbody>
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Maes, H.E.
93129 Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model
93215 The ESD Protection Capability of SOI Snapback NMOSFETs: Mechanisms and Failure Modes
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2001062 Analysis and Improved Compact Modeling of the Breakdown Behavior of Sub-0.25 Micron ESD Protection ggNMOS Devices
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Magrini, F.
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Mahn, T.G.
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90197 Enhanced P+ Substrate Tap Conductance in the Presence of NPN Snapback
91059 Reducing Field Failure Rate with Improved EOS/ESD Design
91144 Package Effects On Human Body and Charged Device ESD Tests
92129 Integrated Circuit Metal in the Charged Device Model: Bootstrap Heating, Melt Damage, and Scaling Laws
93225 Two Unusual HBM ESD Failure Mechanisms On a Mature CMOS Process
93239 Designing On-Chip Power Supply Coupling Diodes for ESD Protection and Noise Immunity
94141 Core Clamps for Low Voltage Technologies
95001 Novel Clamp Circuits for IC Power Supply Protection
95295 Melt Filaments in n+p+n Lateral Bipolar ESD Protection Devices
97246 Protection of High Voltage Power and Programming Pins
99070 Stacked PMOS Clamps for High Voltage Power Supply Protection
99212 A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies
2001398 Improving the Balanced Coaxial Differential Probe for High-Voltage Pulse Measurements
2002001 New Considerations for MOSFET Power Clamps
2003027 Methods for Designing Low-leakage Power Supply Clamps
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
Using Coupled Transmission Lines to Generate Impedance-Matched Pulses Resembling Charged Device Model ESD

Unifying Factory ESD Measurements and Component ESD Stress Testing

Using Coupled Lines to Produce Highly Efficient Square Pulses for VF-TLP

Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System

Shielded Cable Discharge Induces Current on Interior Signal Lines

Wafer-Level Charged Device Model Testing

Evaluating TLP Transients and HBM Waveforms

HBM Tester Waveforms, Equipment Circuits, and Socket Capacitance

Filter Models of CDM Measurement Channels and TLP Device Transients

Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results

Antenna Response to CDM E-Fields

CDM Tester Properties as Deduced from Waveforms

Measuring Handler CDM Stress Provides Guidance for Factory Static Controls

Malwitz, N.

ESD Attenuation By Thin Metal Films

Mandelman, J.

Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks

Manley, R.

Novel ESD Protection for Advanced CMOS Output Drivers

Manna, I.

A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology

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Manouvrier, J-R.

Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain

A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients

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A Novel Physical Model for the SCR ESD Protection Device

Mao, W.

A Scalable Verilog-A Modeling Method for ESD Protection Devices

Marcelo, M.L.D.

Preventing Arcing Damage on Radio Frequency Device Wafer by Controlling ESD Resistively Level of Water for Saw and Wash
Marcinko, T.
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Marcon, D.
2011147  HBM ESD Robustness of GaN-on-Si Schottky Diodes

Marichal, O.
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2007366  Characterizing the Transient Device Behavior of SCRs by Means of VFTLP Waveform Analysis
2008325  CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results Between IO Test Chips and Product Level
2010167  On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8 kV Contact System Level

Marin-Cudraz, D.
2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration
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Mariolle, D.
97337  An Attempt to Explain Thermally Induced Soft Failures During Low Level ESD Stresses: Study of the Differences Between Soft and Hard

Mark, D.
94324  Failure Analysis of CMOS PALs Exhibiting ESD-Type Polygate Short To Substrate Using a State-Of-The-Art IC Diagnostic uProber

Marley, J.
2001120  Controlling ESD Damage of ICs at Various Steps of Back-End Process

Marom, H.
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Marquardt, H.
2012085  Topology-Aware ESD Checking: A New Approach to ESD Protection

Marshall, A.
2005280  ESD Evaluation of the Emerging MuGFET Technology

Martin, L.C.
79198  Statistical Failure Analysis of Military Systems for High Altitude EMP
82076  Modeling of Current and Thermal Mode Second Breakdown Phenomena
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Martin, P.
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Martinez, D.
99391  ESD Sensitivity Study of GMR Recording Heads with a Flex-On-Suspension Head-Gimbal Assembly
Martinez, P.L.
88077 Test Methods to Characterize Triboelectric Properties of Materials

Martynov, Y.B.
97013 Gate Burnout of Small Signal MODFETs at TLP Stress
97330 Electrical Filamentation in GGMOS Protection Structures

Marum, S.
2004132 Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers
2005307 Problems with IO to all Other IOs ESD Stress Test: Two Case Studies
2006001 System Event Triggered Latch-up in IC Chips: Test Issues and Chip Level Protection Design
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2007283 CDM Peak Current Variations and Impact Upon CDM Performance Thresholds
2008094 Single Pulse CDM Testing and its Relevance to IC Reliability
2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
2009183 Influence of CDM Tester Plate Size on Discharge Current
2009377 Protecting Circuits From the Transient Voltage Suppressor’s Residual Pulse During IEC 61000-4-2 Stress
2012414 Characterizing Devices Using the IEC 6100-4-5 Surge Stress

Maschietto, A.
2001249 Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

Mason, J.
95129 Effectiveness of ESD Training Using Multimedia

Mason, Jr., R.M.
82082 A Probabilistic Estimator for Bounding Transistor Emitter-Base Junction Transient-Induced Failures

Mason, K
2013214 An Active MOSFET Rail Clamp Network for Component and System Level Protection

Mass, T.R.
90237 ESD Polymer Alloys: An Alternative Approach for Producing Permanently Static Dissipative Polyethylene

Mathews, D.
80117 Some Design Criteria for Avoiding Second Breakdown in Bipolar Devices

Mathurin, J.
81198 Behavior of Thick-Film Power Resistors Subjected to Large Momentary Overloads

Matsil, I.S.
97205 What Every ESD Engineer Needs to Understand About Patents (Invited Paper)

Matsugi, J.
2003382 ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads
Matsuhashi, K.
98218 Measures Against Electrostatic Destruction of Electronic Devices at Electronic Equipment Assembly Shops

Matsui, J
2013091 Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate

Matsui, M.
87227 Electromagnetic Wave Generation From Electrostatic Discharge Between Charged Human's Body and Earthed Electrode

Matsumoto, M.
94090 New Failure Mechanism Due to Non-Wired Pin ESD Stressing

Matsuo, Y.
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Mauran, N.
2007304 Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester
2009165 Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
2013155 20GHz On-Chip Measurement of ESD Waveform for System Level Analysis
2013258 Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement

Maurer, L.
2008221 ESD Concept for High-Frequency Circuits

Mavinkurve, A.
2011210 Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment

May, J.E.
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May, J.T.
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Mayerhofer, M.T.
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2008221 ESD Concept for High-Frequency Circuits
2011187 ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology
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McAleer, R.E.
81034 A Pragmatic Approach to ESD Problem Solving in the Manufacturing Environment, A Case History
<table>
<thead>
<tr>
<th>Author</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>McAndrew, C.</td>
<td>A Physically-Based Behavioral Snapback Model</td>
</tr>
<tr>
<td>McAteer, O.J.</td>
<td>An Effective ESD Awareness Training Program</td>
</tr>
<tr>
<td></td>
<td>Identification of Latent ESD Failures</td>
</tr>
<tr>
<td></td>
<td>An Effective ESD Awareness Training Program</td>
</tr>
<tr>
<td></td>
<td>Analysis of Electrostatic Discharge Failures</td>
</tr>
<tr>
<td></td>
<td>Latent ESD Failures</td>
</tr>
<tr>
<td></td>
<td>ESD: A Decade of Progress</td>
</tr>
<tr>
<td>McCaffrey, B.</td>
<td>Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)</td>
</tr>
<tr>
<td>McCarthy, A.M.</td>
<td>Applications of a New Wafer Surface Charge Monitor</td>
</tr>
<tr>
<td>McCarthy, D.</td>
<td>Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics Toward Creating a More Repeatable Simulation or;</td>
</tr>
<tr>
<td>McCarthy, W.F.</td>
<td>Root Cause Analysis and Packaging Enhancements To Improve Processor ESD Susceptibility</td>
</tr>
<tr>
<td>McConaghy, C.F.</td>
<td>Modeling and Testing for Second Breakdown Phenomena</td>
</tr>
<tr>
<td>McCullough, D.T.</td>
<td>Reliability of EOS Screened Gold Doped 4002 CMOS Devices</td>
</tr>
<tr>
<td>McDonald, A.</td>
<td>A Pragmatic Approach to ESD Problem Solving in the Manufacturing Environment, A Case History</td>
</tr>
<tr>
<td>McFarland, W.Y.</td>
<td>The Economic Benefits of an Effective Electrostatic Discharge Awareness and Control Program - An Empirical Analysis</td>
</tr>
<tr>
<td></td>
<td>You've Implemented an ESD Program - What's Next?</td>
</tr>
<tr>
<td></td>
<td>ESD Program Auditing: The Auditor's Perspective</td>
</tr>
<tr>
<td>McGee, J.</td>
<td>Single Pulse CDM Testing and its Relevance to IC Reliability</td>
</tr>
<tr>
<td></td>
<td>Influence of CDM Tester Plate Size on Discharge Current</td>
</tr>
<tr>
<td>McKeighen, R.E.</td>
<td>Reversible Charge Induced Failure Mode of CMOS Matrix Switch</td>
</tr>
<tr>
<td>McKenna, A.</td>
<td>Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature</td>
</tr>
</tbody>
</table>
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McKinley, W.
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McLain, D.
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Medhat, D
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Meeuwsen, S.
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Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness

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A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts

Anti-Series Ggnmos ESD Clamp for Space Application IC’s

Meng, K-H

The Need for Transient I-V Measurement of Device ESD Response

Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry

Mensing, R.W.

Statistical Failure Analysis of Military Systems for High Altitude EMP

Mercha, A.

Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Mergens, M.P.J.

Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations

Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions

ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior

Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling

GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes

High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation

Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

ESD Protection Solutions for High Voltage Technologies

ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive

Merrill, R.

ESD Design Methodology

Mertens, R.

A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting

Separating SCR and Trigger Circuit Related Overshoot in SCR-based ESD Protection Circuits

Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

Theory of Active Clamp Response to Power-On ESD and Implications for Power Supply Integrity

Mettler, S.

Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations

Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions
ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior
Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress
Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
Study of CDM Specific Effects for a Smart Power Input Protection Structure
Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit

Metz, W.J.

A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

Meuse, T.

Characterization and Optimization of a Bipolar ESD – Device by Measurements and Simulations
Investigation into Socketed CDM (SDM) Tester Parasitics
Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps
HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike
VF-TLP Round Robin Study, Analysis and Results
CDM2 - A New CDM Test Method for Improved Test Repeatability and Reproducibility
Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
Activities Towards a New Transient Latch-up Standard

Meyer, R.L.

Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies

Meyerson, B.

Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors

Miao, G

On-Chip System Level ESD Protection for Class G Audio Power Amplifiers
HBM ESD Protection for Class G Power Amplifiers

Mignoli, F.

Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology

Milburn, R.T.

Diagnosis and Analysis of Emitter-Base Junction Overstress Damage
Failure Analysis of Electrostatic Sensitive ECL Gate Arrays
EOS Induced Polysilicon Migration in VLSI Gate Arrays
Mileham, J.R.

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Millar, S.

- 2010217  CDM Damage due to Automated Handling Equipment
- 2010233  Comparison of Methods of Evaluation of Charge Dissipation from AHE Soak Boats

Miller, D.

- 2010317  Problematic Natural Gas Power Plant Pumping/Irrigation

Miller, J.W.

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- 2000308  Engineering the Cascoded NMOS Output Buffer for Maximum Vt1
- 2001082  Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies
- 2003017  Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
- 2004255  Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies
- 2004280  Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications
- 2005070  ESD Protection for Advanced CMOS SOI Technologies
- 2006046  Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe
- 2006186  Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology
- 2008030  HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike
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- 2011007  A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction
- 2011076  When Good Trigger Circuits Go Bad: A Case History
- 2013313  Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps
- 2014232  A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry

Miller, J.

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Miller-Lynch, T.

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Min, K.

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  - Latch-up in Advanced CMOS Technologies
- 2006342  Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators Meet the
Minami, T.
87137 Static Electricity Elimination Using Conductive Fiber by Dyeing

Minear, R.L.
79188 The Phantom Emitter - an ESD-Resistant Bipolar Transistor Design and its Applications to Linear Integrated Circuits

Minegishi, S.
2003173 4.5GHz Measurement of Transition Duration and Frequency Spectra Due to Small Gap Discharge as Low Voltage ESD

Minixhofer, R.
2011123 Process Variation Aware ESD Design Window Considerations on a 0.18 um Analog, Mixed-Signal High Voltage Technology
2012298 ESD Induced Leakage Current Increase of Diffused Diodes

Minor, J.L.
94193 Simulation of a System Level Transient-induced Latch-Up Event

Mishra, R.
2009069 Technology Scaling of Advanced Bulk CMOS On-Chip ESD Protection
2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations
2011022 Technology Scaling Effects on the ESD Performance of Silicide-Blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies
2012319 Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers
2014021 ESD Device Performance Analysis in a 14nm FinFET Soi Cmos Technology: Fin-based versus Planar-based

Mistry, K.R.
89121 On Latency and the Physical Mechanisms Underlying Gate Oxide Damage During ESD Events in N-Channel MOSFETs
90214 Dependence of Input ESD Failure Thresholds on IC Design Style
92250 ESD Protection in a 3.3V Sub-Micron Silicided CMOS Technology
94113 Circuit Interactions During Electrostatic Discharge

Mitani, S.
79088 Failure Analysis of Microcircuits Subjected to Electrical Overstress

Mitarai, S.
99078 Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Mitard, J.
2012001 ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling

Mitchell, T.
2014342 Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting
Mitra, S.

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2009196  ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology

2009334  Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line

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2010177  Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations

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2013351  Identification and Verification of BEOL Metal Fails due to ESD Stress using Current Density Analysis Tool

Miyamoto, K.

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Miyamoto, Y.

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Mogami, T.

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Mohammadnejad, M
2013329  Auditing of a Class 0 Facility

Mohan, V.
2010381  CDM Effect on a 65 nm SOC LNA

Mohn, R.
2002010  High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

Money, R.J.
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Monfray, S.
2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Monma, H.
98199   ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate
99078   Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Monnereau, N.
2010127  Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation
2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
2011343  Investigating the Probability of Susceptibility Failure Within ESD System Level Consideration

Monstream, J.
2010091  An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies
2012068  Advanced ESD Tool Flow, Testing, and Design Verification Results

Montanaro, J.
98086   Cross Reference ESD Protection for Power Supplies

Montoya, J.A.
96145   Developing an Exit Charge Specification for Production Equipment
2000394  A Study of the Mechanisms for ESD Damage to Reticles
2005229  Unifying Factory ESD Measurements and Component ESD Stress Testing

Moon, H.S.
2002233  ESD Protection Materials Using Conductive Polymers

Moon, K.C.
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Moon, K.S.
2002233  ESD Protection Materials Using Conductive Polymers

Moon, M.G.
79104   ESD Susceptibilities of High Performance Analog Integrated Circuits
Moore, B  
2012161  Latch-up Characterization and Checking of a 55 nm CMOS Mixed Voltage Design

Moore, C.  
99309  ESD Testing of GMR Heads as a function of Temperature  
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Moosa, M  
2013313  Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

More, V.  
2011250  Interrogation of Damage-State in Leadfree Electronics under Sequential Exposure to Thermal Aging and Thermal Cycling

Morena, E.  
2003088  Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress  
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Morgan, I.H.  
88155  A Method of Calibration for Human Body Model ESD Testers to Establish Correlatable Results  
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Morimura, H.  
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Morin, G.  
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98151  Semiconductor Process and Structural Optimization of Shallow Trench Isolation- Defined and Polysilicon – Bound Source/Drain Diodes

Pekny, T.

92136  ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Pelella, A.R.

85024  A Design Methodology for ESD Protection Networks

Pellella, M.M.

2004248  ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure
2005421  SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies
2007185  Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI
2008235  ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology

Pellinen, D.

80225  Measurement of Fast Transients and Application to Human ESD

Peltoniemi, T

2012181  Triboelectrification of Static Dissipative Materials
2012248  Low Level Human Body Model ESD

Pelzl, R.M.

82049  A Survey of EOS/ESD Data Sources
85100  A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models with

Pendley, M.

2000379  Measurement Technique Developed to Evaluate Transient EMI in a Photo Bay With and Without Air Ionization
2003259  Creating and Measuring Photomask Damage

Perdu, P.

2004174  ESD Induced Latent Defects in CMOS ICs and Reliability Impact
Peretti, V.
2008272 EOS/ESD Sensitivity of Functional RF-MEMS Switches

Perez, C.N.
2005131 Guard Rings: Theory, Experimental Quantification and Design

Perez, R.
93029 Electrostatic Discharge Analyses for Spacecraft in Geosynchronous Orbit

Perillat Jr., J.
84144 An Evaluation of EOS Failure Models

Perkins, J.F.
79064 Effects of Electrical Overstress on Digital Bipolar Microcircuits and Analysis Techniques for Failure Site Location

Perreau, P.
2010185 Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Perry, B.
99293 Fields and ESD Risk from Charged Object Introduction into Hard Drives
99361 Using HGA Antennas to Measure EMI; Establishing and Correlating Damage Thresholds of GMR Heads
99373 A Study of Head Stack Assembly Sensitivity to ESD
2000318 ESD Damage Thresholds: History and Prognosis
2001311 ESD Audit Limits and Actual Damage Thresholds: A Theoretical Analysis
2002326 Impact of Insulating “Conductive” Materials on Disk Drive ESD Robustness

Pessl, P.
2005245 SoC-A Real Challenge for ESD Protection?

Petersen, R.
2006039 Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications

Peterson, J.C.
82076 Modeling of Current and Thermal Mode Second Breakdown Phenomena

Peterson, W.G.
2001272 Electronic Part Damage by Antistat Vapor

Petrizio, C.J.
79183 Electrical Overstress Versus Device Geometry

Pfaff, F.A.
90245 Electrical Characterization of Static-Dissipative Flooring

Pfeifle, R.
<table>
<thead>
<tr>
<th>Name</th>
<th>Document Number</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pham, H.</td>
<td>2000132</td>
<td>Advancements in Inherently Dissipative Polymer (IDP) Alloys Provide New Levels of Clean, Consistent ESD Protection</td>
</tr>
<tr>
<td>Phatak, S.</td>
<td>92159</td>
<td>PIN Photodetectors-The ESD Bottleneck in Laser Packages</td>
</tr>
<tr>
<td>Phelps, R</td>
<td>2012152</td>
<td>Transient Latch-up of Switching Arrays in Power Management Circuits</td>
</tr>
<tr>
<td>Philipp, H.R.</td>
<td>80026</td>
<td>Transient Protection with ZnO Varistors: Technical Considerations</td>
</tr>
<tr>
<td>Phillips, C.</td>
<td>94214</td>
<td>CDM Events in Automated Test Handlers and Environmental Testing - A Case History</td>
</tr>
<tr>
<td>Phillips, L.P.</td>
<td>82136</td>
<td>Basic Specification for ESD Protection in Industry</td>
</tr>
<tr>
<td>Phunyapinuant, S.</td>
<td>2001149</td>
<td>DC Transient Monitoring and Analysis to Prevent EOS in Burn-in Systems</td>
</tr>
<tr>
<td>Picozzi, D.</td>
<td>2004182</td>
<td>CDM Failure Modes in a 130nm ASIC Technology</td>
</tr>
<tr>
<td>Pierce, D.G.</td>
<td>81120</td>
<td>An Overview of Electrical Overstress Effects on Semiconductor Devices</td>
</tr>
<tr>
<td></td>
<td>82056</td>
<td>Modeling Metallization Burnout of Integrated Circuits</td>
</tr>
<tr>
<td></td>
<td>82082</td>
<td>A Probabilistic Estimator for Bounding Transistor Emitter-Base Junction Transient-Induced Failures</td>
</tr>
<tr>
<td></td>
<td>84144</td>
<td>An Evaluation of EOS Failure Models</td>
</tr>
<tr>
<td></td>
<td>85067</td>
<td>Electro-Thermomigration as an Electrical Overstress Failure Mechanism</td>
</tr>
<tr>
<td></td>
<td>87051</td>
<td>Critical Issues Regarding ESD Sensitivity Classification Testing</td>
</tr>
<tr>
<td></td>
<td>88137</td>
<td>Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses</td>
</tr>
<tr>
<td>Pinnoi, J.</td>
<td>2001299</td>
<td>Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process</td>
</tr>
<tr>
<td>Pirici, D.</td>
<td>2003161</td>
<td>A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach</td>
</tr>
<tr>
<td>Plana, R.</td>
<td>2009273</td>
<td>ESD Events in SiN RF-MEMS Capacitive Switches</td>
</tr>
<tr>
<td>Plaster, J.S.</td>
<td>87010</td>
<td>ESD Control in the Automotive Electronics Industry - a Case Study</td>
</tr>
<tr>
<td>Pogany, D.</td>
<td>99241</td>
<td>Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices</td>
</tr>
</tbody>
</table>
Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric Thermal Mapping

Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry

Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness

Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications

Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices

External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique

IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements

ESD Robust DeMOS Devices in Advanced CMOS Technologies

HBM ESD Robustness of GaN-on-Si Schottky Diodes

Pok, R.

Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

Polowski, M.

Pitfalls for CDM Calibration Procedures

Polgreen, T.

Improving the ESD Failure Threshold of Silicided NMOS Output Transistors by Ensuring Uniform Current Flow

Pollock, J.

Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures

Pommerenke, D.

Transient Fields of ESD

Calculation and Measurement of Transient Fields of Voluminous Objects

To What Extent Do Contact-Mode and Indirect ESD Test Methods Reproduce Reality?

Numerical Calculation of ESD

An Analysis of the Fields on the Horizontal Coupling Plane in ESD Testing

About the Different Methods of Observing ESD

Metrology and Methodology of System Level ESD Testing

Broadband Measurement of ESD Risetimes to Distinguish between Different Discharge Mechanisms

Effects of TVS Integration on System Level ESD Robustness

A Study of a Measurement and Simulation Method on ESD Noise Causing Soft-Errors by Disturbing Signals

A Novel Method for ESD Soft Error Analysis on Integrated Circuits Using a TEM Cell

A Systematic Method for Determining Soft-Failure Robustness of a Subsystem

Powered System-Level Conductive TLP Probing Method for ESD/EMI Hard Fail and Soft Fail Threshold Evaluation
Pompl, T.
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress

Pon, H.
89078 High Current ESD Damage to MOS I/O Structures Caused by Charged Video Monitor Surfaces and Casings

Poon, S.S.
2001398 Improving the Balanced Coaxial Differential Probe for High-Voltage Pulse Measurements
2002001 New Considerations for MOSFET Power Clamps
2003027 Methods for Designing Low-leakage Power Supply Clamps
2004308 Using Coupled Transmission Lines to Generate Impedance-Matched Pulses Resembling Charged Device Model ESD
2006310 Using Coupled Lines to Produce Highly Efficient Square Pulses for VF-TLP
2007311 Shielded Cable Discharge Induces Current on Interior Signal Lines

Poro, R.
2014258 Reflection Control in VF-TLP Systems

Porter, T.
98328 Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing
99361 Using HGA Antennas to Measure EMI; Establishing and Correlating Damage Thresholds of GMR Heads
99373 A Study of Head Stack Assembly Sensitivity to ESD
2002326 Impact of Insulating “Conductive” Materials on Disk Drive ESD Robustness

Portnoy, W.M.
82091 Second Breakdown in Switching Transistors
83118 Temperature at Second Breakdown at a Well-Defined Site

Posadas, A.
97287 Particle Generation of Ceramic Emitters for Cleanroom Air Ionizers

Pote, D.
92121 Annealing of ESD-induced Damage in Power MOSFETs

Prass, T.
2008040 VF-TLP Round Robin Study, Analysis and Results

Prather, B.
88177 An Integrated EMI/EMC/EMP Induced Upset Hardening Design Approach for Subsystems

Preble, B.D.
2003017 Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies

Price II, L.A.
79036 Module Electrostatic Discharge Simulator
Priestman, J.
85015 Integration of a Comprehensive Static Control Program Into an Automated Manufacturing Facility

Pritchard, D.
99168 Test Methodologies for Detecting ESD Events in Automated Processing Equipment
2000499 Electrostatic Voltmeter and Fieldmeter Measurements on GMR Recording Heads
2003265 Ion Imbalances on the Ionizer Controlled Work Surface
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry

Proctor, R.
2004166 ESD Design Automation for a 90nm ASIC Design System

Ptasinski, L.
96351 Detection Hazards Caused by ESD - Case Study, Hazards in Silos

Pupaichitkul, C.
2001299 Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process

Pusa, F.
2010083 On-Chip System ESD Protection of FM Antenna Pin

Putnam, C.S.
2001205 Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13μm CMOS Logic
2005413 PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latchup Robustness
2006179 Design and Characterization of a Multi-RC-Triggered MOSFET-based Power Clamp for On-Chip ESD Protection
2008312 ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology
2009084 Impact of Stress Engineering on High-k Metal Gate ESD Diodes in 32 nm SOI Technology

Puvvada, V.
98104 A Simulation Study of HBM Failure in an Internal Clock Buffer and the Design Issues for Efficient Power Pin Protection Strategy
2000437 A Scalable Analytical Model for the ESD N-Well Resistor

Qawami, S.
93225 Two Unusual HBM ESD Failure Mechanisms On a Mature CMOS Process

Qu, N.
2003088 Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2004107 Study of CDM Specific Effects for a Smart Power Input Protection Structure
2005080 Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit
2006303 Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses
Quan, C.
98135 Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Quan, X
2013209 HBM ESD Protection for Class G Power Amplifiers

Quittard, O.
2006077 ESD Protection for the High-Voltage CMOS Technologies
2007047 Designing HV Active Clamps for HBM Robustness

Qun, Y.
99380 ESD Damage of GMR Sensors at Head Stack Assembly

Rackley, K.
93123 EOS Induced Polysilicon Migration in VLSI Gate Arrays

Raczkowski, K.
2009329 CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS
2011116 CDM Protection for Millimeter-Wave Circuits

Raghaven, R.
82169 Circuit Design for EOS/ESD Protection

Raghavendra Rao, M.
2011230 Movement of Metallic Particles in a 3-Phase Common Enclosure Gas Insulated Substations

Raha, P.
95212 EOS/ESD Protection Circuit Design for Deep Submicron SOI Technology
97356 Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology

Rajagopal, K.
2014289 Identification of Two-Probe TLP Contact Resistance Issues and Proposed Solutions

Ramaswamy, S.
95212 EOS/ESD Protection Circuit Design for Deep Submicron SOI Technology
96285 EOS/ESD Analysis of High-Density Logic Chips
96316 Circuit-Level Simulation of CDM-ESD and EOS in Submicron MOS Devices
98161 ESD-Related Process Effects in Mixed-Voltage Sub-0.5 μm Technologies
2000505 Effect of 1nS to 250 mS ESD Transients on GMR Heads
2001071 Modeling Substrate Diodes under Ultra High ESD Injection Conditions

Ramer, C.E.
97176 ESD Control and ISO 9000

Ramos, J.
2005025 Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor
Rao, J-H
2014304  Metal Routing Induced Burn Out in GGNMOS ESD Protection for Low-Power DRAM Application

Rao, V.R.
2009221  IGBT Plugged in SCR Device for ESD Protection in Advanced CMOS Technology

Rascoe, J.
2002092  Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

Rasras, M.
98177  Non-Uniform Triggering of gg-nMOSI Investigated by Combined Emission Microscopy and Transmission Line Testing

Rastefano, E.
79147  Microwave Nanosecond Pulse Burnout Properties of One Micron MESFETS

Rataski, C.
91065  What Happens After It Leaves the Plant?

Rattawat, P.
2011210  Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment

Rauch, S.
2007009  A Self Protecting RF Output with 2kV HBM Hardness

Ravner, H.
82115  Electroactive Polymers as Alternate ESD Protective Materials

Razman, H.
2012129  Implementing Air Ionizing Blower at KLA Tencor 2401 Metrology Tool Reduce Visual Inspection Failure for Semiconductor Wafers

Read, P.H.
97139  Mitigating Electrostatic Discharge (ESD) in Solid CO2, Pellet Cleaning of Printed Wiring Boards and Assemblies

Rector, L.
98022  ESD Events in Aircraft Cabin Environment

Redden, J.
93173  Expanded Evaluation of Static Protective Shrink Wrap Film

Reddy, V.
96285  EOS/ESD Analysis of High-Density Logic Chips
2002257  Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 μm ESD Protection Circuits
2004132  Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers

Redkar, S.
2002382  Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD
Reichl, H.
2003328  A Traceable Method for the Arc-free Characterization and Modeling of CDM-Testers and Pulse Metrology Chains

Reilly, S.
2011100  Small Footprint ESD Protection of Hot-Swappable I/Os

Reimbold, G.
97337    An Attempt to Explain Thermally Induced Soft Failures During Low Level ESD Stresses: Study of the Differences Between Soft and Hard

Reiner, J.C.
95311    Latent Gate Oxide Defects Caused By CDM-ESD

Reinprecht, W.
2011123  Process Variation Aware ESD Design Window Considerations on a 0.18 um Analog, Mixed-Signal High Voltage Technology
2012298  ESD Induced Leakage Current Increase of Diffused Diodes
2013268  Activities Towards a New Transient Latch-up Standard

Reinvuo, T.
2007318  Simulation and Physics of Charged Board Model for ESD
2011279  Measurements and Simulations in Product Specific Risk Analysis

Renaud, D.P.
85006    ESD in Semiconductor Wafer Processing - An Example

Renaud, P.
2006069  Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology

Renfrew, P.
85015    Integration of a Comprehensive Static Control Program Into an Automated Manufacturing Facility

Renninger, R.G.
88162    A Microwave-Bandwidth Waveform Monitor for Charged-Device Model Simulators
89059    A Field-induced Charged-Device Model Simulator
91127    Mechanisms of Charged-Device Model Electrostatic Discharges
94042    Field-Induced ESD From CRTs: Its Cause and Cure

Reyes, B.
98139    Electrostatic Hazards of Explosive, Propellant and Pyrotechnic Powders

Reynders, K.
2002274  Effect of the n+Sinker in Self-Triggering Bipolar ESD Protection Structures
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2005407  Design and Characterization of a High Voltage SCR with High Trigger Current

Reynolds, B.
2013391  Influence of Package Parasite Elements on CDM Stress
Rhoades, W.T.
90082 ESD Stress on IC’s in Equipment

Ribardiere, P.
98118 Electrostatic Discharges from Charged Particles Approaching a Grounded Surface

Rice, A.F.
96001 An Investigation of ESD Protection for Magnetoresistive Heads

Richardson, L.M.
84202 A CMOS VLSI ESD Input Protection Device, DIFIDW
86188 Design and Test Results for a Robust CMOS VLSI Input Protection Network

Richier, C.
97240 Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 μm CMOS Technology
2000251 Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 μm CMOS Process
2005170 Impact of the CDM Tester Ground Plane Capacitance on the DUT Stress Level
2008067 A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients
2008088 A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology

Richner, J.
2000085 TLP Calibration, Correlation, Standards, and New Techniques
2001453 Correlation Considerations: Real HBM to TLP and HBM Testers
2002155 Correlation Considerations II: Real HBM to HBM testers
2003179 Real HBM & MM - The dV/dt Threat
2005141 Voltages Before and After Current in HBM Testers and Real HBM
2013140 On-Chip System Level ESD Protection for Class G Audio Power Amplifiers

Ricklef, R.
2011076 When Good Trigger Circuits Go Bad: A Case History

Ricotti, G.
2006032 Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies

Rideout, L.B.
79022 The Generation of Electrostatic Charges in Silicone Encapsulants During Cyclic Gaseous Pressure Tests

Rieck, G.
89182 Novel ESD Protection for Advanced CMOS Output Drivers

Rief, C.D.
86030 Internal Quality Auditing and ESD Control

Riess, P.
2001205 Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13μm CMOS Logic
2007328  Reliability Aspects of Gate Oxide under ESD Pulse Stress

Righter, A.W.
2002163  A New ESD Model: The Charged Strip Model
2003034  Real-World Charged Board Model (CBM) Failures
2007175  Modeling Snapback of LVTSCR Devices for ESD Circuit Simulation Using Advanced BJT and MOS Models
2009173  CDM ESD Current Characterization - Package Variability Effects and Comparison to Die-Level CDM
2010249  A New ESD Design Methodology for High Voltage DMOS Applications
2012032  Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2012254  Sampling Pin Approaches for ESD Test Applications
2013268  Activities Towards a New Transient Latch-up Standard
2014312  Non-EOS Root Causes of EOS-Like Damage

Rigour, S.
2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver

Ristikangas, P.
2012181  Triboelectrification of Static Dissipative Materials

Ritrovato, V.
2010433  A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic

Ritter, H-M.
2009308  Latent Damage Due to Multiple ESD Discharges

Ritz, M.
2005212  Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Rivenc, J.
2003161  A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach

Rivoir, R.
94292  A Method for the Characterization and Evaluation of ESD Protection Structures and Networks

Rizvi, S.A.H.
97153  Mathematical Modeling of Electrostatic Propensity of Protective Clothing Systems

Roberts, B.C.
84157  Determination of Threshold Energies and Damage Mechanisms in Semiconductor Devices Subjected to Voltage Transients

Robinson, C.M.
94085  Charged Device Damage of PLCCs Inside an Antistatic Shipping Tube - A Case History

Robinson-Hahn, D.
88015  Tape and Reel Packaging - An ESD Concern
95154  ESD Flooring: An Engineering Evaluation
Recommendations to Further Improvements of HBM ESD Component Level Test Specifications

Rödle, T.

2005001 Selecting an Appropriate ESD Protection for Discrete RF Power LD MOSTs

Rodrigo, R.D.

2001281 A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2006240 Trends in External Ionizer Monitoring and Control

Rodriguez, J.

2005043 Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window

Roesch, W.J.

86159 Electrostatic Discharge Effects on Gallium Arsenide Integrated Circuits
88062 Lack of Latent and Cumulative ESD Effects on MESFET-Based GaAs ICs

Roger, F.

2011123 Process Variation Aware ESD Design Window Considerations on a 0.18 um Analog, Mixed-Signal High Voltage Technology
2012298 ESD Induced Leakage Current Increase of Diffused Diodes

Roldan, E.

2000060 Detecting ESD Events using a Loop Antenna

Romanescu, A.

2010021 A Novel Physical Model for the SCR ESD Protection Device
2011179 Scalable Modeling Studies on the SCR ESD Protection Device

Rommers, P.

90119 Standard ESD Testing of Integrated Circuits

Ronan, B.

2002092 Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

Rooyackers, R.

2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design

Rose, P.

2006303 Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses

Rosenbaum, E.

95212 EOS/ESD Protection Circuit Design for Deep Submicron SOI Technology
96316 Circuit-Level Simulation of CDM-ESD and EOS in Submicron MOS Devices
97356 Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology
Substrate Resistance Modeling and Circuit-Level Simulation of Parasitic Device Coupling Effects for CMOS I/O Circuits Under ESD

Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors

Breakdown and Latent Damage of Ultra-Thin Gate Oxides under ESD Stress Conditions

Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies

Compact Modeling of Vertical ESD Protection NPN Transistors for RF Circuits

Comprehensive ESD Protection for RF Inputs

A Study of Vertical SiGe Thyristor Design and Optimization

Combined TLP/RF Testing System for Detection of ESD Failures in RF Circuits

Transmission Line Pulsed Waveform Shaping with Microwave Filters

A Compact, Timed-Shutoff, MOSFET-Based Power Clamp for On-Chip ESD Protection

Improved Wafer-level VFTLP System and Investigation of Device Turn-on Effects

Diode-Based Tuned ESD Protection for 5.25-GHz CMOS LNAs

Layout Guidelines for Optimized ESD Protection Diodes

A Kelvin Transmission Line Pulsing System with Optimized Oscilloscope Ranging

A Novel Testing Approach for Full-Chip CDM Characterization

Analytical Modeling of External Latchup

Voltage Clamping Requirements for ESD Protection of Inputs in 90nm CMOS Technology

Small Footprint Trigger Voltage Control Circuit for Mixed-Voltage Applications

A Dual-Base Triggered SCR With Very Low Leakage Current And Adjustable Trigger Voltage

HBM Cross Power Domain Failure Due to Secondary Tester Pulse

CDM Simulation Study of a System-in-Package

Investigation of Current Flow during Wafer-Level CDM using Real-Time Probing

Effect of On-Chip ESD Protection on 10 Gb/s Receivers

Voltage Monitor Circuit for ESD Diagnosis

Comparing FICDM and Wafer-Level CDM Test Methods: Apples to Oranges?

The Need for Transient I-V Measurement of Device ESD Response

A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting

ESD-Resilient Active Biasing Scheme for High-Speed SSTL I/Os

Separating SCR and Trigger Circuit Related Overshoot in SCR-based ESD Protection Circuits

Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components

A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry

Theory of Active Clamp Response to Power-On ESD and Implications for Power Supply Integrity
Rosenbaum, R.
2009196  ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology

Rosner, R.
2000121  Invited Paper: Conductive Materials for ESD Applications: An Overview

Rossi, M.G.
83198   A Study of ESD Latent Defects in Semiconductors

Rost, T.
2011379  Two New Unexplained and Unresolved HBM Tester Related Failures

Rothkirch, W.

Rountree, R.N.
83181   A Summary of Most Effective Electrostatic Discharge Protection Circuits for MOS Memories and their Observed Failure Modes
85045   ESD Design Considerations for ULSI
86173   Thick Oxide Device ESD Performance Under Process Variations
88201   A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes
88206   Output ESD Protection Techniques for Advanced CMOS Processes
91088   A Synthesis of ESD Input Protection Scheme

Roussel, P.J.
93129   Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model
96302   A Compact Model for the Grounded-Gate NMOS Behaviour Under CDM ESD Stress
2005152  Transient Voltage Overshoot in TLP testing - Real or Artifact?
2009152  Calibration of Very Fast TLP Transients

Rowan, W.H.
81151   EOS/ESD Failure Threshold Analysis Errors, Their Source, Size and Control
82019   Limitations in Modeling Electrical Overstress Failure in Semiconductor Devices

Rowe, W.J.
88033   Resolving ESD Incidents in Spacecraft Production Systems

Royce, S.
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<td>CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS</td>
</tr>
<tr>
<td>2009352</td>
<td>A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS</td>
</tr>
<tr>
<td>2009364</td>
<td>Self-Protection Capability of Power Arrays</td>
</tr>
<tr>
<td>2009371</td>
<td>Center Balanced Distributed ESD Protection for 1-110 GHz Distributed Amplifier in 45 nm CMOS Technology</td>
</tr>
<tr>
<td>2009405</td>
<td>On-Wafer Human Metal Model Measurements for System-Level ESD Analysis</td>
</tr>
<tr>
<td>2010157</td>
<td>SCCF-System to Component Level Correlation Factor</td>
</tr>
<tr>
<td>2010293</td>
<td>Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays</td>
</tr>
<tr>
<td>2010425</td>
<td>HBM Parameter Extraction and Transient Safe Operating Area</td>
</tr>
<tr>
<td>2010443</td>
<td>Behavior of RF MEMS Switches under ESD Stress</td>
</tr>
<tr>
<td>2011130</td>
<td>A SCR-Based ESD Protection for MEMS-Merits and Challenges</td>
</tr>
<tr>
<td>2011147</td>
<td>HBM ESD Robustness of GaN-on-Si Schottky Diodes</td>
</tr>
<tr>
<td>2012007</td>
<td>ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits</td>
</tr>
<tr>
<td>2012051</td>
<td>Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester</td>
</tr>
<tr>
<td>2012060</td>
<td>HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform</td>
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<tr>
<td>2012379</td>
<td>Mixed-Mode Simulations for Power-on ESD Analysis</td>
</tr>
<tr>
<td>2013001</td>
<td>Exploring ESD Challenges in Sub-20-nm Bulk FinFET CMOS Technology Nodes</td>
</tr>
<tr>
<td>2013022</td>
<td>ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices</td>
</tr>
<tr>
<td>2013148</td>
<td>Impact of the On-Chip and Off-Chip ESD Protection Network on Transient-Induced Latch-up in CMOS IC</td>
</tr>
<tr>
<td>2014061</td>
<td>CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus</td>
</tr>
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<tr>
<th>Schrimpf, R.D.</th>
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</thead>
<tbody>
<tr>
<td>89084</td>
<td>Electrostatic-Discharge Detectors</td>
</tr>
</tbody>
</table>
ESD Effects on the Radiation Response of Power VDMOS Transistors
Detection of ESD-Induced NonCatastrophic Damage in P-Channel Power MOSFETs
Annealing of ESD-induced Damage in Power MOSFETs

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2009084 Impact of Stress Engineering on High-k Metal Gate ESD Diodes in 32 nm SOI Technology
<table>
<thead>
<tr>
<th>Year</th>
<th>Title</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies</td>
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</tr>
<tr>
<td>2011</td>
<td>A Current Density Analysis Tool to Identify BEOL Fails Under ESD Stress</td>
<td></td>
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- Relations Between System Level ESD and (vf-) TLP
- Designing HV Active Clamps for HBM Robustness
- Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections During Fast Transients
- Gate Oxide Protection and ggNMOSTs in 65 nm
- On the Relevance of IC ESD Performance to Product Quality
- A Methodology for the ESD Test Reduction for Complex Devices
- A DRC-Based Check Tool for ESD Layout Verification
- On-Chip System ESD Protection of FM Antenna Pin
- Pitfalls for CDM Calibration Procedures
- Predictive CDM Simulation Approach Based on Tester, Package and Full Integrated Circuit Modeling
- A Contribution to the Evaluation of HMM for IO Design
- Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
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- Characterization Methods to Replicate EOS Fails

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Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics Toward Creating a More Repeatable Simulation or;
An Investigation into the Performance of the IEC 1000-4-4 Capacitive Clamp
Metrology and Methodology of System Level ESD Testing
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96022 Static Charge Control Issues for Disk Drive Production Using MR Heads

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2003017 Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
2004255 Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies
2004280  Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications
2005070  ESD Protection for Advanced CMOS SOI Technologies
2006046  Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe
2006186  Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology
2007289  A Novel Testing Approach for Full-Chip CDM Characterization
2009091  CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps
2011007  A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction
2011076  When Good Trigger Circuits Go Bad: A Case History
2013214  An Active MOSFET Rail Clamp Network for Component and System Level Protection
2013313  Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps
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Stoker, D.K.

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Stokes, S.

2002123  Effects of ESD Transients on the Properties of GMR Heads

Storm, D.C.

79004  Controlling Electrostatic Problems in the Fabrication and Handling of Spacecraft Hardware

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RF ESD Protection Strategies: Codesign vs. Low-C Protection

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94230 A New Technology in Low Tribocharging Adhesives
Resistance To Ground and Tribocharging of Personnel, As Influenced By Relative Humidity
Antistatic Masking Tapes for Solder Flux Reflow Processing of Printed Circuit Boards
Shock in the Shower
Invited Paper: ESD Control in the Factory of the Future or 20.20 to the Rescue
Compliance Verification: The Critical Component of a Certified ANSI/ESD S20.20 ESD Control Program Plan
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Electrical Fields: What to Worry About?

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Swiecicki, M.
Electrostatic Concerns in the Graphic Arts Industry

Sydänheimo, L.
ESD Sensitivity of 01005 Chip Resistors and Capacitors

Sydney, G.T.
The Versatility of Electron Beam Processing, and the Conversion of Medium and High Performance Polymeric Films for ESD Protection

Szatkowski, J.
Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies

Szymanski, M.
Evaluation of Wrist Strap Monitors from an MR Head Perspective

Tabat, N.
Limitations of the Adiabatic Model for ESD Failure in GMR Structures
Floating Gate EEPROM as EOS Indicators During Wafer-Level GMR Processing
Effects of ESD Transients on the Properties of GMR Heads

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2005203 ESD Control in Automated Placement Process
2007202 Characterization of ESD Risks in an Assembly Process by Using Component Level CDM Withstand Voltage
2010267 Characterizing Slowly Dissipative Materials
Product Specific ESD Risk Analysis
Measurements and Simulations in Product Specific Risk Analysis
Low Level Human Body Model ESD
System Level ESD Discharges with Electrical Products
Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials
Optimizing Investment in ESD Control
Electrostatic Threats in Hospital Environment
ESD Sensitivity of 01005 Chip Resistors and Capacitors

Tan, D.
Controlling ESD Damage of ICs at Various Steps of Back-End Process

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Tan, P.
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A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology
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Minimizing ESD Hazards in IC Test Handlers and Automatic Trim/Form Machines
Implementing an ESD Program in a Multi-National Company: A Cross-Cultural Experience
Evaluating and Qualifying Automated Test Handlers in a Semiconductor Company
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Use of Static-Safe Polymers in Automated Handling Equipment
Carbon Loaded Device Handling Trays: Analysis and Measurements
Non-Particulate Static Dissipative Polymers Used in Wafer Handling Equipment
Magneto Optical Static Event Detector
Test Methodologies for Detecting ESD Events in Automated Processing Equipment
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84165 Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
84189 A Failure Analysis Methodology for Revealing ESD Damage to Integrated Circuits
85141 Deficiencies in ESD Testing Methodology Highlighted by Failure Analysis
86092 Junction Degradation and Dielectric Shorting: Two Mechanisms for ESD Recovery

Taylor, T.
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Tazzoli, A.
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2008059 Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques
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2008272 EOS/ESD Sensitivity of Functional RF-MEMS Switches
2009240 Application of 3D Electromagnetic Modeling to ESD Design and Control for Class 0 Devices
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2011171 A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts
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Teague, E.
2010317 Problematic Natural Gas Power Plant Pumping/Irrigation
Teene, M.
89175 A "Waffle" Layout Technique Strengthens the ESD Hardness of the NMOS Output Transistor

Templar, L.C.
81151 EOS/ESD Failure Threshold Analysis Errors, Their Source, Size and Control

Teng, T.
79168 Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature
80087 LSI Design Considerations for ESD Protection Structures Related to Process and Layout Variations

Teng, Z.Y.
2001295 A Study of GMR Breakdown Damage in Cleaning
2002332 ESD Damage by Arcing near GMR Heads
2004346 Breakdown Behavior of TMR Head in ESD Transients
2006108 Breakdown Evaluation of Ultrathin Barrier Magnetic Tunnel Junctions with V-Ramp Testing
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Tenzer, F.D.
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Ter Beek, M.
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2004117 Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application
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Terashige, T.
2002240 Noise Reduction of Corona Discharge Air Ionizer
2006235 Development of Ion Balance Sensor by using MOSFET
2007237 Noise Characteristics of MOSFET Ionizer Balance Sensor
2008174 Electrostatic Control System Using Ceramic Transformer
2009055 Space Charge Balance Sensing for Static Control
2010273 Neutralizing Current Sensor for AC Corona Ionizer
2013037 Basic Characteristics of the Field Assisted Air Ionizer

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Terol, G.
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Testin, A.  
2009387 Human Metal Model (HMM) Testing, Challenges to Using ESD Guns

Tew, C.P.  
2003291 Exploring a Clean ESD Laminate & Ionic Contamination Methodology

Theis, T.L.  
97188 ESD Program Auditing: The Auditor's Perspective

Thiemann, U.  

Thijs, S.  
2003195 Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits  
2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node  
2004040 ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions  
2004098 Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies  
2004316 Multilevel Transmission Line Pulse (MTLP) Tester  
2005025 Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor  
2005152 Transient Voltage Overshoot in TLP testing - Real or Artifact?  
2007053 Voltage Overshoot Study in 20V DeMOS-SCR Devices  
2007089 Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis  
2007158 Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions  
2007242 T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology  
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications  
2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices During HBM ESD Stress  
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors  
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets  
2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness  
2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design  
2009152 Calibration of Very Fast TLP Transients  
2009265 A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response Under EOS-ESD Stress  
2009329 CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS  
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On-Wafer Human Metal Model Measurements for System-Level ESD Analysis

SCCF-System to Component Level Correlation Factor

Improving the ESD Self-Protection Capability of Integrated Power NLD[MOS Arrays

HBM Parameter Extraction and Transient Safe Operating Area

Behavior of RF MEMS Switches under ESD Stress

On Gated Diodes for ESD Protection in Bulk FinFET CMOS Technology

CDM Protection for Millimeter-Wave Circuits

A SCR-Based ESD Protection for MEMS-Merits and Challenges

HBM ESD Robustness of GaN-on-Si Schottky Diodes

ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling

ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits

Mixed-Mode Simulations for Power-on ESD Analysis

Exploring ESD Challenges in Sub-20-nm Bulk FinFET CMOS Technology Nodes

Anti-Series Gnnmos ESD Clamp for Space Application IC’s

Semiconductor Device Failure Criteria for Sinusoidal Stresses

Behavior of Thick-Film Power Resistors Subjected to Large Momentary Overloads

Discrete Semiconductor ESD Testing to 40 kV

A Survey of EOS/ESD Data Sources

Air Force Maintenance Program for Electrical Overstress/Electrostatic Discharge (EOS/ESD) Control

ESD Damage, Does it Happen on PCBs?

Theory of Active Clamp Response to Power-On ESD and Implications for Power Supply Integrity

Microwave Nanosecond Pulse Burnout Properties of One Micron MESFETS

Functional Methods to Determine the EPA Compatibility of Mechanical Tools

Anti-Series Gnnmos ESD Clamp for Space Application IC’s

A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal Ics
<table>
<thead>
<tr>
<th>Author</th>
<th>Paper Title</th>
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<tbody>
<tr>
<td>Tian, H.</td>
<td>99315 ESD Protection of GMR Heads in Manufacturing</td>
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<tr>
<td></td>
<td>99380 ESD Damage of GMR Sensors at Head Stack Assembly</td>
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<td>Ting, L.M.</td>
<td>2001445 Integration of TLP Analysis for ESD Troubleshooting</td>
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<td>2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed</td>
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<td>Todoroki, S.</td>
<td>2001306 Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group</td>
</tr>
<tr>
<td>Togari, H.</td>
<td>96365 Electrostatic Problems in TFT-LCD Production and Solutions Using Ionization</td>
</tr>
<tr>
<td>Tokunaga, T.</td>
<td>2009055 Space Charge Balance Sensing for Static Control</td>
</tr>
<tr>
<td>Tomibe, J.</td>
<td>98018 Controlling ESD and Absorbing and Shielding EMW by Using Conductive Fiber in Aircraft</td>
</tr>
<tr>
<td>Tong, M.H.</td>
<td>96280 Study of Gated PNP as an ESD Protection Device for Mixed-Voltage and Hot-Pluggable Circuit Applications</td>
</tr>
<tr>
<td>Tong, P.</td>
<td>2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation</td>
</tr>
<tr>
<td>Toneya, Y.</td>
<td>93009 Impulsive ESD Noise Occurred From an Office Chair</td>
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<td>94164 Impulsive EMI Effects From ESD On Raised Floor</td>
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<td>Patent Number</td>
<td>Title</td>
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<tr>
<td>96327</td>
<td>Study of ESD Quench Effects by Air Ionization</td>
</tr>
<tr>
<td>81065</td>
<td>Incoming Inspection of Antistatic Packaging Materials</td>
</tr>
<tr>
<td>2010075</td>
<td>TLP Characterization for Testing System Level ESD Performance</td>
</tr>
<tr>
<td>2001082</td>
<td>Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies</td>
</tr>
<tr>
<td>2003017</td>
<td>Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies</td>
</tr>
<tr>
<td>2006131</td>
<td>A New Electrical Overstress (EOS) Test for Magnetic Recording Heads</td>
</tr>
<tr>
<td>2009286</td>
<td>Using VFTLP Data to Design for CDM Robustness</td>
</tr>
<tr>
<td>2002281</td>
<td>Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN</td>
</tr>
<tr>
<td>2004174</td>
<td>ESD Induced Latent Defects in CMOS ICs and Reliability Impact</td>
</tr>
<tr>
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<td>Transient Voltage Overshoot in TLP testing - Real or Artifact?</td>
</tr>
<tr>
<td>2006039</td>
<td>Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications</td>
</tr>
<tr>
<td>2007089</td>
<td>Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis</td>
</tr>
<tr>
<td>2007158</td>
<td>Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions</td>
</tr>
<tr>
<td>2007242</td>
<td>T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology</td>
</tr>
<tr>
<td>2007408</td>
<td>Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications</td>
</tr>
<tr>
<td>2008295</td>
<td>Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets</td>
</tr>
<tr>
<td>2009059</td>
<td>Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness</td>
</tr>
<tr>
<td>2009076</td>
<td>Electrical and Thermal Scaling Trends for SOI FinFET ESD Design</td>
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<tr>
<td>2009165</td>
<td>Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System</td>
</tr>
<tr>
<td>2009273</td>
<td>ESD Events in SiN RF-MEMS Capacitive Switches</td>
</tr>
<tr>
<td>2010127</td>
<td>Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation</td>
</tr>
<tr>
<td>2011045</td>
<td>High Temperature Operation MOS-IGBT Power Clamp for Improved ESD Protection in Smart Power SOI Technology</td>
</tr>
<tr>
<td>2011241</td>
<td>Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection</td>
</tr>
<tr>
<td>2011329</td>
<td>ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver</td>
</tr>
<tr>
<td>2011343</td>
<td>Investigating the Probability of Susceptibility Failure Within ESD System Level Consideration</td>
</tr>
<tr>
<td>2013258</td>
<td>Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement</td>
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<tr>
<td>2001445</td>
<td>Integration of TLP Analysis for ESD Troubleshooting</td>
</tr>
</tbody>
</table>
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2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design
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Trivedi, N.
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2011307  An Automated Approach for Verification of On-Chip Interconnect Resistance for Electrostatic Discharge Paths
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Ukkonen, L.
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84040 A Room Ionization System for Electrostatic Charge and Dust Control
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86059 Sheet Resistance Measurement of Buried Shielding Layers
86127 Triboelectric Charging of Personnel From Walking on Tile Floors
87007 The March of the EOS/ESD Ducks
88077 Test Methods to Characterize Triboelectric Properties of Materials
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2005393 Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies Avoiding Competitive
2006172 Concept for Bulk Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering
2007366 Characterizing the Transient Device Behavior of SCRs by Means of VFTLP Waveform Analysis
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Van Dalen, R.
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94307  Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit

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Van Hoof, C.
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van IJzerloo, A.
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Van Laecke, A.
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Van Lint, V.A.
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van Maasakkers, M.
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van Roozendaal, L.
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90143 An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes

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2006136 Relations Between System Level ESD and (vf-) TLP
2009292 A DRC-Based Check Tool for ESD Layout Verification
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94307 Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit

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Varrot, M.
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Vashchenko, V.A.
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97330 Electrical Filamentation in GGMOS Protection Structures
2002101 Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway
2004117 Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application
2005387 Implementation of High VT Turn-on in Low-Voltage SCR Devices
2006039 Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications
2006064 Dual-Direction Isolated NMOS-SCR Device for System Level ESD Protection
2007053 Voltage Overshoot Study in 20V DeMOS-SCR Devices
2007075 Implementation of Dual-Direction SCR Devices in Analog CMOS Process
2008196 Small Footprint Trigger Voltage Control Circuit for Mixed-Voltage Applications
2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices During HBM ESD Stress
2008242 A Dual-Base Triggered SCR With Very Low Leakage Current And Adjustable Trigger Voltage
2009204 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses
2009344 System Level and Hot Plug-in Protection of High Voltage Transient Pins
2009364 Self-Protection Capability of Power Arrays
2009405 On-Wafer Human Metal Model Measurements for System-Level ESD Analysis
2010157 SCCF-System to Component Level Correlation Factor
2010293 Improving the ESD Self-Protection Capability of Integrated Power NLDMS Arrays
2010301 Study of Power Arrays in ESD Operation Regimes
2010425 HBM Parameter Extraction and Transient Safe Operating Area
2011140 Active Clamp Implementation in Complementary BiCMOS Process with High Voltage BJT Devices
2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes
2012348 SCR Clamps with Transient Voltage Detection Driver
2014189 Automated Latchup Analysis
2014342 Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting

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2002111 Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices
2003195 Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits
2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2004040 ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions
2004098 Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies
2004316 Multilevel Transmission Line Pulse (MTLP) Tester
2005152 Transient Voltage Overshoot in TLP testing - Real or Artifact?
2009322 Diode Isolation Concept for Low Voltage and High Voltage Protection Applications
2010335 Spacecraft Charging and an Instrument for its Monitoring Aboard the International Space Station
2014282 Over-Voltage Protection Strategies for LED Based Light Source Systems and other Applications

Vaughn, J.
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Vaxman, A.
98001 New Injection Moldable ESD Compounds Based on Very Low Carbon Black Loadings
99251 Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing
2000139 Controlling ESD and Cleanliness by Using New Thermoplastic Compounds for Injection Molded and Corrugated Packaging Products

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Veloso, Anabela
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Venkatashubramanian, R.
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   2011395  Using Directional Couplers to Overcome the Bandwidth Limitations of IV-Probes in TLP Measurements

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   93129  Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model
   93215  The ESD Protection Capability of SOI Snapback NMOSFETs: Mechanisms and Failure Modes
   94049  Influence of Tester, Test Method and Device Type On CDM ESD Testing
   94096  ESD Protection Elements During HBM Stress Tests - Further Numerical and Experimental Results
   96040  Recommendations to Further Improvements of HBM ESD Component Level Test Specifications
   96302  A Compact Model for the Grounded-Gate NMOS Behaviour Under CDM ESD Stress
   98301  Investigation into Socketed CDM (SDM) Tester Parasitics
   2000018  Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices
   2000085  TLP Calibration, Correlation, Standards, and New Techniques
   2001001  Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling
   2001022  GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes
   2002010  High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
   2002155  Correlation Considerations II: Real HBM to HBM testers
   2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design
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2007202  Characterization of ESD Risks in an Assembly Process by Using Component Level CDM Withstand Voltage  
2007318  Simulation and Physics of Charged Board Model for ESD  
2009414  ESD Event Receiver for System Level Testing  
2010267  Characterizing Slowly Dissipative Materials  
2011202  Product Specific ESD Risk Analysis  
2012181  Triboelectrification of Static Dissipative Materials  
2012248  Low Level Human Body Model ESD  
2013084  Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials  
2014033  Optimizing Investment in ESD Control  
2014206  Electrostatic Threats in Hospital Environment  

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ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads

Linewidth Control Effects on MOSFET ESD Robustness

CMOS-ON-SOI ESD Protection Networks

Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks

ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced Semiconductor Technology

Semiconductor Process and Structural Optimization of Shallow Trench Isolation- Defined and Polysilicon – Bound Source/Drain Diodes

Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips

A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies

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Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

An Automated Electrostatic Discharge Computer-Aided Design System with the Incorporation of Hierarchical Parameterized Cells in BiCMOS Analog and RF Technology For Mixed Signal Applications

The Effect of Deep Trench Isolation, Trench Isolation and Sub-collector Doping on the Electrostatic Discharge (ESD) Robustness of Radio Frequency (RF) ESD STI-Bound P+/N-Well Diodes in BiCMOS Silicon Germanium Technology

Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

Low-Voltage Diode-Configured SiGe:C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (fT/fMAX)

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Vuorinen, R.

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Young, M.
2000413 ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors
<table>
<thead>
<tr>
<th>Author</th>
<th>Paper Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Young, P.A.</td>
<td>Electrical Overstress Investigations in Modern Integrated Circuit Technologies</td>
</tr>
<tr>
<td></td>
<td>Power Failure Modeling of Integrated Circuits</td>
</tr>
<tr>
<td>Young, W.</td>
<td>A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods</td>
</tr>
<tr>
<td>Yu, B.</td>
<td>Punchthrough Transient Voltage Suppressor for EOS/ESD Protection of Low-Voltage ICs</td>
</tr>
<tr>
<td>Yu, S.</td>
<td>ESD Polymer Alloys: a Novel Approach for Permanently Static Dissipative Thermoplastics</td>
</tr>
<tr>
<td>Yue, W.</td>
<td>Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor</td>
</tr>
<tr>
<td>Zacher, D.</td>
<td>New Charged-Plate Monitor Design Offers Greater Flexibility</td>
</tr>
<tr>
<td>Zaengl, F.</td>
<td>Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices</td>
</tr>
<tr>
<td>Zaharia, C.</td>
<td>Development of an Experimental Platform to Study the Effect of Speed of Approach on the Electrostatic Discharge (ESD) Event</td>
</tr>
<tr>
<td>Zait, E.</td>
<td>ESD Attenuation By Thin Metal Films</td>
</tr>
<tr>
<td>Zajac, H.R.</td>
<td>Study of Effects of Electro-Static Discharge on Solid-State Devices</td>
</tr>
<tr>
<td>Zangl, F.</td>
<td>High Abstraction Level Permutational ESD Concept Analysis</td>
</tr>
<tr>
<td></td>
<td>SoC-A Real Challenge for ESD Protection?</td>
</tr>
<tr>
<td>Zanoni, E.</td>
<td>Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology</td>
</tr>
<tr>
<td></td>
<td>Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes</td>
</tr>
<tr>
<td></td>
<td>ESD Robustness of AlGaN/GaN HEMT Devices</td>
</tr>
<tr>
<td>Zaridze, R.</td>
<td>Calculation and Measurement of Transient Fields of Voluminous Objects</td>
</tr>
<tr>
<td></td>
<td>Numerical Calculation of ESD</td>
</tr>
</tbody>
</table>
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A Survey of EOS/ESD Data Sources
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Modeling Metallization Burnout of Integrated Circuits
82062  Volmerange, H., TRW
An Improved EOS Conduction Model of Semiconductor Devices
82071  Ward, A.L., Harry Diamond Laboratories
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82110  Davenport, D.E., Tracor MBA
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ESD in I.C. Assembly (A Base Line Solution) [BPR]
82145  Strand, C.J., Tweet, A., Weight, M.E., Sperry Univac
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82157  Youn, S.Y., Hartdegen, N.J., Sharp, M.J., MOSTEK Corporation
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Uniform ESD Protection in a Large Multi-Department Assembly Plant
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Sauers, J.P., Magnavox Government and Industrial Company
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86224 Enoch, D.R., Shaw, R.N., British Telecom
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87205 Anderson, Jr., W.T., USN, Naval Research Laboratory, Chase, E.W., Bell Communications Research
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ESD Design Methodology

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Designing On-Chip Power Supply Coupling Diodes for ESD Protection and Noise Immunity

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Realities of Wrist Strap Monitoring Systems

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Field-Induced ESD From CRTs: Its Cause and Cure

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Bi-Modal Triggering for LVSCR ESD Protection Devices

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ESD Trigger Circuit

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**Charge Generation From Floor Materials Using a Rolling Friction Tester**

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ESD Control Program: A Viewpoint From the Receiving End

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Resistance To Ground and Tribocharging of Personnel, As Influenced By Relative Humidity

95154 Robinson-Hahn, D., AT&T Microelectronics
ESD Flooring: An Engineering Evaluation

95162 Duvvury, C., Amerasekera, A., Texas Instruments, Inc.
Advanced CMOS Protection Device Trigger Mechanisms During CDM [BPR]
A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices

Study of ESD Evaluation Methods for Charged Device Model

Transient-induced Latchup Testing of CMOS Integrated Circuits

ESD Reliability Impact of P+ Pocket Implant On Double Implanted NLDD MOSFET

Layout Optimization of an ESD-Protection N-MOSFET By Simulation and Measurement

EOS/ESD Protection Circuit Design for Deep Submicron SOI Technology

Use of Static-Safe Polymers in Automated Handling Equipment

Cross-Linkable Conducting Polymer Coatings

Electrically Conductive Polypropylene-Polyaniline Blend in ESD Protection

Carbon Loaded Device Handling Trays: Analysis and Measurements

Best Practices for Applying Air Ionization

A Method for Measurement of Triboelectric Charging

Electrostatic Decay Measurement Theory and Applications

Failure Analysis of Shallow Trench Isolated ESD Structures

The Correlation Between Latch-Up Phenomenon and Other Failure Mechanisms

Melt Filaments in n+pn+ Lateral Bipolar ESD Protection Devices

Quantifying ESD/EOS Latent Damage and Integrated Circuit Leakage Currents

Latent Gate Oxide Defects Caused By CDM-ESD

ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads [BPP]

Explosions and Static Electricity

ESD - An Explosive Subject?

An Investigation of ESD Protection for Magnetoresistive Heads

Field-induced Charged Device Model Testing of Magnetoresistive Recording Heads

Characterization of ESD Tweezers for Use with Magnetoresistive Recording Heads

Static Charge Control Issues for Disk Drive Production Using MR Heads
ESD Induced Capacitor Shorts

Chase, G., Bellcore; Patel, J., The Pennsylvania State University
A Low Cost Visual Indicator for Detecting Ground Connection Failure of CRT Filter Screens

Verhaege, K., David Sarnoff Research Center; Russ, C., Groeseneken, G., IMEC; Robinson-Hahn, D., Lin, D., Lucent Technologies; Farris, M., Intel; Scanlon, J., American Systems Corporation; Veltri, J., Digital
Recommendations to Further Improvements of HBM ESD Component Level Test Specifications [BPR]

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ESD and Latch Up Phenomena on Advanced Technology LSI

Gieser, H., Haunschild, M., Fraunhofer-Institut Festkorpertechnologie
Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model [BPP]

Li, S., Lee, K., Hulog, J., Kazmi, S., Yin, S., Pollock, J., Advanced Micro Devices
Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures

Voldman, S., Never, J., Holmes, S., Adkisson, J., IBM Microelectronics Division
Linewidth Control Effects on MOSFET ESD Robustness

Almazar, R., Hoffman, B., Motorola-Philippines, Inc.
Immediate Elimination of Gross ESD Failures in PLCC MECL Product Line Through Innovative Techniques

Bernier, J., Croft, G., Harris Semiconductor
Die Level CDM Testing Duplicates Assembly Operation Failures

Jarrett, T., Cardiac Pacemakers, Inc.; Unger, B., CRO-BAR, Inc.
Interconnects for Device ESD Protection

Helling, K., Siemens AG
ESD Protection Measures Return on Investment Calculation and Case Study

Steinman, A., Ion Systems, Inc.; Montoya, J., Intel Corporation
Developing an Exit Charge Specification for Production Equipment

Vosteen, W., Monroe Electronics, Inc.
Alternate Uses for the Charged Plate Monitor

Baumgartner G., Lockheed Martin Missiles & Space
ESD Demonstrations to Increase Engineering & Manufacturing Awareness

Henry, L.G., Advanced Micro Devices; Hyatt, H., Hyger Physics, Inc.; Barth, J., Barth Electronics, Inc.; Stevens, M., Motorola; Diep, T., Texas Instruments
Charged Device Model (CDM) Metrology: Limitations and Problems

Glattli, P., Swiss Telecom PTT
What is a Real 1 GHz Bandwidth ESD Generator Calibration?

Takai, T., Kaneko, M., Hitachi Electronics Services Co., Ltd.; Honda, M., Impulse Physics Laboratory, Inc.
One of the Methods of Observing ESD Around Electronic Equipments

Greason, W., Bulach, S. Flatley, M., University of Western Ontario
Non-invasive Detection and Characterization of ESD Induced Phenomena in Electronic Systems

Jobava, R., Karkashadze, D., Zaridze, R., Shubitidze, P., Tbilisi State University; Pommerenke, D., Technical University Berlin; Aidam, M., Technical University Munich
Numerical Calculation of ESD
Barth, J., Barth Electronics, Inc.; Dale, D., Hall, K., McCarthy, D., Hewlett Packard; Hy aft, H., Hyger
Physics, Inc.; Nuebel, J., Sun Microsystems; Smith, D., Auspex Systems
Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics Toward Creating
a More Repeatable Simulation or: Simulators Should Simulate

Smith, D., Auspex Systems
An Investigation into the Performance of the IEC 1000-4-4 Capacitive Clamp

Somasiri, N., Talbot, V., Clatanoff, W., Morrison, E., 3M Company
Vanadium Pentoxide Based Antistatic Coatings

Extrand, C., Fluoroware
Comparison of Several Anti-Static Surfactant Coatings for Plastics

Ball, A., Yau, S., Gutman, G., Swenson, D. 3M/Electrical Specialties Division
Antistatic Masking Tapes for Solder Flux Reflow Processing of Printed Circuit Boards

Rudman, B., Chandler, C., Cortec Corporation
A Hybrid Technology: Static Dissipative/VCI Films

Zacher, D., Trek, Inc.
New Charged-Plate Monitor Design Offers Greater Flexibility

Ehrmaier, B., Schmeer, H., Universitaet der Bundeswehr Muenchen
Some Results in Measuring Static Decay

Beebe, S., Advanced Micro Devices
Methodology for Layout Design and Optimization of ESD Protection Transistors

Croft, G., Harris Semiconductor
Transient Supply Clamp with a Variable RC Time Constant

Tong, M., Gauthier, R. Gross, V., IBM Microelectronics Division
Study of Gated PNP as an ESD Protection Device for Mixed-Voltage and Hot-Pluggable Circuit
Applications

Ramawamy, S., Kang, S., University of Illinois at Urbana-Champaign; Duvvury, C., Amerasekera, A.,
Reddy, V., Texas Instruments, Inc.
EOS/ESD Analysis of High-Density Logic Chips

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Center
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Davies, D.K., Markab
The ESD Threat

Honda, M., Impulse Physics Laboratory, Inc.; Murakami, T., Harada Corporation; Tonoya, Y. Tokyo
Metropolitan Industrial Research Center
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Thurmer, J., 3M Laboratories (Europe) GmbH
Functional Methods to Determine the EPA Compatibility of Mechanical Tools

Ptasinski, L., Zeglen, T., University of Mining and Metallurgy; Gajewski, A., Cracow Academy of Economy
Detection Hazards Caused by ESD - Case Study, Hazards in Silos

Holdstock, P., Wilson, N., British Textile Technology Group
The Effect of Static Charge Generated on Hospital Bedding
<table>
<thead>
<tr>
<th>Paper ID</th>
<th>Authors</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>97001</td>
<td>Bock, K., IMEC</td>
<td>ESD Issues in Compound Semiconductor High-Frequency Devices and Circuits</td>
</tr>
<tr>
<td>97013</td>
<td>Vashchenko, V., Sinkevitch, V., SRI Pulsar; Martynov, J., SRPC Istok</td>
<td>Gate Burnout of Small Signal MODFETs at TLP Stress</td>
</tr>
<tr>
<td>97018</td>
<td>Neitzert, H-C., Cappa, V., Crovato, R., CSELT</td>
<td>Influence of the Device Geometry and Inhomogeneity on the Electrostatic Discharge Sensitivity of InGaAs/InP Avalanche Photodetectors</td>
</tr>
<tr>
<td>97027</td>
<td>Lipka, K.-M., Schmid, P., Birk, M., Splingart, B., Kohn, E., Schneider, J., Heinecke, H., University of Ulm; Demmler, M., Tasker, P., Fraunhofer Institut Freiburg</td>
<td>Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs</td>
</tr>
<tr>
<td>97033</td>
<td>Fromm, L., Hewlett Packard; Klein, W., K&amp;S Laboratories; Fowler, S., Fowler Associates</td>
<td>Procedures for the Design, Analysis and Auditing of Static Control Flooring/Footwear Systems</td>
</tr>
<tr>
<td>97049</td>
<td>Tan, W., Advanced Micro Devices</td>
<td>Non-Particulate Static Dissipative Polymers Used in Wafer Handling Equipment</td>
</tr>
<tr>
<td>97059</td>
<td>Smith, J., Lockheed Martin Advanced Technology Center</td>
<td>General EOS/ESD Equation</td>
</tr>
<tr>
<td>97068</td>
<td>Baumgartner, G., Lockheed Martin Missiles and Space</td>
<td>Analysis of ESD Glove Use</td>
</tr>
<tr>
<td>97076</td>
<td>Van den Berghe, S., De Zutter, D., University of Ghent</td>
<td>ESD Entrypoints: Coaxial Cables vs. Shielding Apertures</td>
</tr>
<tr>
<td>97083</td>
<td>Bernier, J., Croft, G., Lowther, R., Harris Semiconductor</td>
<td>ESD Sources Pinpointed by Analysis of Radio Wave Emissions</td>
</tr>
<tr>
<td>97088</td>
<td>Lin, D., DeChiaro, L., Jon, M-C., Lucent Technologies/Bell Laboratories</td>
<td>A Robust ESD Event Locator System With Event Characterization</td>
</tr>
<tr>
<td>97099</td>
<td>Frei, S., Technical University of Berlin; Pommerenke, D., Hewlett Packard</td>
<td>An Analysis of the Fields on the Horizontal Coupling Plane in ESD Testing</td>
</tr>
<tr>
<td>97107</td>
<td>Lo, T., Alexander, P., University of Windsor; Wong, S., PQT Systems</td>
<td>Fast Fourier Transform Analysis of Published ESD Waveforms and Narrowband Frequency Domain Measurement of Human ESD Events</td>
</tr>
<tr>
<td>97117</td>
<td>Frei, S., Technical University of Berlin; Pommerenke, D., Hewlett Packard</td>
<td>About the Different Methods of Observing ESD</td>
</tr>
<tr>
<td>97125</td>
<td>Greason, W., University of Western Ontario</td>
<td>Methodology to Simulate Speed of Approach in Electrostatic Discharge (ESD)</td>
</tr>
<tr>
<td>97132</td>
<td>Wu, Z., Huang, J., Liu, S., Institute of Applied Electrostatics</td>
<td>Measurements of Body Impedance for ESD</td>
</tr>
<tr>
<td>97135</td>
<td>Huang, J., Wu, Z., Liu, S., Institute of Applied Electrostatics</td>
<td>Why the Human Body Capacitance is So Large</td>
</tr>
<tr>
<td>97153</td>
<td>Gonzalez, J., Rizvi, S., Crown, E., Smy, P., University of Alberta</td>
<td>Mathematical Modeling of Electrostatic Propensity of Protective Clothing Systems</td>
</tr>
<tr>
<td>97170</td>
<td>Gaertner, R., Helling, K., Biermann, G., Bradza, E., Haberhauer, R., Koehl, W., Mueller, R., Niggemeier, W., Soder, B., Siemens AG</td>
<td>Grounding Personnel via the Floor/Footwear System</td>
</tr>
</tbody>
</table>
Kolyer, J., Ramer, C., Williams, W., Boeing North American, Inc.

ESD Control and ISO 9000

Theis, T., McFarland, W., Brin, R., Lucent Technologies

ESD Program Auditing: The Auditor's Perspective

Noll, C., ITW Static Control and Air Products, SIMCO Static Control and Cleanroom Products; Lawless, P., Research Triangle Institute, Center for Engineering and Environmental Technology

Comparison of Germanium and Silicon Needles as Emitter Electrodes for Air Ionizers

Matsil, I., Texas Instruments, Inc.

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Voldman, S., Assaderaghi, F., Mandelman, J., Hsu, L., Shahidi, G., IBM

Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks

Notermans, G., Philips Semiconductors

On the Use of N-Well Resistors for Uniform Triggering of ESD Protection Elements

Chen, J., Amerasekera, A., Duvvury, C., Texas Instruments, Inc.

Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes

Richier, C., Mabboux, G., SGS-Thomson; Maene, N., Bellens, R., Alcatel Telecom

Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 µm CMOS Technology

Maloney, T., Parat, K., Clark, N., Darwish, A., Intel Corporation

Protection of High Voltage Power and Programming Pins


Neteler, J., Richmond Technology, Inc.

Clean Room ESD Packaging Overview

Cooper, D., Linke, R., The Texwipe Company

Measurement of Cleanroom Fabric Surface Resistivities

Dyer, M., DuPont

The Antistatic Performance of Cleanroom Clothing - Do Tests on the Fabric Relate to the Performance of the Garment Within the Cleanroom?

Okano, K., Posadas, A., Polytechnic University

Particle Generation of Ceramic Emitters for Cleanroom Air Ionizers

Swiecicki, M., Static Solutions, Inc.

Electrostatic Concerns in the Graphic Arts Industry

Steinman, A., Ion Systems, Inc.

Static Control Technology Preserves Ancient Egyptian Artifacts

Swenson, D., 3M/Electrical Specialties Division

Shock in the Shower

Bock, K., Russ, C., Badenes, G., Groesenenken, G., Deferm, L., IMEC

Influence of Well Profile and Gate Length on the ESD Performance of a Fully Silicided 0.25 um CMOS Technology

Voldman, S., IBM Microelectronics Division

ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced Semiconductor Technology

Vashchenko, V., Sinkevitch, V., SRI Pulsar; Martynov, J., SRPC Istok

Electrical Filamentation in GGMOS Protection Structures

Salome, P., Leroux, C., Mariolle, D., Lafond, D., Reimbold, G., LETI CEA Technologies, Chante, J., CEGELY ECPA-INSa; Crevel, P., MATRA MHS

An Attempt to Explain Thermally Induced Soft Failures During Low Level ESD Stresses: Study of the Differences Between Soft and Hard NMOS Failures
Unique ESD Failure Mechanisms During Negative to VCC HBM Tests

Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology

Does the ESD-Failure Current Obtained by Transmission Line Pulsing Always Correlate to Human Body Model Tests?

Decay-Time Characterization of ESD Materials for Use with Magnetoresistive Recording Heads

Field-Induced Breakdown ESD Damage of Magnetoresistive Recording Heads

Characterization of ESD Damaged Magnetoresistive Recording Heads

"Direct Charging" Charge Device Model Testing of Magnetoresistive Recording Heads

Three-Dimensional Transient Simulation of Magnetoresistive Head Temperature During an ESD Event

Effects of Unbalanced Ionizers on Magnetoresistive Recording Heads

New Injection Moldable ESD Compounds Based on Very Low Carbon Black Loadings

Evaluation of Cleanroom/ESD Garment Fabrics: Test methods and Results

Controlling ESD and Absorbing and Shielding EMW by Using Conductive Fiber in Aircraft

ESD Events in Aircraft Cabin Environment

Metrology and Methodology of System Level ESD Testing

An Experimental and Theoretical Consideration of Physical Design Parameters in Field-Induced Charged Device Model ESD Simulators and Their Impact upon Measured Withstand Voltages

ESD Protection for Mixed Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration

A Substrate Triggered Lateral Bipolar Circuit for High Voltage Tolerant ESD Protection Applications

How to Safely Apply the LVTSCR for CMOS Whole-Chip Protection without being Accidentally Triggered On

Cross Reference ESD Protection for Power Supplies

High Voltage Resistant ESD Protection Circuitry for 0.5 μm CMOS OTP/EPROM Programming Pin

A Simulation Study of HBM Failure in an Internal Clock Buffer and the Design Issues for Efficient Power Pin Protection Strategy

Human Body Capacitance: Static or Dynamic Concept?

Electrostatic Discharges from Charged Particles Approaching a Grounded Surface
Outgassing, Volatile Organic Content, and Contamination Content of Materials Used in Today’s Electronics Workplace

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Institute of Post and Telecommunication

Electrostatic Hazards of Explosive, Propellant and Pyrotechnic Powders

S. Voldman, S. Geissler, J. Nakos, J. Pekarik, R. Gauthier, IBM
Semiconductor Process and Structural Optimization of Shallow Trench Isolation- Defined and Polysilicon – Bound Source/Drain Diodes for ESD Networks

V. Gupta, A. Amerasekera, S. Ramaswamy, A. Tsai, Texas Instruments, Inc.
ESD-Related Process Effects in Mixed-Voltage Sub-0.5 μm Technologies

S. Notermans, P. de Jong, F. Kuper, Philips Semiconductors
Pitfalls When Correlating TLP, HBM, and MM Testing

C. Russ, K. Boek, M. Rasras, I. De Wolf, G. Groeseneken, H. Maes, IMEC
Non-Uniform Triggering of gg-nMOS Investigated by Combined Emission Microscopy and Transmission Line Testing

P. Salome, STMicroelectronics; C. Leroux, CEA Technologies Avancees; P. Crevel, MHS-Route de Gachet; J. P. Chante, CEGELY-ECFA-INSIA
Investigations on the Thermal Behavior of Interconnects Under ESD Transients Using a Simplified Thermal RC Network

T. Suzuki, S. Sekino, S. Ito, H. Monma, Fujitsu Limited
ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate

S. Sinha, H. Swaminathan, G. Kadamati, C. Duvvury, Texas Instruments, Inc.
An Automated Tool for Detecting ESD Design Errors

I. Omar, Motorola
Charge Trap Phenomena on EPROM Device – Methodology to Identify the Cause of the Problem in IC Manufacturing Process to Improve Electrical Test Yield

G. Beebe, Advanced Micro Devices
Simulation of Complete CMOS I/O Circuit Response to CDM Stress

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Substrate Resistance Modeling and Circuit-Level Simulation of Parasitic Device Coupling Effects for CMOS I/O Circuits Under ESD Stress
A. Sticker, W. Fichtner, Swiss Federal Institute of Technology; S. Mettler, M. Mergens, W. Wilkening, Robert Bosch GmbH; H. Wolf, H. Gieser, Fraunhofer-Institut Festkörpertechnologie; K. Bock, IMEC; L.G. Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations

Henry, ORYX Instruments Corporation; T. Meuse, Key

M. Chaine, Texas Instruments, Inc.; K. Verhaege, L. Avery, Sarnoff Corporation: M. Kelly, Delphi Delco Electronics Systems; H. Gieser, IFT Fraybgifer Ubstutyte Festkorpertechnologie; K. Bock, IMEC; L.G. Investigation into Socketed CDM (SDM) Tester Parasitics

Henry, ORYX Instruments Corporation; T. Meuse, KeyTe

C. Chu, E Worley, Rockwell Semiconductor Systems

Ultra Low Impedance Transmission Line Tester

A. Kagerer, T. Brodbeck, Siemens AG

Influence of the Device Package on the Results of CDM Tests – Consequences for Tester Characterization and Test Procedure

J. Himple, R. Bailey, J. Hogue, R. Mckenzie, T. Porter, W. Boone, Maxtor Corporation; A. Fishman, Guzik Enterprises

Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing

D. Olson, C. Chang, Seagate Technology

Ion Milling Induced ESD Damage During MR Head Fabrication

F. Goceman, M. Szymanski, MKE-Quantum Corporation LLC; J. Salosbury, M. Sanchez, Semtronics Corporation

Evaluation of Wrist Strap Monitors from an MR Head Perspective

L. Zhu, Headway Technologies, Inc.

ESD Prevention on an Unshunted MR Head

C. Lam, C. Chang, R. Katimi, Read-Rite Corporation

A Study of ESD Sensitivity of AMR and GMR Recording Heads

A. Wallash, Quantum Corporation; D. Smith, Auspex Corporation

Electromagnetic Interference (EMI) Damage to Giant Magnetoresistive (GMR) Recording Heads

L. Levit, Ion Systems; A. Wallash, Quantum Corporation

Measurement of the Effects of Ionizer Imbalance and Proximity to Ground in MR Head Handling

M. Mergens, W. Wilkening, S. Mettler, Robert Bosch GmbH, H. Wolf, Fraunhofer-Institut (IZM), A. Stricker, W. Fichtner, Swiss Federal Institute of Technology (ETHZ)

Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions

G. Boselli, T. Mouthaan, University of Twente; F. Kuper, S. Meeuwsen, Philips, Semiconductors Nijmegen

Investigations on Double-Diffused MOS (DMOS) transistors under ESD zap conditions

H. Gossner, T. Muller-Lynch, K. Esmark, M. Stecher, Infineon Technologies

Wide Range Control of the Sustaining Voltage of ESD Protection Elements Realized in a Smart Power Technology

H. Wolf, Technische Universität München; H. Gieser, Fraunhofer-Institute Zuverlässigkeit in der Mikrosystemtechnik; W. Wilkening, Robert Bosch GmbH

Analyzing the Switching Behavior of ESD-Protection Transistors by Very Fast Transmission Line Pulsing

K.P. Cheung, Bell Laboratories, Lucent Technologies

Invited Paper: Plasma-charging damage and ESD, help each other?

R. Ford-Smith, Ion Systems; H. Barnett, G. Leal, G. Sutorius, Motorola

A Study of ESD Induced Lockups in a Semiconductor Photolithography Area

R. Gompf, NASA; P. Holdstock, British Textile Technology Group; J. Chubb, John Chubb Instrumentation

Electrostatic Test Methods Compared

K. Davies, MARKAB; S. Gerken, USAF

Charging and Ignition of Sprayed Fuel
<table>
<thead>
<tr>
<th>Page</th>
<th>Authors</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>99062</td>
<td>J. Smith, Motorola</td>
<td>An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events</td>
</tr>
<tr>
<td>99070</td>
<td>T. Maloney, W. Kan, Intel Corporation</td>
<td>Stacked PMOS Clamps for High Voltage Power Supply Protection</td>
</tr>
<tr>
<td>99095</td>
<td>K. Bock, B. Keppens, V. De Heyn, G. Groeseneken, IMEC; L.Y. Ching, A. Naem, National Semiconductor</td>
<td>Influence of gate length on ESD-performance for deep sub micron CMOS technology</td>
</tr>
<tr>
<td>99105</td>
<td>S. Voldman, D. Hui, L. Warriner, D. Young, J. Howard, F. Assaderaghi, G. Shahidi, IBM</td>
<td>Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips</td>
</tr>
<tr>
<td>99116</td>
<td>K. Narita, Y. Horiguchi, K. Hayano, K. Suzuki, NEC Corporation</td>
<td>A Simulation Analysis of Quarter-Micron CMOS LSI Input Circuit Behavior under CDM-ESD for Protection Device Improvement</td>
</tr>
<tr>
<td>99131</td>
<td>C.G. Noll, ITW Static Control and Air Products</td>
<td>Balanced Static Elimination in Variable Ion Mobility Environments</td>
</tr>
<tr>
<td>99145</td>
<td>R. Vermillion, ARP Engineering; L. Fromm, Hewlett-Packard Company</td>
<td>A Study of ESD Corrugated</td>
</tr>
<tr>
<td>99155</td>
<td>L. Seng, Siemens Components (AT) Sdn. Bhd.</td>
<td>Conductive Floor and Footwear System as Primary Protection Against Human Body Model ESD Event</td>
</tr>
<tr>
<td>99160</td>
<td>Y. Anand, D. Crowe, M/A-Com Inc.</td>
<td>Latent ESD Failures in Schottky Barrier Diodes</td>
</tr>
<tr>
<td>99178</td>
<td>M. Kelly, Delphi Delco Electronics Systems; L.G. Henry, ORYX Instruments Corporation; J. Barth, Barth Electronics, Inc.; G. Weiss, Lucent Technologies; M. Chaine, Micron Technology, Inc.; H. Gieser, D.</td>
<td>Developing a Transient InducedLatch-up Standard for Testing Integrated Circuits</td>
</tr>
<tr>
<td>99190</td>
<td>I. Morgan, M. Mahanpour, Advanced Micro Devices; C. Hatchard, ORYX Instruments Corporation</td>
<td>TransientLatch-Up Using an Improved Bi-polar Trigger</td>
</tr>
<tr>
<td>99203</td>
<td>L.G. Henry, ORYX Instruments Corporation; M. Kelly, Delphi Delco Electronics Systems; T. Diep, Texas Instruments; J. Barth, Barth Electronics</td>
<td>Issues Concerning CDM ESD Verification Modules-The Need to Move to Alumina</td>
</tr>
<tr>
<td>99225</td>
<td>T. Ikehashi, K. Imamiya, K. Sakui, Toshiba Corporation</td>
<td>Design Methodology of a Robust ESD Protection Circuit for STI Process 256Mb NAND Flash Memory</td>
</tr>
<tr>
<td>99235</td>
<td>C. Chu, G.P. Li, University of California; W.J. Ho, H.Y. Hsu, T-M Kao, C. Hua, D. Day, Network Device, ESD Performance Optimization of Ballast Resistor On Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology</td>
<td></td>
</tr>
</tbody>
</table>
Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices

Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing

Investigating the Performance of Conductive Thick Epoxy Floors

Processable ESD Control Materials Filled With Tunable Intrinsically Conductive Polymer Nanocomposites

Effects of Aging, Wiping and Humidity on Surface Resistivity of Polyethylene and Polypropylene

Development of Accelerated Aging Test for ESD/EMI Protective Materials and Electrical Discontinuity at Seams and Interconnections

Electrostatic Discharge (ESD) Mechanism for Battery Charge Contact Failure in Cordless Phones

Fields and ESD Risk from Charged Object Introduction into Hard Drives

ESD Testing of Head Stack Assemblies Used in Magnetic Recording Hard Disk Drives

The Real CDM Field Induced ESD Waveform from MR Heads

ESD Testing of GMR Heads as a function of Temperature

ESD Protection of GMR Heads in Manufacturing

Analysis of the Electrical Field Effects of AC and DC Ionization Systems for MR Head Manufacturing

Unusual Forms of ESD and Their Effects

An Improved Model of Man for ESD Applications

Investigation of a Test Methodology for Triboelectrification

Hardware/Firmware Co-Design in an 8-Bits Microcontroller to Solve the System-Level ESD Issue on Keyboard

Using HGA Antennas to Measure EMI; Establishing and Correlating Damage Thresholds of GMR Heads

ESD Damage by Directly Arcing to a MR Head

A Study of Head Stack Assembly Sensitivity to ESD

ESD Damage of GMR Sensors at Head Stack Assembly

A Study of Diode Protection for Giant Magnetoresistive Recording Heads
C. Lam, D. Martinez, C. Chang, Read-Rite Corporation
ESD Sensitivity Study of GMR Recording Heads with a Flex-On-Suspension Head-Gimbal Assembly

K. Yokoi, T. Watanabe, NEC Corporation
Invited Paper: A Study of Wafer Level ESD Testing

C. Duvvury, S. Ramaswamy, A. Amerasekera, R. Cline, B. Andresen, V. Gupta, Texas Instruments
Substrate Pump NMOS for ESD Protection Applications

K. Verhaege, C. Russ, Sarnoff Corporation
Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices

S. Voldman, J. Howard, M. Sherony, F. Assaderaghi, IBM Semiconductor Research and Development Center;
D. Hui, D. Young, D. Dreps, IBM Corporation; G. Shahidi, IBM T.J. Watson Research Center
Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

H. Hyatt, Littelfuse, Inc. and Hyger Physics, Inc.; J. Harris, J. Colby, Littelfuse, Inc.; P. Bellew, Littelfuse, Ireland Ltd.
Optimizing The Performance of a Composite ESD Circuit Protection Device

D. Smith, D.C. Smith Consultants; E. Nakauchi, Garwood Laboratories, Inc.
ESD Immunity in System Designs, System Field Experiences and Effects of PWB Layout

W. Greason, University of Western Ontario
Generalized Model of Electrostatic Discharge (ESD) for Bodies in Approach: Analyses of Multiple Discharges and Speed of Approach

J. Muñoz, J. Tan, C. Adriano, E. Roldan, Intel Technology Philippines Incorporated
Detecting ESD Events using a Loop Antenna

T. Brodbeck, Infineon Technologies AG
Influence of the Charging Effect on HBM ESD Device Testing

L.G. Henry, EDS/TLP Consulting; M. Kelly, Delphi Delco Electronics Systems; T. Diep, Texas Instruments; J. Barth, Barth Electronics, Inc.
The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation

J. Barth, J. Richner, Barth Electronics Inc; K. Verhaege, Sarnoff Corporation; L.G. Henry, ESD/TLP Consultant
TLP Calibration, Correlation, Standards, and New Techniques

J. Lee, M. Hoque, J. Liou, University of Central Florida; G. Croft, W. Young, J. Bernier, Intersil Corporation
A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods

M. Lee, C. Liu, C-C Lin, J-T Chou, H. Tang, Y. Chang, K. Fu, United Microelectronics Corp.
Comparison and Correlation of ESD HBM (Human Body Model) Obtained Between TLP, Wafer-Level, and Package-Level Tests

H. Hyatt, Littelfuse & Hyger Physics, Inc.; J. Harris, A. Alanzo, Littelfuse, Inc.; P. Bellew, Littelfuse Ireland
TLP Measurements for Verification of ESD Protection Device Response

R. Rosner, 3M Electronics Handling & Protection Division
Invited Paper: Conductive Materials for ESD Applications: An Overview

K. Kim, N. Hardwick, H. Pham, T. Fahey, BFGoodrich Static Control Polymers
Advancements in Inherently Dissipative Polymer (IDP) Alloys Provide New Levels of Clean, Consistent ESD Protection

M. Narkis, Technion – Institute of Technology; G. Lidor, A. Vaxman, L. Zuri, Carmel Olefins Ltd.
Controlling ESD and Cleanliness by Using New Thermoplastic Compounds for Injection Molded and Corrugated Packaging Products

H. Uchida, H. Kurosaki, T. Numaguchi, Sumitomo 3M Limited
New Methods for Measuring Resistance and Charge decay of Worksurfaces

C. Extrand, Entegris
Mechanical and Electrical Properties of Poly (ether ether ketone) (PEEK) with Various Conductive Fillers

T. Lesniewski, K. Yates, TRW Space and Electronics Group
Evaluation of Materials Used in Cleanrooms with ESD Sensitive Hardware
E. Granstrom, N. Tabat, Seagate Recording Head Operations

Limitations of the Adiabatic Model for ESD Failure in GMR Structures

R. Bordeos, J. Kagaoan, Shenzhen Kaifa Technology Co. Ltd.

A Case Study on Hidden ESD Events of GMR HGA Dynamic Test Fixture

H. Snyder, Technical Consulting Associates; A. Wallash, Quantum Corporation

A Study of Methods to Eliminate Metal Contact in GMR Head Manufacturing

N. Jacksen, ExMod Corporation; L. Nelsen, D. Boehm, Novx Corporation; T. Odom, VCD Technologies

Advances in Magneto Optical Static Event Detector Technology

F. Zhao, R. Tao, H. Tian, SAE Magnetics (HK) Ltd.

The Effect of Bonding Sequence on GMR ESD Protection

D. Nordin, Quantum Corporation

HDA-Level ESD Testing of Giant Magnetoresistive (GMR) Recording Heads

D. Vickers, D. Carradero, Quantum Corporation

Evaluation of Tribocharging and ESD Protection Schemes on GMR Magnetic Recording Heads During CO2 Jet Cleaning

W. Ogle, C. Moore, Integral Solutions, Int’l.

Measuring and Specifying Limits on Current Transients and Understanding Their Relationships to MR Head Damage

V. Kraz, Credence Technologies, Inc.; A. Wallash, Quantum Corporation

The Effects of EMI from Cell Phones on GMR Magnetic Recording Heads and Test Equipment

B-C Yap, Western Digital (Malaysia) Sdn. Bhd.; C. Patton, Senergy Co.

Investigation of ESD Transient EMI Causing Spurious Clock Track Read Transitions During Servo-Write

S. Voldman, N. Schmidt, R. Johnson, L. Lanzerotti, A. Joseph, C. Brennan, J. Dunn, D. Harame, IBM Semiconductor Research and Development Center; P. Juliano, E. Rosenbaum, University of Illinois at Urbana-Champaign; B. Meyerson, IBM T.J. Watson Reserch

Electrostatic Discharge Characterization ofEpitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors


Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 µm CMOS Process

H. Koizumi, Y. Komine, Y. Ohtomo, M. Shimaya, NTT Telecommunications Energy Laboratories

ESD Protection in Fully-Depleted CMOS/SIMOX with a Tungsten-Clad Source/Drain

T. Wang, Sunplus Technology Co. Ltd.; M-D Ker, National Chiao-Tung University

On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Applications

G. Groeseneken, IMEC

Invited Paper: Hot Carrier Degradation and ESD in Submicron CMOS Technologies: How Do They Interact?

J. Wu, P. Juliano, E. Rosenbaum, University of Illinois at Urbana-Champaign

Breakdown and Latent Damage of Ultra-Thin Gate Oxides under ESD Stress Conditions

E. Worley, A. Salem, Y. Sittampalam, Conexant Systems

High Current Characteristics of Devices in a 0.18 µm CMOS Technology

J. Miller, M. Khazhinsky, J. Weldon, Motorola, Inc.

Engineering the Cascoded NMOS Output Buffer for Maximum Vt1

B. Perry, Maxtor Corporation

ESD Damage Thresholds: History and Prognosis

D. Guarisco, M. Li, Maxtor Corporation

ESD Sensitivity of GMR Heads at Variable Pulse Length
R. Tao, FG Zhao, SAE Magnetics (HK) Ltd.  
**Threshold of ESD Damage to GMR Sensor**

M. Honda, Impulse Physics Laboratory, Inc.  
**Charge Induction on GMR Recording Heads Caused by AC Power Fields**

L. Henry, ESD/TLP Consultant; A. Wallash, Quantum Corporation  
**Considerations for an HBM ESD Standard for Measuring and Testing of Magneto Resistive Heads**

C. Moore, Integral Solutions, Int’l.  
**A Comparison of Quasi-Static Characteristics and Failure Signatures of GMR Heads subjected to CDM and HBM ESD Events**

A. Wallash, Quantum Corporation  
**In-situ Spin Stand ESD Testing of Giant Magneto resistive (GMR) Recording Heads**

Y. Shen, R. Leung, J. Sun, SAE Magnetics (HK) Ltd.  
**Baseline Popping of Spin-Valve Recording Heads Induced by ESD**

D. Swenson, 3M Electronics Handling & Protection Division  
**Invited Paper: ESD Control in the Factory of the Future or 20.20 to the Rescue**

B. Unger, Burt Unger Associates  
**Device Charging in Shipping Packages**

D. Stockin, Lyncole Industries, Inc.  
**Designing and Testing of Facilities Ground**

J. Franey, Lucent Technologies Bell Labs  
**Corrosion Induced Electrostatic Damage**

A. Rudack, M. Pendley, International SEMATECH; L. Levit, Ion Systems  
**Measurement Technique Developed to Evaluate Transient EMI in a Photo Bay With and Without Air Ionization**

Y. Anand, D. Crowe, A. Feinberg, C. Jones, M/A-COM, Incorporated  
**Random GaAs IC’s ESD Failures Caused by RF Test Handler**

J. Montoya, Intel Corporation; L. Levit, Ion Systems; A. Englisch, Dupont Photomasks  
**A Study of the Mechanisms for ESD Damage to Reticles**

**A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process**

K-L Lei, C. Chu, J. Tseng, Y-M Chiang, M. Young, Advanced Custom Sensors, Inc.; G. Li, University of California  
**ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors**

K. Esmark, W. Stadler, M. Wendel, H. Gößner, X. Guggenmos, Infineon Technologies AG; W. Fichtner, ETH Zurich  
**Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase**

Y. Wang, P. Juliano, S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign  
**Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies**

V. Puvvada, V. Srinivasan, V. Gupta, Texas Instruments (India) Ltd.  
**A Scalable Analytical Model for the ESD N-Well Resistor**

M. Mergens, Bosch (now with Sarnoff Corporation); W. Wilkening, G. Kiesewetter, S. Mettler, J. Hieber, Robert Bosch GmbH; H. Wolf, Fraunhofer-Institut für Zuverlässigkeit un Mikrointegration (IZM); W. Fichtner, Swiss Federal Institute of Technology (ETHZ)  
**ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior**

J. Lee, S. Kang, University of Illinois; Y. Huh, J-W Chen, P. Bendix, LSI Logic Corporation  
**Chip-Level Simulation for CDM Failures in Multi-Power ICs**

M. Baird, Arizona State University and Motorola; R. Ida, Motorola  
**Verify ESD: A Tool for Efficient Circuit Level ESD Simulations of Mixed-Signal ICs**
A. Wallash, J. Hillman, Quantum Corporation; D. Wang, Nonvolatile Electronics, Inc.
ESD Evaluation of Tunneling Magneto resistive (TMR) Devices

W. Lukaszek, Wafer Charging Monitors, Inc.
Wafer Charging in Process Equipment and Its Relationship to GMR Heads Charging Damage

E. Granstrom, R. Cermak, P. Tesarek, N. Tabat, Seagate Recording Head Operations
Floating Gate EEPROM as EOS Indicators During Wafer-Level GMR Processing

R. Bordeos, Z. Lianzhu, Shenzhen Kaifa Technology Co. Ltd.; S. Hung, C. Wong, The Hong Kong University of Science & Technology
Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach

C. Lam, Read-Rite Corporation
A Study of Static Dissipative Tweezers for Handling Giant Magneto-Resistive Recording Heads

D. Pritchard, Trek Incorporated
Electrostatic Voltmeter and Fieldmeter Measurements on GMR Recording Heads

S. Ramaswamy, J. Carter, J. Stubbart, A. Singh, R. Krasnick, MKPA/Panasonic; F. Gocemen, MKPA/Panasonic (now with Quantum Corporation)
Effect of InS to 250 mS ESD Transients on GMR Heads

Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling

K. Kunz, C. Duvvury, H. Shichijo, Texas Instruments, Inc.
5-V Tolerant Fail-Safe ESD Solutions for a 0.18µm Logic CMOS Process

GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes

M.D. Ker, C-H Chuang, National Chiao-Tung University; H-C Jiang, Industrial Technology Research Institute
ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device

J. Allen, VPI Mirrex Corporation
An Analysis of ESD Packaging Systems Through Thermoforming

J. Paasi, R. Vuorinen, P. Maijala, H. Palmen, VTT Automation; V. Salminen, Nokia Networks
Performance of Fiber Based ESD Protective Packaging

N. Nishihata, Kureha Chemical Industry Co., Ltd.
New ESD Control Material Based on Special Carbon

V. Vassilev, H. Maes, IMEC, KUL, ESAT; M. Lorenzini, G. Groeseneken, IMEC; M. Steyaert, KUL, ESAT
Analysis and Improved Compact Modeling of the Breakdown Behavior of Sub-0.25 Micron ESD Protection gGNMOS Devices

G. Boselli, University of Twente, Texas Instruments, Inc.; S. Ramaswamy, A. Amerasekera, Texas Instruments, Inc.; T. Mouthaan, University of Twente; F. Kuper, University of Twente, Philips
Modelling Substrate Diodes under Ultra High ESD Injection Conditions

C.A. Torres, J.W. Miller, M. Stockinger, M.D. Akers, M.G. Khazhinsky, J.C. Weldon, Motorola, Inc.
Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies

P. Ngan, D. Oliver, T. Smedes, Philips Semiconductors; R. Gramacy, University of California; C-K Wong, Kestrel Solutions
Automatic Layout Based Verification of Electrostatic Discharge Paths
2001102  R. Depetro, A. Andreini, C. Contiero, ST-Microelectronics; F. Mignoli, G. Meneghesso, E. Zanoni, University of Padova
Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology

2001110  A. Guilhaume, EADS CCR, CEGELY; B. Foucher, EADS CCR; J.P. Chante, CEGELY; P. Galy, Pole Universitaire Leonard De Vinci; S. Bardy, F. Blanc, Philips Semiconducteurs
Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test

2001112  J. Marley, D. Tan, Xilinx, Inc.; V. Kraz, Credence Technologies, Inc.
Controlling ESD Damage of ICs at Various Steps of Back-End Process

2001125  K-P Yan, R. Gaertner, S. Lim, Infineon Technologies (Malaysia) Sdn. Bhd.
An Effective ESD Protection System in the Back End (BE) Semiconductor Manufacturing Facility

2001133  T. Lesniewski, S. Hartooni, TRW Space & Electronics Group; E. Kaully, Kulicke & Soffia Industries, Inc.
Preparing a Microelectronics Assembly and Test Area for More Sensitive Product

2001141  D.G. Bellmore, Universal Instruments Corporation
Anodized Aluminum Alloys, Insulator or Not?

2001149  Y. Jaimsomporn, S. Phunyapinuant, W. Tan, Advanced Micro Devices
DC Transient Monitoring and Analysis to Prevent EOS in Burn-in Systems

2001153  C. Newberg, River’s Edge Technical Service
Measurement of Electrostatic Generation in Semiconductor Processing Fluids as a Result of Pumping Through Insulative Pumps and Tubing

2001160  B-C Yap, Western Digital (Malaysia) Sdn. Bhd.; J. Turangan, Western Digital
Field-Induced Charging and FIM ESD Tests on GMR Heads in Hard Disk Assembly

2001167  A. Wallash, Maxtor Corporation
A Study of Shunt ESD Protection for GMR Recording Heads

2001172  T. Ohtsu, H. Yoshida, N. Hatanaaka, Hitachi, Ltd.
Field Emission Noise Caused by Capacitance Coupling ESD in AMR/GMR Heads

2001175  S.T. Hung, C.Y. Wong, The Hong Kong University of Science & Technology; M. Osborn, Digital Instruments; J. Kagaoan, L.Z. Zhang, R. Bordeos, Shenzhen Kaifa Technology Co. Ltd.
A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping

2001182  J. Himle, Maxtor Corporation
Using PSPICE to Study Transient Propagation in GMR Circuits

2001187  I-F Tsu, M. Davis, C. Chang, Seagate Technology
Effect of Low-Level ESD on the Lifetime of GMR Heads

2001191  K. Banerjee, Stanford University Paper Not Available at Press Time
Invited Paper: Interconnect Reliability Under ESD Conditions: Physics, Models, and Design

2001192  C. Salling, J. Hu, J. Wu, C. Duvvury, R. Cline, R. Pok, Texas Instruments, Inc.
Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

2001205  R. Gauthier, M. Muhammad, C. Putnam, IBM Microelectronics Semiconductor Research and Development Center; W. Stadler, K. Esmark, P. Riess, Infineon Technologies AG; A. Salman, George Mason University
Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13µm CMOS Logic Technology

2001216  D. Pogany, M. Litzenberger, P. Kamvar, E. Gornik, Vienna University of Technology; C. Fürböck, Vienna University of Technology (now with Austria Microsystems) G. Groos, K. Esmark, H. Gossner, M. Stecher, Infineon Technologies
Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric Thermal Mapping Technique

Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection
Human Body Model, Machine Model, and Charged Device Model ESD Testing of Surface
Micromachined Microelectromechanical Systems (MEMS)

2001249 G. Meneghesso, A. Chini, A. Maschietto, E. Zanoni, University of Padova; P. Malberti, M. Ciappa, Swiss
Federal Institute of Technology (ETH)
Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

2001255 S.J. Dahman, RTP Company
Recent Innovations of Inherently Conducting Polymers for Optimal (106 – 109 OHM/SQ) ESD
Protection Materials

The Purity, Wetting, and Electrical Properties of Static-Dissipative Surfactant Coatings Versus
Inherently-Dissipative Polymer Alloys

2001267 H. Berndt, B.E.STAT
A Study of the Variables of Electrodes Used in the Measurement of Table and Floor Materials and
How They Affect the Test Results

2001272 J.M. Kolyer, A.A. Passchier, W.G. Peterson, The Boeing Company
Electronic Part Damage by Antistat Vapor

2001281 C. Newberg, River's Edge Technical Service, Inc.; B. Baumgartner, ESD West; G. Chase, S. Weitz, ETS,
Inc.; W. Casselman, QRP Incorporated; A. Hartkopf, Ansell Healthcare; T. Jarrett, Guidant Corp.; W.J. Metz,
Hewlett Packard; R.D. Rodrigo, SIMCO; J. Turan
A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

2001288 R.W. Welker, M. Schulman, Jet Propulsion Laboratory
Contact Transfer of Anions from Hands as a Function of the Use of Hand Lotions

2001291 A. Wallash, Maxtor Corporation
Transmission Line Pulse (TLP) Testing of GMR Recording Heads

2001295 F. Deng, Z.Y. Teng, W. Li, R. Tao, SAE Magnetics (HK), Ltd.
A Study of GMR Breakdown Damage in Cleaning

2001299 A. Siritaratiwat, N. Suwannata, Khon Kaen University; J. Pinnoi, C. Pupaichitkul, Seagate Technology
(Thailand) Ltd.
Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process

2001305 PAPER WITHDRAWN

Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test
Element Group

2001311 B. Perry, Maxtor Corporation
ESD Audit Limits and Actual Damage Thresholds: A Theoretical Analysis

2001318 J.S. Luo, C-Y Yeh, A. Sanayei, IBM
GMR Heads as ESD Detectors-A Direct Assessment of Subtle ESD

2001322 D.R. Pehlke, Ericsson, Inc.
Invited Paper: The Future of RF Technology for Established Wireless Markets and Emerging
Wireless Applications

2001326 S. H. Voldman, A. Botula, IBM Communications Research and Development Center; D. T. Hui, IBM
Corporation; P. A. Juliano, University of Illinois at Urbana-Champaign
Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit

2001337 R.M.D.A. Velghe, Philips Semiconductors Nijmegen (now with Philips Research Leuven); P.W.H. de
Vreede, P.H. Woerlee, Philips Research Laboratories Eindhoven
Diode Network Used as ESD Protection in RF Applications

2001346 M-D Ker, T-Y Chen, National Chiao-Tung University; C-Y Chang, Industrial Technology Research Institute
ESD Protection Design for CMOS RF Integrated Circuits

2001355 C. Ito, K. Banerjee, R.W. Dutton, Stanford University
Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and
RF Applications
2001364 S.H. Voldman, L.D. Lanzerotti, R.A. Johnson, IBM Communications Research and Development Center
Influence of Process and Device Design on ESD Sensitivity of a Silicon Germanium Heterojunction Bipolar Transistor

2001373 S. Bönisch, W. Kalkner, Technical University Berlin; D. Pommerenke, Hewlett Packard
Broadband Measurement of ESD Risetimes to Distinguish between Different Discharge Mechanisms

2001385 D.C. Smith, D.C. Smith Consultants; M. Hogsett, Ion Systems
The EMI/ESD Environment of Large Server Installations

2001390 J. Harris, Littelfuse, Inc.
Comparison of Solutions to Minimize Voltages Induced by ESD Events on Adjacent Microstrips

2001398 T.J. Maloney, D-H Cho, S.S. Poon, B. Lisenker, Intel Corporation
Improving the Balanced Coaxial Differential Probe for High-Voltage Pulse Measurements

2001408 W.D. Greason, Z. Kucerovsky, C. Zaharia, University of Western Ontario
Development of an Experimental Platform to Study the Effect of Speed of Approach on the Electrostatic Discharge (ESD) Event

2001415 J. Huang, Q. Deng, F. Liu, Z. Chen, P. Liu, Beijing Research Institute of Special Electromechanical
Electromagnetic Field Generated by Transient Electrostatic Discharges (ESD) from Person Charged with Low Electrostatic Voltage

2001419 K. Kato, Y. Fukuda, OKI Electric Industry Co., Ltd.
Invited Paper: ESD Evaluation by TLP Method on Advanced Semiconductor Devices

The Application of Transmission Line Pulse Testing for the ESD Analysis of Integrated Circuits

2001435 R.A. Ashton, Y. Smooha, Agere Systems
Characterization of a 0.16um CMOS Technology using SEMATECH ESD Benchmarking Structures

2001445 L-M Ting, C. Duvvury, O. Trevino, J. Schichl, T. Diep, Texas Instruments
Integration of TLP Analysis for ESD Troubleshooting

2001453 J. Barth, J. Richner, Barth Electronics, Inc.
Correlation Considerations: Real HBM to TLP and HBM Testers

2001461 B. Keppens, V. De Heyn, M. Natarajan Iyer, G. Groeseneken, Imec vzw
Contributions to Standardization of Transmission Line Pulse Testing Methodology

2002001 S. S. Poon, T. J. Maloney, Intel Corporation
New Considerations for MOSFET Power Clamps

2002006 Y. Morishita, NEC Corporation
New ESD Protection Circuits Based on PNP Triggering SCR for Advanced CMOS Device Applications

High Holding Current SCRs (HHI-SCR) for ESD Protection andLatch-up Immune IC Operation

A 6mW, 1.5dB NF CMOS LNA for GPS with 3kV HBM ESD-Protection

Sources of Impulsive EMI in Large Server Farms

2002032 D. C. Smith, D. C. Smith Consultants; A. Wallash, Maxtor Corporation
Electromagnetic Interference (EMI) Inside a Hard Disk Drive Due to External ESD

2002037 W. D. Greason, University of Western Ontario
Experimental Investigation of the Electrostatic Discharge (ESD) Characteristics for the Charged Human Body Handling Circuit Packs

2002047 M. Honda, Impulse Physics Laboratory, Inc.
A Study of Flip-Flop IC Upset Exposed by ESD Radiated Fields

2002052 S. Voldman, IBM Communications Research and Development Center (CRDC)
Variable-Trigger Voltage ESD Power Clamps for Mixed Voltage Applications Using a 120 GHz/100 GHz (fT/fMAX) Silicon Germanium Heterojunction Bipolar Transistor with Carbon Incorporation
2002233  K. S. Suh, J. E. Kim, Korea University and InsCon Tech.; T. Y. Kim, Korea University; K. S. Moon, H. S. Moon, Y. K. Park, Samsung Electronics  
ESD Protection Materials Using Conductive Polymers

2002240  T. Terashige, Hiroshima International University; D. Ohashi, K. Okano, The Polytechnic University  
Noise Reduction of Corona Discharge Air Ionizer

2002245  P. Gefter, Ion Systems  
Biological Aspects of Clean-Room Ionization

2002250  J. Passi, P. Tamminen, T. Kalliohaka, H. Kojo, K. Tappura, VTT Industrial Systems  
ESD Control Tools for Surface Mount Technology and Final Assembly Lines

2002257  G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.  
Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 ?m ESD Protection Circuits

2002259  J. van Zwol, A. van den Berg, T. Smedes, Philips Semiconductors  
ESD Protection by Keep-On Design for a 550 V Flourescent Lamp Control IC with Integrated LDMOS Power Stage

Effect of the n+Sinker in Self-Triggering Bipolar ESD Protection Structures

2002281  D. Tremouilles, LAAS-CNRS and ON Semiconductor; G. Bertrand, L. Lescouzere, ON Semiconductor; M. Bafleur, N. Nolhier, LAAS-CNRS  
Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN

2002289  S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign  
Compact Modeling of Vertical ESD Protection NPN Transistors for RF Circuits

2002296  S. Voldman, S. Strang, D. Jordan, IBM Communications Research and Development Center (CRDC)  
An Automated Electrostatic Discharge Computer-Aided Design System with the Incorporation of Hierarchical Parameterized Cells in BiCMOS Analog and RF Technology For Mixed Signal Applications

2002306  T. Cheung, ReadRite Corporation; L. Baril, A. Wallash, Maxtor Corporation  
Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads I

2002315  L. Baril, A. Wallash, Maxtor Corporation; T. Cheung, ReadRite Corporation  
Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads II

2002321  R. Bordeos, Shenzhen Kaifa Technology Co. Ltd.  
The Practical Approach of ESD Control Solution in Headstack Assembly (HSA) Manufacturing

2002326  B. Perry, T. Porter, W. Boone, Maxtor Corporation  
Impact of Insulating “Conductive” Materials on Disk Drive ESD Robustness

2002332  Z. Y. Teng, Y. G. Wang, W. Li, R. Tao, SAE Magnetics (HK) Ltd.  
ESD Damage by Arcing near GMR Heads

2002337  A. Lai, SAE Magnetics (HK) Ltd.; A. Wallash, Maxtor Corporation  
Effect of GMR Recording Head Resistance on Human Body and Machine Model ESD Waveforms

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Study for Recovery Process of Damaged Al2O3 during Ion Milling to Increase Tolerance to ESD

2002348  P. Besse, LAAS-CNRS and Motorola Semiconductors Toulouse; M. Zelcri, Motorola Semiconductors Toulouse; N. Nolhier, M. Bafleur, LAAS-CNRS; Y. Chung, Motorola Semiconductors  
Investigations for a Smart Power and Self-Protected Device Under ESD Stress Through Geometry and Design Considerations for Automotive Applications

2002354  T. Smedes, J. van Zwol, P. C. de Jong, Philips Semiconductors; A. Heringa, Philips Research Laboratories  
The Impact of Substrate Resistivity on ESD Protection Devices

2002362  B-C Jeon, S-C Lee, J-K Oh, S-S Kim, M-K Han, Seoul Nat’l University; Y-I Jung, H-T So, J-S Shim, K-H Kim, Hynix Semiconductor Inc.  
ESD Characterization of Grounded-Gate NMOS with 0.35 ?m/18 V Technology Employing Transmission Line Pulser (TLP) Test

2002373  B. Lisenker, Intel Israel  
Process Influence on Product CDM ESD Sensitivity
**Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD**

**Investigation of ESD Protection Elements Under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry**

2003008 J. C. Smith, G. Boselli, Texas Instruments, Inc. 
**A MOSFET Power Supply Clamp with Feedback Enhanced Triggering for ESD Protection in Advanced CMOS Technologies**

**Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies**

2003027 T. J. Maloney, S. S. Poon, L. T. Clark, Intel Corporation 
**Methods for Designing Low-leakage Power Supply Clamps**

2003034 A. Olney, B. Gifford, J. Guravage, A. Righter, Analog Devices, Inc. 
**Real-World Charged Board Model (CBM) Failures**

2003044 E. Grund, Oryx Instruments Corp. 
**A Wafer Level HBM Tester Delivering Pulses with Variable Risetime through Transmission Lines**

2003051 J. van Zwol, W. Kemper, P. Bruin, Philips Semiconductors 
**Transmission Line Pulsed Photo Emission Microscopy as an ESD Troubleshooting Method**

**ESD Protection Design Challenges for a High Pin-Count Alpha Microprocessor in a 0.13µm CMOS SOI Technology**

2003070 M. Chaine, J. Davis, A. Kearney, Micron Technology, Inc. 
**TLP Analysis of 0.125µm CMOS ESD Input Protection Circuit**

2003080 S. Bargstädt-Franke, W. Stadler, K. Esmark, M. Streibl, K. Domanski, Infineon Technologies; H. Gieser, H. Wolf, IZM-Fraunhofer; W. Bala, Nicholaus Copernicus University 
**Transient Latch-up:Experimental Analysis and Device Simulation**

**Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress**

2003098 R. M. Steinhoff, J.-B. Huang, P. L. Hower, J. S. Brodsky, Texas Instruments, Inc. 
**Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor**

2003108 T. Smedes, Y. Li, Philips Semiconductors 
**ESD Phenomena in Interconnect Structures**

2003116 M. Graf, F. Dietz, V. Dudek, Atmel; S. Bychikhin, D. Pogany, E. Gornik, Vienna University of Technology; W. Soppa, FH Osnabrück; H. Wolf, Fraunhofer-IZM 
**Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness**

**High Abstraction Level Permutational ESD Concept Analysis**

2003131 W. D. Greason, University of Western Ontario 
**On the Development of Passive/Active Guard Electrode Systems for Human Body Electrostatic Discharge (ESD) Control**

2003137 K. Suzuki, M. Sato, Fab Solutions, Inc. 
**Advanced Technology for Monitoring Plasma Sparking ESD Damage using High Frequency Magnetic Wave Sensors**

**ESD Sensitivity of Devices on a Charged Printed Wiring Board**
<table>
<thead>
<tr>
<th>Paper No.</th>
<th>Authors</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>2003151</td>
<td>J. Paasi, H. Salmela</td>
<td>New Methods for the Assessment of ESD Threats to Electronic Components</td>
</tr>
<tr>
<td>2003161</td>
<td>D. Pirici, J. Rivenc, A. Agneray</td>
<td>A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach</td>
</tr>
<tr>
<td>2003169</td>
<td>M. Honda</td>
<td>Characteristics of Unipolar Impulsive Fields from a Nearby ESD Source</td>
</tr>
<tr>
<td>2003173</td>
<td>K. Kawamata</td>
<td>4.5GHz Measurement of Transition Duration and Frequency Spectra Due to Small Gap Discharge as Low Voltage ESD</td>
</tr>
<tr>
<td>2003179</td>
<td>J. Barth, J. Richner</td>
<td>Real HBM &amp; MM - The dV/dt Threat</td>
</tr>
<tr>
<td>2003188</td>
<td>S. Hyvonen</td>
<td>Comprehensive ESD Protection for RF Inputs</td>
</tr>
<tr>
<td>2003195</td>
<td>V. Vassilev</td>
<td>The Effect of Deep Trench Isolation, Trench Isolation and Sub-collector Doping on the Electrostatic Discharge (ESD) Robustness of Radio Frequency (RF) ESD STI-Bound P+/N-Well Diodes in BiCMOS Silicon Germanium Technology</td>
</tr>
<tr>
<td>2003204</td>
<td>S. Joshi</td>
<td>A Study of Vertical SiGe Thyristor Design and Optimization</td>
</tr>
<tr>
<td>2003233</td>
<td>B. Caillard</td>
<td>STMSCR: A New Multi-Finger SCR-Based Protection Structure Against ESD</td>
</tr>
<tr>
<td>2003242</td>
<td>S. Thijs</td>
<td>STMicroelectronics Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design</td>
</tr>
<tr>
<td>2003250</td>
<td>B. Keppens</td>
<td>Exploring a Clean ESD Laminate &amp; Ionic Contamination Methodology</td>
</tr>
<tr>
<td>2003259</td>
<td>A. C. Rudak</td>
<td>Creating and Measuring Photomask Damage</td>
</tr>
<tr>
<td>2003265</td>
<td>B.-C. Yap</td>
<td>Flue Gas Cleaning Using Wet-Type Electrostatic Precipitator</td>
</tr>
<tr>
<td>2003271</td>
<td>J. Crowley</td>
<td>Biased-Plate Characterization of Pulsed DC Ionizers</td>
</tr>
<tr>
<td>2003280</td>
<td>L. Dong</td>
<td>Exploring a Clean ESD Laminate &amp; Ionic Contamination Methodology</td>
</tr>
<tr>
<td>2003285</td>
<td>J. Crowley</td>
<td>Flue Gas Cleaning Using Wet-Type Electrostatic Precipitator</td>
</tr>
<tr>
<td>2003291</td>
<td>J. G. Neteler</td>
<td>Biased-Plate Characterization of Pulsed DC Ionizers</td>
</tr>
<tr>
<td>2003300</td>
<td>P. Holdstock</td>
<td>Test Procedures for Predicting Surface Voltages on Inhabited Garments</td>
</tr>
</tbody>
</table>
2003306  S. J. Dahman, RTP Company
   All Polymeric Compounds: Conductive and Dissipative Polymers in ESD Control Materials

2003313  N. Jensen, M. Denison, M. Stecher, Infineon Technologies; G. Groos, University of the Federal Armed Forces; J. Kuznik, D. Pogany, E. Gornik, Vienna University of Technology
   Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications

2003319  W. Stadler, K. Esmark, Infineon Technologies; K. Reynders, M. Zubeidat, AMIS; M. Graf, Atmel; W. Wilkening, J. Willemen, N. Qu, S. Mettler, M. Etherton, Robert Bosch GmbH; D. Nuernbergk, H. Wolf, H. Gieser, Fraunhofer-IZM; W. Soppa, FH Osnabrück; V. De He
   Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

2003328  H. A. Gieser, H. Wolf, W. Soldner, H. Reichl, Fraunhofer-IZM; A. Andreini, STMicroelectronics; M. I. Natarajan, IMEC; W. Stadler, Infineon Technologies
   A Traceable Method for the Arc-free Characterization and Modeling of CDM-Testers and Pulse Metrology Chains

2003338  H. Wolf, H. Gieser, Fraunhofer-IZM; W. Stadler, Infineon Technologies AG; W. Wilkening, Robert Bosch GmbH
   Capacitively Coupled Transmission Line Pulsing CC-TLP - A Traceable and Reproducible Stress Method in the CDM-Domain

2003346  S. Hyvonen, S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign
   Combined TLP/RF Testing System for Detection of ESD Failures in RF Circuits

2003354  E. Grund, Oryx Instruments Corp.; R. Gauthier, IBM Microelectronics
   TLP Systems with Combined 50 and 500-ohm Impedance Probes and Kelvin Probes

2003364  S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign
   Transmission Line Pulsed Waveform Shaping with Microwave Filters

2003372  In memory of Hugh Hyatt  S. H. Voldman, IBM Microelectronics; R. Ashton, B. McCaffrey, White Mountain Labs, Inc.; J. Barth, Barth Electronics, Inc.; D. Bennett, M. Hopkins, Thermo KeyTek; J. Bernier, Intersil Corp.; M. Chaine, Micron Technology, Inc.; J.
   Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

2003382  J. Matsugi, T. Nakano, Y. Mizoh, K. Nakamura, Matsushita-Kotobuki Electronics Industries; H. Sakakima, Matsushita Electric Industrial
   ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads

2003389  S. Kawata, T. Nakajima, Alps Electric Co. Ltd.
   A Consideration about Ionizer Balance in HGA Process

2003394  A. Wallash, Maxtor Corporation
   Continuous Voltage Monitoring Techniques for Improved ESD Auditing

2003402  T. Ohtsu, K. Kataoka, A. Morinaga, S. Natori, Hitachi Global Storage Technologies
   Study on Magnetic Instability of GMR Heads Using Quasi-Static Tester with Laser Heating Function

2003407  A. Wallash, Maxtor Corporation
   ESD SPICE Model and Measurements for a Hard Disk Drive

2003414  J. Salisbury, G. Stuckert, N. R. Oswald, R. L. Meyer, Seagate Technology
   Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies

2003419  L. Baril, A. Wallash, D. Guarisco, Maxtor Corporation
   Effect of ESD Transients on Noise in GMR Recording Heads

2003426  Y. Soda, Sony Corporation; S. Koike, Tokyo Electronics Trading Co., M. Honda, Impulse Physics Laboratory, Inc.
   Discharge Current and Electric Field Radiated from a Small Capacitance Device

2004001  A. Wallash, L. Baril, Maxtor Corporation; V. Kraz, T. Gurga, Credence Technologies
   Electromagnetic Field Induced Degradation of Magnetic Recording Heads in a GTEM Cell

2004008  R. J. Money, R&D Money Company; C. Coureau, Saint Gobain High Performance Materials; W. Boone, Hemisphere Static Solutions; A. Wallash, Maxtor Corporation
   Wire Bonding Tip Study for Extremely ESD Sensitive Devices

2004016  Y. Mizoh, T. Nakano, K. Tagashira, K. Nakamura, T. Suzuki, Matsushita-Kotobuki Electronics Industries,
   Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process
2004024  K. Suzuki, M. Sato; Fab Solutions, Inc.
Nanotransient Current and Transient Resistance on the Conductive or Dissipative Materials for Extremely Sensitive Devices

2004032  M-D Ker, B-J Kuo; National Chiao-Tung University
Optimization of Broadband RF Performance and ESD Robustness by \( \alpha \)-model Distributed ESD Protection Scheme

ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions

2004050  Y. Ma, Rockwell Scientific; G. P. Li, University of California
InGaP/GaAs HBT DC-20 GHz Distributed Amplifier with Compact ESD Protection Circuits

2004057  S. H. Voldman, E. G. Gebreselasie, IBM Microelectronics
Low-Voltage Diode-Configured SiGe:C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (\( f_T/f_{MAX} \)) SiGe:C HBT Device

2004067  W. Stadler, S. Bargstädt-Franke, T. Brodbeck, R. Gaertner, M. Goroll, H. Goßner, N. Jensen, Chr. Müller, Infineon Technologies AG
From the ESD Robustness of Products to the System ESD Robustness

2004075  N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, K. Machida, NTT Microsystem Integration Laboratories
Evaluation of ESD Hardness of Fingerprint Sensor LSIs

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Induced ESD on Metal Object with a Small Air Gap

2004088  K. Shrier, T. Truong, J. Felps, Electronic Polymer, Inc.
Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance

Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies

Study of CDM Specific Effects for a Smart Power Input Protection Structure

2004117  V. A. Vashchenko, W. Kindt, M. ter Beek, P. Hopper, National Semiconductor Corporation
Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application

ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices

2004132  C. Duuvury, R. Steinhoff, G. Boselli, V. Reddy, H. Kunz, S. Marum, R. Cline, Texas Instruments, Inc.
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The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps

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Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps
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Latchup Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

ESD Design Automation for a 90nm ASIC Design System

2004174  N. Guitard, D. Trémouilles, S. Alves, M. Bafleur, LAAS-CNRS; F. Beaudoin, P. Perdu, CNES-THALES; A. Wislez, LCIE
ESD Induced Latent Defects in CMOS ICs and Reliability Impact

2004182  C. J. Brennan, J. Sloan, D. Picozzi, IBM Microelectronics
CDM Failure Modes in a 130nm ASIC Technology

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Compliance Verification: The Critical Component of a Certified ANSI/ESD S20.20 ESD Control Program Plan

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Notes on Maintaining Sub-1V Balance of an Ionizer

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Humidity Effects on Laminated ESD Worksurface Resistance and Charge Dissipation Properties

2004211  B-C. Yap, Nanotronix Technology; C. Newberg, MicroStat Laboratories, Inc.
Study of "Hot Spots" Arising from Non-Homogeneity in the Micro-Structures of Dissipative Materials

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Characterizing Automated Handling Equipment Using Discharge Current Measurements

2004229  J. Paasi, H. Salmela, VTT Technical Research Centre of Finland; J. M. Smallwood, Electrostatic Solutions, Electrostatic Field Limits and Charge Threshold for Field Induced Damage to Voltage Susceptible Devices

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Distributed Gate ESD Network Architecture for Inter-Power Domain Signals

2004248  A. Salman, M. Pelella, S. Beebe, N. Subba, Advanced Micro Devices
ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure

2004255  M. G. Khazhinsky, J. W. Miller, M. Stockinger, J. C. Weldon, Freescale Semiconductor, Inc.
Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies

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Design on Latchup-Free Power-Rail ESD Clamp Circuit in High-Voltage CMOS ICs

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A Compact, Timed-Shutoff, MOSFET-Based Power Clamp for On-Chip ESD Protection

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Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications

2004289  B. Keppens, M. P. J. Mergens, B. Van Camp, K. G. Verhaege, Sarnoff Europe; C. S. Trinh, Sarnoff Corporation; C. C. Russ, Infineon Technologies
ESD Protection Solutions for High Voltage Technologies

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Development Strategy for TLU-Robust Products

2004308  T. J. Maloney, S. S. Poon, Intel Corporation
Using Coupled Transmission Lines to Generate Impedance-Matched Pulses Resembling Charged Device Model ESD
Multilevel Transmission Line Pulse (MTLP) Tester

Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations

2004331 J. Li, S. Hyvonen, E. Rosenbaum, University of Illinois at Urbana-Champaign
Improved Wafer-level VFTLP System and Investigation of Device Turn-on Effects

2004338 E. Grund, Oryx Instruments Corp., R. Gauthier, IBM Semiconductor Research and Development Center
VF-TLP Systems Using TDT and TDRT for Kelvin Wafer Measurements and Package Level Testing

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Breakdown Behavior of TMR Head in ESD Transients

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Effects of ESD Transients on Noise in Tunneling Recording Heads

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Dynamic Temperature Rise of Shielded MR Sensors During Simulated Electrostatic Discharge Pulses of Variable Pulse Width

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Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC

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Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window

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Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology

SCR Operation Mode of Diode Strings for ESD Protection

ESD Protection for Advanced CMOS SOI Technologies
Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit

The Influence of High Resistivity Substrates on CMOS Latchup Robustness

Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies

The Influence of Implanted Sub-collector on CMOS Latchup Robustness

Dependences of Damping Frequency and Damping Factor of Bi-Polar Trigger Waveforms on Transient-Induced Latchup

Design Automation to Suppress Cable Discharge Event (CDE) Induced Latchup in 90nm CMOS ASICs

Guard Rings: Theory, Experimental Quantification and Design

Voltages Before and After Current in HBM Testers and Real HBM

Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices

Characterizing Automated Handling Equipment Using Discharge Current Measurements II

ESD Control in Automated Placement Process

Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

An Alternative Method to Verify The Quality of Equipment Grounding

Unifying Factory ESD Measurements and Component ESD Stress Testing

EOS from Soldering Irons Connected to Faulty 120VAC Receptacles

SoC-A Real Challenge for ESD Protection?
Charge Sensitivity Analysis of Multiple Discharges in a Three Conductor System with Small Gaps

Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup Under System-Level ESD Test

Cell Phone GaAs Power Amplifiers: ESD, TLP, and PVS Devices

ESD Evaluation of the Emerging MuGFET Technology

A Study of Relation Between a Power Supply ESD and Parasitic Capacitance

A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65nm CMOS Technologies

Problems with IO to all Other IOs ESD Stress Test: Two Case Studies

On-Chip System ESD Protection Design for STN LCD Drivers

A Study of ESD Damage to a Device Inside a Metal Enclosure

Amplitude and Asymmetry Study using Magnetoresistive Sensitivity Mapping (MSM) on Manufacturing ESD Failures and ESD Simulation Experiments

A Second ESD Threat for ESD Sensitive Devices with Copper Leads

EOS Exposure of Magnetic Heads and Assemblies in Automated Manufacturing

The Thermodynamics of Physical and Magnetic Changes to AMR Sensors from EOS at Variable Pulse Widths

A Miniature Charged Plate for Testing of Charge Accumulation in Hard Disk Drives

Tribocharging of Materials Used In Tape Heads and Associated ESD Damage

SCR Based ESD Protection in Nanometer SOI Technologies

Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90nm CMOS ASICs

Implementation of High VT Turn-on in Low-Voltage SCR Devices

Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies Avoiding Competitive Triggering

A PNP-Triggered SCR with Improved Trigger Techniques for High-Speed I/O ESD Protection in Deep Sub-Micron CMOS LSIs
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Design and Characterization of a High Voltage SCR with High Trigger Current

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Discharge-Like Events into Unstressed Neighbor Pin

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Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies

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Tremouilles, IMEC vzw; M. Sawada, T. Nakaei, T. Hasebe, Hanwa Electronics Ind. Co. Ltd.; M. Ter Beek,
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Implications

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ESD Protection for the High-Voltage CMOS Technologies

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Devices for Automotive Applications

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Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

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**A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic Cures**

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**Behavior of RF MEMS Switches under ESD Stress**

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**Analysis of Dynamic Effects of Charge Injection due to ESD in MEMS**

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**ESD Events of Cabled GMR Sensors**

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**ESD Robust DeMOS Devices in Advanced CMOS Technologies**

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**When Good Trigger Circuits Go Bad: A Case History**

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**CDM Secondary Clamp of RX and TX for High Speed SerDes Application in 40 nm CMOS**

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**Effect of On-Chip ESD Protection on 10 Gb/s Receivers**

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**Process Variation Aware ESD Design Window Considerations on a 0.18 um Analog, Mixed-Signal High Voltage Technology**

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**Active Clamp Implementation in Complementary BiCMOS Process with High Voltage BJT Devices**

**HBM ESD Robustness of GaN-on-Si Schottky Diodes**

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**CDM Event Simulation in SPICE: A Holistic Approach**

2011163 Dolphin Abessolo-Bidzo, Theo Smedes, Albert Jan Huising, NXP Semiconductors  
**Predictive CDM Simulation Approach Based on Tester, Package and Full Integrated Circuit**

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**A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts**

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**ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology**
2011197 Agha Jahanzeb, Kankan Wang, Jeff Harrop, Jonathan Brodsky, Toshio Ban, Scott Ward, Joe Schichl, Keith Burgess, Charvaka Duvvury, Texas Instruments
Capturing Real World ESD Stress with Event Detector

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Diode Protection of GMR Sensors

Study of System ESD Codesign of a Realistic Mobile Board

Voltage Monitor Circuit for ESD Diagnosis

Two New Unexplained and Unresolved HBM Tester Related Failures

Filter Models of CDM Measurement Channels and TLP Device Transients

Using Directional Couplers to Overcome the Bandwidth Limitations of IV-Probes in TLP Measurements

ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Grenoble

ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits

ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

The Influence of Source Ballast Resistance on Current Spreading in Grounded Gate NMOSs

Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results

ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

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**HBM ESD Protection for Class G Power Amplifiers**

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**An Active MOSFET Rail Clamp Network for Component and System Level Protection [BPR]**

You Li, James Di Sarro, Shunhua Chang, Junjun Li, Robert Gauthier, Ralph Halbach, IBM Semiconductor Research and Development Center

**Maximizing ESD Robustness of Current-Mode-Logic (CML) Driver with Internal Gate Bias Network**

Michael Stockinger, Wenzhong Zhang, Kristen Mason, James Feddeler, Freescale Semiconductor

**An Active MOSFET Rail Clamp Network for Component and System Level Protection [BPR]**

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**High-Voltage Asymmetrical Bi-Directional Device for System-Level ESD Protection of Automotive Applications on a BiCMOS Technology**

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**Effect of Process Technology Variation on ESD Clamp Parameters**

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2014258 Evan Grund, Kyle Grund, Jorge Hernandez, Justin Katz, Grund Technical Solutions; Thomas Chang, Robert Gauthier, Richard Poro, IBM Semiconductor Research and Development Center  
**Reflection Control in VF-TLP Systems**

2014268 Ulrich Glaser, Julien Lebon, Yiqun Cao, Joost Willemen, Infineon Technologies AG  
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2014275 Ramachandran Venkatasubramanian, Kent Oertle, Broadcom Corp.; Sule Ozev, Arizona State University  
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2014282 Dimitri Linten, Steven Thijis, Jan Wouters, Geert Thys, Geert Hellings, IMEC vzw; Vesselin Vassilev,  
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2014326 Icko Eric Timothy Iben, Alain Loiseau, Ephrem Gerbelaise, IBM, Corp.  
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2014336 Shih-Yu Wang, Hao-Chan Huang, Chieh-Wei He, Yao-Wen Chang, Tao-Cheng Lu, Kuang-Chao Chen, Chih-  
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2014342 B. Aliaj, V.A.Vashchenko, T. Mitchell, Maxim Integrated Products; J. J. Liou, University of Central Florida  
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2014349 Yi-Feng Chang, Tsung-Che Tsai, Wan-Yen Lin, Chia-Wei Hsu, Jam-Wem Lee, Shui-Ming Cheng, Ming-Hsiang Song, TSMC  
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2014354 Wen-Yang Hsu, Po-Hsiang Lan, Wan-Yen Lin, Jam-Wem Lee, Kuo-Ji Chen, Ming-Hsiang Song, Taiwan  
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2014359 Alexandar Balevsky, Krassimira Ivanova, LumnComp Design, Ltd., Labora Expert, Ltd.; Alexandar Krumov,  
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2014368 Stanislav Scheier, Stephan Frei, TU Dortmund University
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2014375 Pasi Tamminen, Lauri Sydänheimo, Leena Ukkonen, Tampere University of Technology
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2014384 T. Smedes, S. Zhao, NXP Semiconductors; Y. Christoforou, YC Industrial Projects (Formerly with NXP Semiconductors)
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2014393 Alain Kamdem, Normandie Universite, Presto Engineering; Patrick Martin, Fanny Berthet, Bernadette Domengès, Dominique Lesenechal, Normandie Universite; Jean-Luc Lefebvre, Presto Engineering; Pierre Guillot, NXP Semiconductors
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