White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements

Executive Summary

Industry Council on ESD Target Levels

March 2009

Revision 1.0

工业协会关于 ESD 目标级别

This page is intentionally left blank

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements on IC products for safe handling and mounting in ESD protected areas while addressing the constraints from silicon technology scaling and IC design. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), ESD tester manufacturers, ESD consultants and ESD IP companies. *In terms of product shipped, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies, and over 70% of the total volume of product shipped by the top 20 companies, as reported in the EE Times issue of August 6, 2007*. Membership on the Industry Council is continuously growing and interested parties should contact the Chairmen.

Core Contributing Members	**Supporting Members (Feb 2009)**
Stephen Beebe, AMD	Robert Ashton, ON Semiconductor
Brett Carn, Intel Corporation	Jon Barth, Barth Electronics
Charvaka Duvvury*, Texas Instruments (Chairman)	Michael Chaine, Micron Technology
David Eppes, AMD	Freon Chen, VIA Technologies
Melanie Etherton, Freescale Semiconductor	Stephanie Dournelle, ST Microelectronics
Yasuhiro Fukuda, OKI Engineering	Ted Dangelmayer, Dangelmayer Associates
Reinhold Gärtner, Infineon Technologies	Horst Gieser, FhG IZM
Robert Gauthier, IBM	Leo G. Henry, ESD/TLP Consulting
Ron Gibson, Celestica	Kelvin Hsueh, UMC
Harald Gossner*, Infineon Technologies (Chairman)	Natarajan Mahadeva Iyer, Chartered
Hiroyasu Ishizuka, Renesas Technology	Marty Johnson, National Semiconductor
Satoshi Isofuku, Tokyo Electronics Trading	Michael Jones, Sun Microsystems
Larry Johnson, LSI Corporation	ChangSu Kim, Samsung
John Kinnear, IBM	David Klein, IDT
Timothy Maloney, Intel Corporation	Marcus Koh, Everfeed
James Miller, Freescale Semiconductor	Brian Langley , Sun Microsystems
Alan Righter, Analog Devices	Alan Liang, TSMC
Theo Smedes, NXP Semiconductors	Tom Meuse, Thermo Fisher Scientific
Arnold Steinman, MKS Ion Systems	Homi Nariman, AMD
Teruo Suzuki, Fujitsu	Nate Peachey, RFMD
Benjamin Van Camp, Sarnoff Europe	Roger Peirce, Simco
	Joachim Reiner, AustriaMicroSystems
	Donna Robinson-Hahn, Fairchild Semiconductor
	Jeff Salisbury, Flextronics
* - Charvaka Duvvury: c-duvvury@ti.com	Jay Skolnik, Skolnik-Tech
* - Harald Gossner: harald.gossner@infineon.com	Jeremy Smallwood, Electrostatic Solutions Inc.
	Jeremy Smith, Silicon Labs
	Bart Sorgeloos, Sarnoff Europe
	David E. Swenson, Affinity Static Control Consulting
	Koen Verhaege, Sarnoff Europe
	Tetsuaki Wada, Matsushita Electric Industrial
	Nobuyuki Wakai, Toshiba
	Terry Welsher, Dangelmayer Associates

Translation to Mandarin

Zhixin Wang, Synaptics Inc
Yihong Yang, Synaptics Inc

Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for the future ESD target levels. The Council Members and Associates will promote these recommended targets for adoption as company goals. Being an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies and contract manufacturers. The data represents CDM and field failure information collected from a large variety and volume of IC products; no specific components are identified. The readers should not construe this information as evidence for unrelated field failures resulting from electrical overstress events or system level ESD incidents. The document only refers to component level ESD recommendations which should have no impact on system level ESD requirements.

The Industry Council, while providing these recommendations, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Executive Summary

It is now well understood in the IC industry that the Charged Device Model (CDM) ESD is the ESD model which best describes real world component level ESD events during IC manufacturing and handling. See Chapter 1 for details. In contrast to HBM, where basic ESD control measures at the factory level ensure a single safe and realistic specification level (i.e. 1000V HBM as reported in White Paper I [1]), CDM protection requires additional degrees of ESD control such as managing against the charging of insulators, at specific process steps, to ensure safe and realistic levels for all product designs.

Some important aspects of the CDM challenge must be understood:

1. IC Design / Development Constraints which result from: **silicon technology scaling**, **IC high speed circuit design requirements**, and **larger IC package size trends**. See Chapter 2 for details. These constraints are inhibiting the ESD design methodology required to meet the commonly customer specified 500V CDM level. This is especially true for very high speed high performance pin design types, which have limitations in CDM discharge peak current. As a result, practical designs are restricted to 2-6 Amps of peak CDM current, which translates to a 200-400V CDM voltage level for many advanced technology products (depending on pin-count). Table I below contains representative cases that illustrate the peak current limitation for CDM protection based on high-speed pin design constraints, including the corresponding CDM voltage levels.

Table I: Advanced Circuit Design Impact on Achievable CDM Levels

Technology	Design Type	CDM Peak Current	Package Size	CDM Level
65nm	High Speed Serial Link	5-6 Amps	>300 Pins	300-400V
45nm	High Speed Serial Link	4-5 Amps	>300 Pins	250-300V
45nm	Radio Frequency (RF)	2-3 Amps	>200 Pins	200-250V

2. Perceived CDM requirements of 500V or greater. These no longer can be routinely met for the reasons discussed above, often leading to delays in qualification and time-to-market. The more important focus should be that the designs can no longer support these previous levels and that with the available CDM control methods there is no need for higher CDM levels that make the designs impossible for circuit performance.

3. Improved state-of-the-art CDM ESD control methods that are in practice in the industry today. These controls allow safe handling for devices with CDM pass voltage levels as low as 100V. This work has revealed several important findings that need to be considered before recommending a safe and practical CDM level

执行摘要

目前IC工业界已经充分了解到器件充电模型（CDM）能够更好地描述IC在生产与操作过程中会遇到的实际的元件级ESD的静电级别。更多细节请参看第一章。不同于HBM模型通过在工厂中采用基本的ESD控制措施来保证一个简单、安全、以及实际的技术规范级别（比如在白皮书I中提到的1000V HBM [1]），CDM模型的保护需要额外的ESD控制，比如要在特殊的制程步骤中减少对绝缘体的充电，来保证能够适用于所有产品设计的安全的与实际的级别。

若干需要理解的CDM挑战的重要方面：

1. **IC设计/开发局限性**来源于：**硅制程缩小**，**IC高速电路设计要求**，以及**更大的IC封装尺寸的趋势**。更多细节请参看第二章。这些限制正在妨碍满足普遍客户指定的500V CDM 级别的ESD设计方法。这一点尤其适用于会限制CDM放电峰值电流的超高速高性能的管脚设计类型。结果是对于许多先进制程产品而言（取决于管脚数），实际的设计会局限于2-6安培CDM峰值电流，这相当于200V-400V的CDM电压级别。下面的表I包含了具有代表性的例子，它们阐明基于高速管脚设计限制的CDM保护所对应的峰值电流限制，其中还包含了相对应的CDM电压级别。

表I：先进电路设计对于可达到的CDM级别的影响

制程	设计类型	CDM 峰值电流	封装大小	CDM级别
65nm	**高速串行连接**	**5-6 Amps**	**>300 Pins**	**300-400V**
45nm	**高速串行连接**	**4-5 Amps**	**>300 Pins**	**250-300V**
45nm	**射频 （RF）**	**2-3 Amps**	**>200 Pins**	**200-250V**

2. 公认的500V或更高的CDM要求。由于上述原因，这个要求已经不能普遍达到，因而经常导致合格性验证与上市时机的延迟。而更重要的焦点则是在于设计已经不再能够达到之前描述的级别，同时，当采用可用的CDM控制方法，那些会阻碍电路设计性能的过高的CDM级别要求已经没有必要了。

3. 改进的最先进的CDM模型静电控制方法目前已经应用于工业界。这些控制可以允许操作只通过低至100V CDM级别的器件。白皮书指明出若干重要发现，而这些发现在推荐一个安全且实际的CDM级别之前需要被考虑。

A. Field returns data from 11 billion IC devices show that customer returns can occur for products with CDM pass levels from 200V to 2000V, meaning control of CDM at production sites is more important than a specific performance target level. See Chapter 5.
B. Field failures also can occur when proper CDM control is not established during a product ramp-up (pre-qualification), meaning that production failures must be addressed by correcting the CDM control methods at critical process steps rather than requiring the designs to pass at higher voltages than are achievable by design. See Chapter 3.
C. CDM control measures are available throughout the industry to meet safe manufacturing and handling of products at 100V or above, meaning that products designed for CDM levels at 250V or 500V are equally safe and reliable with good margin. See Chapter 3.
D. Thus, any product with a CDM passing level of 250V or higher can be handled safely and reliably in a facility with basic CDM control measures. This level of protection should result in minimal impact on design and IC circuit performance requirements, and make them compatible with current technology trends. See Chapter 6.
E. As future IC technologies are enabled, there should be a continuous improvement of CDM control with even more advanced methods coming into practice.

4. Recommended CDM Levels: Based on this extensive study, a safe and practical CDM passing level of 250V is recommended at this time as outlined in Table II below. Products with a CDM level lower than 250V should implement additional process-specific measures for CDM control, especially during product ramp-up.

Table II: New Recommended CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to JEDEC)	**ESD control requirements**
$V_{CDM} \geq 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators
$125V \leq V_{CDM} < 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators **+** • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads).
$V_{CDM} < 125V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators **+** • **Process specific measures** to reduce the charging of the device **AND** to avoid a hard discharge (high resistive material in contact with the device leads) **+** • **Charging/discharging measurements at each process step**.

A. 110亿个IC退货器件的分析数据显示，通过200V至2000V的CDM级别的器件均可出现在退货中，这说明在生产地的CDM控制比一个专门的性能目标级别更为重要。请参看第五章。
B. 当正确的CDM控制并没有使用在产品的产能提升阶段（资格预审）时，这也可以导致现场失效，意味着须要在关键的制程步骤中纠正CDM控制的方法来解决失效的问题，而不是要求设计去通过高于设计本身可达到的电压水平。请参看第三章。
C. 工业界拥有只需达到100V或者以上即可满足产品安全生产与操作要求的CDM控制措施，这意味着达到250V或者500V的CDM级别的产品是同等安全与可靠，并拥有充足的安全余裕。请参看第三章。
D. 因此，具有基本CDM控制措施的设备均可以安全与可靠地操作任何通过250V或者更高CDM级别的产品。这个级别的保护应该可以把对设计与IC电路性能要求的影响降至最低，并让它们更符合目前制程的趋势。请参看第六章。
E. 随着未来的IC技术被采用，CDM控制应该不断改进和促进更先进的控制方法成为现实。

4. 推荐的CDM级别：进一步的研究表明，目前推荐采用250V作为一个安全和实际的CDM通过级别，详情列于下表。低于250V CDM级别的产品应该采用额外的、基于其制程的措施来控制CDM，尤其是在产品的产能提升阶段。

表II: 基于工厂CDM控制的全新推荐的CDM分类等级

CDM等级分类 (基于JEDEC标准的测试)	**ESD控制要求**
$V_{CDM} \geq 250V$	• **基本ESD控制方法，**并且要把机器金属部件接地，和控制绝缘体
$125V \leq V_{CDM} < 250V$	• **基本ESD控制方法，**并且要把机器金属部件接地和控制绝缘体 + • **采用制程相关措施来**降低器件的充电**或**避免强放电（高阻材料接触器件引线）
$V_{CDM} < 125V$	• **基本ESD控制方法，**并且要把机器金属部件接地，和控制绝缘体 + • **采用制程相关措施来**降低器件的充电**和**避免强放电（高阻材料接触器件引线）+ • **在每一个工艺步骤进行充电/放电测试**

5. <u>Future Roadmap for continued silicon technology scaling.</u> As technology further scales towards the 22nm range and beyond, even this recommended 250V safe level will not be achievable by design due to impending further scaling effects and the drive towards higher circuit speed performance at data rates reaching 40 Gb/sec or more. We therefore envision that within the next five years, CDM levels into the 125V range would become the new practical targets as indicated in the roadmap of Figure 1. As a consequence, continuously improved CDM control and monitoring at the production areas must become a routine practice. Judging from the factory control methods and the expertise that are available today, this would not be and should not be an issue. As an important note, CDM control to 50V has already been successfully achieved in certain production areas. A continuous improvement in CDM control methods aimed at the 50V level as indicated below in Figure 1 is not only expected but is also imperative for future IC technologies.

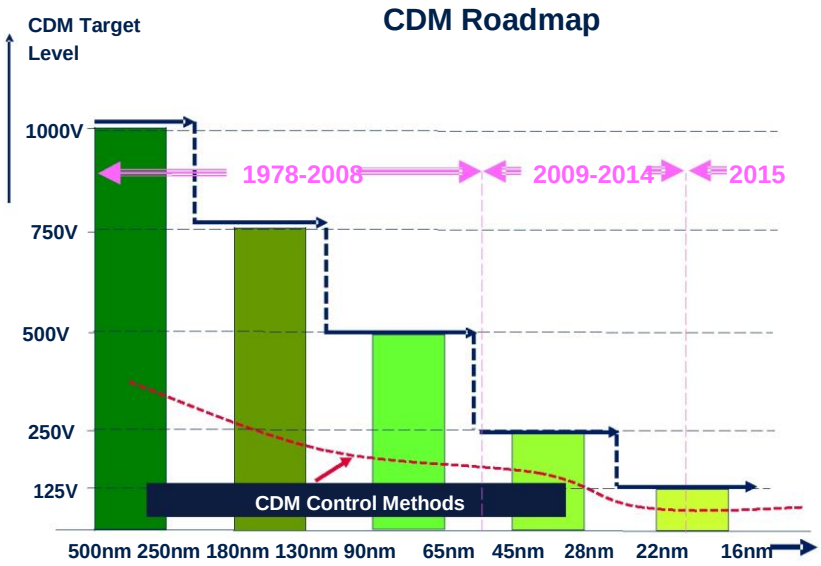

Figure 1: Technology scaling effects on practical CDM levels and the associated CDM control requirements

[1] White Paper 1: "A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," August 2007, www.esdtargets.blogspot.com.

5. 硅制程缩小的未来路线图：随着制程缩小向22nm甚至更低迈进，这里推荐的250V安全级别甚至也很难达到，原因是这会威胁到进一步的缩小效应，以及数据速率高达或超过40Gb/s的高速电路的驱动性能。因此，我们预想在下一个五年内，实际的CDM级别目标将下降至125V范围，这一趋势可以参看图1的路线图。因此，不断改进的CDM控制以及在生产区域的监控必须成为例行措施。从目前可用的工厂的控制方法和专业技术来判断，这将不会、也不应该会成为问题。请注意，在一些特定的生产区域，低至50V的CDM控制方法已经成功实现。图1也显示了在未来的IC技术中，以50V级别为目标而不断改进的CDM控制方法已经不仅仅是预料之中，也是不可避免的。

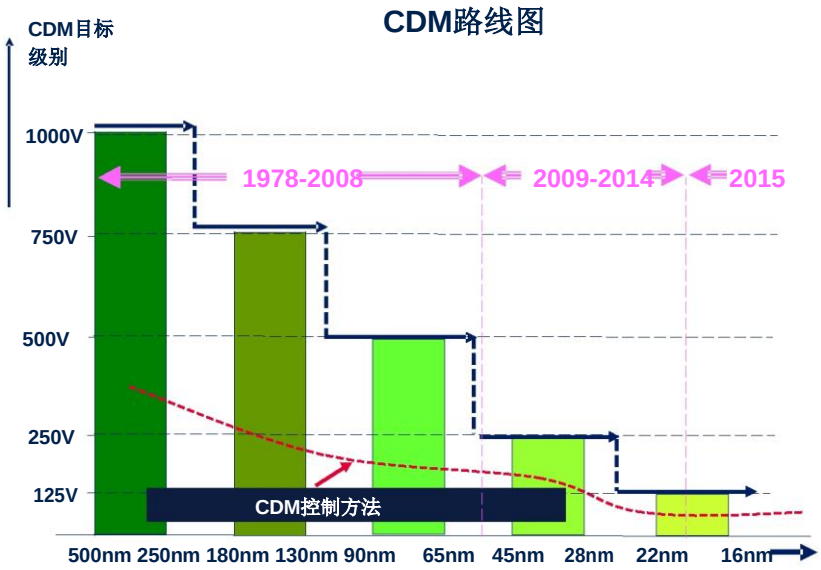

图 1: 制程缩小对实际CDM级别的影响以及相关的CDM控制要求

[1] White Paper 1: “A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements,” August 2007, www.esdtargets.blogspot.com.