47th ANNUAL ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM CALL FOR PAPERS

Including EOS/ESD Manufacturing Sessions

September 13-18, 2025 **Riverside Convention Center** **Riverside, CA, USA**

The EOS/ESD Symposium is dedicated to the understanding of issues related to electrostatic discharge and electrical transients/overstress and the application of this knowledge to the solution of problems in consumer, industrial, and automotive applications, including electronic components, as well as in systems, subsystems, and equipment.

Special Focus Modules

Backside Power, 3D Integration, Memory Stacking, Heterogenous Integration (Enabling the AI Revolution)

Emerging Technologies

The scaling of CMOS technologies continues with a clear outlook beyond the current 3 nm nodes including Gate-All-Around technologies. The introduction of backside power will bring exciting new features to advanced technologies but, at the same time, bring new ESD challenges that need to be addressed in the ESD devices offered. The use of advanced technologies, high application performance, and heterogeneous integration concepts bring up new challenges for ESD protection design. For the 2025 EOS/ESD Symposium we are looking for original publications that showcase the advances and challenges at the technological level.

Device Testing

The scaling of technology and the increasing complexity of packaging require more advanced ESD test solutions. Modern packaging technologies also introduce unknown ESD stress levels during the manufacturing process. Initial measurements show extremely fast pulses addressing the sub-nanosecond time domain. Are existing test methods suitable for the characterization in this time domain or do we need new approaches? We invite submissions that address these questions as well as advances in other areas of ESD testing.

Manufacturing Control

The manufacturing of commercial high-performance 2.5D and 3D ICs has specific ESD-related challenges with new assembly processes incorporating new materials, custom integrations, and associated test methods. Die-to-wafer and wafer-to-wafer bonding, stacked ICs, and modules include subsystems with low ESD withstand levels, with a large number and variety of die-to-die interfaces and small bump pitches. We invite submissions that address advances in control and handling for an industry trending toward very low ESD robustness in the sub-5 V regime.

System and Chip Design

ESD and Latch-up Electronic Design Automation (EDA)

Verifying the ESD protection design of a complex IC design with many supply domains and voltage levels, various functional parts (RF, digital, analog), mixed-voltage circuitry, and advanced packaging will remain a challenge and a driver for the development of new EDA methods. They include ESD EDA verification based on layout-extracted netlists, 2.5D/3D packaging and module-level ESD verification, hybrid flows, including static, dynamic, SPICE and TCAD ESD and latch-up verification, new computational methods, including Machine Learning, and others. For the 2025 EOS/ESD Symposium we are looking for original publications that showcase the advances and challenges in ESD and latch-up EDA.

EMC & ESD Co-Design

The solutions to address conflicting EMC and ESD problems may require co-design efforts, thus leading to innovative solutions at the component and system level while meeting design targets with minimal trade-offs. The problems requiring co-design can be situations such as considering harmonic generation issues due to ESD protection components on high-speed interfaces, reducing EMI on interfaces while protecting against ESD transients, and maintaining signal integrity. Translation of EMC/ESD testing and qualification requirements from the end system environment to IC level has exposed gaps in industry capability to standardize across this ecosystem. Inviting submissions for EMC & ESD co-design efforts influencing IC-level package design, impacts/tradeoffs of technology nodes on ESD for ICs, modules, and system-level design strategies.

Electrostatics

Deep understanding of the basic physical mechanisms of electrostatics such as contact and triboelectric charging, insulators, electrostatic fields and induction, arcing and breakdown, charge motion and dissipation, ionization, etc. are essential for efficient ESD control program and ESD process assessment. We invite submissions addressing the latest advancements and challenges in electrostatics including modeling, measurement, and instrumentation.

Submission Option

Technical Paper	Technical Poster
Abstract: 2-4 pages	**Abstract:** 1-2 pages
Final Manuscript: 6-10 pages	**Final Manuscript:** 3-5 pages
Presentation: Maximum 20 slides	**Presentation:** Maximum 10 slides

Abstract submission due February 7, 2025: Your original 50-word abstract and summary of work to be expanded into a full technical paper or technical poster must clearly and concisely present specific results and explain the importance of your work in the context of prior work. Authors are required to use the applicable abstract submission template available at https://www.esda.org/events/47th-annual-eosesd-symposium-and-exhibits/. The final classification of abstracts as full technical papers or posters is at the discretion of the technical program committee. Full manuscripts of accepted technical papers and posters will be due before the conference. Registration for the conference is required for the author presenting the paper or poster.

The technical program committee accepts unpublished technical papers/posters for peer review with the understanding that the author will not publish the work elsewhere before presentation at the Symposium. Presentation of your work at the earlier International ESD Workshop (IEW) will not preclude your EOS/ESD Symposium abstract submission. The submission must follow guidelines and be expanded significantly for the EOS/ESD Symposium. Publication of accepted papers/posters in any form before presentation at the Symposium may result in the paper/poster being withdrawn from the Symposium Proceedings. Authors must obtain appropriate company and government clearances before submitting an abstract.

Suggested Submission Topics

Advanced CMOS (Analog/Digital) EOS/ESD and Latch-up
- ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, Compound, Graphene, nanowire, etc.)
- On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies
- Backside Power design challenges and opportunities
- ESD Issues in 2.5D & 3D Stacking and TSV

ESD Protection in Bipolar, RF, High Voltage, and BCD Technologies
- ESD Issues in Bipolar, RF, High Voltage, and BCD Technologies and Power Technologies (SiC, GaN, etc.)
- On-Chip ESD Protection Devices & Techniques in Bipolar, RF, High Voltage, and BCD Technologies

Latch-up in CMOS, Bipolar, RF, High Voltage, and BCD Technologies
- DC/Transient Latch-up Issues and Solutions, Troubleshooting, Simulation
- Latch-up prevention in design rules, EDA checks and qualification

Chip/Module/Package EOS/ESD EDA
- Novel EOS/ESD EDA Tools
- Numerical Modeling and Physics of EOS/ESD Events
- ESD Device TCAD and compact models
- ESD Checking and Verification Methodology
- ESD Circuit Simulation and Co-Design
- Circuit Simulation of EOS/ESD Events in CMOS, Bipolar, RF, High Voltage, and BCD Technologies
- Application of EDA tools for EOS/ESD Failure Analysis, Design, and Verification

EOS/ESD Failure Analysis, Troubleshooting, and Case Studies
- EOS/ESD Case Studies, Reviews, and Analysis
- Failure Analysis Techniques and Interpretations
- EOS/ESD Component Failure Analysis
- Testing of MR/TMR Heads and Ultra-Sensitive Devices
- EOS/ESD Protection for Aircraft, Spacecraft, and Avionics

Device Testing: Testers, Methods, and Correlation Issues
- Novel EOS/ESD Test and Characterization Methods
- Transmission Line Pulse Testing Systems
- HBM, CDM Tester Issues and Solutions
- Tester Correlation Issues
- Standards – Round-Robin Testing, Results, and Analysis

System Level EOS/ESD/EMC, HMM
- System Level EOS/ESD/EMC Test Methods
- System Level EOS/ESD Modeling and Simulation
- EOS/ESD Simulators, Calibration, and Correlation
- Transient ESD/EMI Induced Upset
- Case Studies, Reviews, and Analysis
- Standard Test Boards as an Early Measure of Robustness

Manufacturing
- ESD Packaging and Handling Procedures
- EOS/EMI/ESD Detection and Measurement Techniques
- EOS/ESD Mitigation in Test and Manufacturing
- EOS/EMC/ESD Process Assessment
- ESD Control Materials and Use of Low Charging Materials
- EOS/ESD Control Program Topics

Technical Program Chair
Alain Loiseau, Globalfoundries, alain.loiseau@globalfoundries.com

General Chair
Mirko Scholz, Infineon Technology AG, mirko.scholz@infineon.com

EOS/ESD Association, Inc.
Christina Earl, +1-315-339-6937 ext. 222, cearl@esda.org