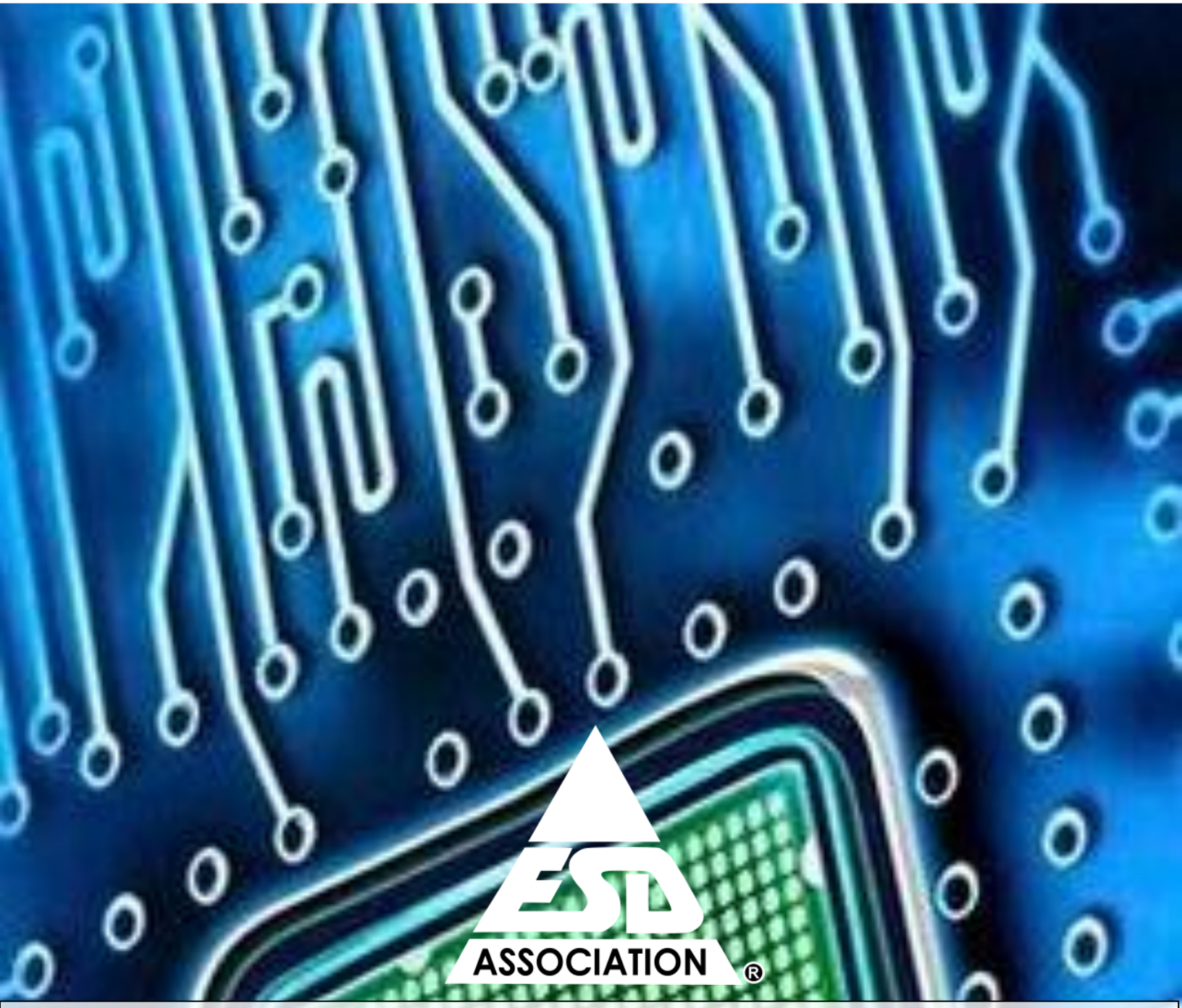

International Electrostatic Discharge Workshop (IEW-US)

April 1-3, 2025

Hyatt Regency, Monterey, CA USA

Co-located with IRPS

Setting the Global Standards for Static Control

EOS/ESD Association, Inc. 218 West Court Street, Rome, NY, 13440 USA
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Experience IEW @ IRPS: Register Here

Dear Colleagues,

Continuing the tradition that started almost two decades ago in Lake Tahoe, now in its fifth year co-located with IRPS, the 2025 US IEW will focus on ESD challenges in IC and systems design and manufacturing. Complementing the three formal technical tracks at IRPS, the IEW parallel workshop program provides a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities.

Our program is designed to stimulate discussions and provide a platform for presenting both completed research and open research questions. Each day, following the IRPS opening, we will start the IEW program with an IEW keynote speaker, each expert from diverse fields of consumer electronics, semiconductor equipment, and EDA. We are particularly excited this year to host two Distinguished Panel sessions that bring ESD experts from Foundry, EDA design, and manufacturing together for unique collaboration and idea exchange. We look forward to participating in the IEW technical sessions, beginning with a five-minute teaser presentation from each author and ending with an engaging poster-based discussion, ensuring opportunities for interaction and advancement of the work.

In addition to everything IEW-US provides, IEW-US registrants can attend the full IRPS technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception. IRPS registrants will have access to the IEW keynote and invited talks.

We look forward to meeting you at IEW and the stimulating engagement that will surely follow

***Ann Concannon**,*
Texas Instruments,
Management Committee Chair
on behalf of the IEW-US management committee

(Keynote) Keeping up with Moore's Law: Navigating Quality & Reliability Challenges in the Fast Lane of Mobile Processors

Tuesday, April 1, 2025, 11:05 AM – 12:20 PM

Amit Marathe, Head of SoC/Module Reliability Engineering, Google

While Moore's Law continues to provide scaling benefits to enable SoCs, it poses major Reliability and Manufacturing challenges. Supply voltages and current densities are scaling at a slower pace than device dimensions. As a result, TDDB, Electromigration and ESD are posing major quality and reliability challenges at advanced nodes (5nm and beyond). The talk will elaborate on technology scaling with focus on mobile applications and highlight the major Silicon reliability degradation mechanisms.

Accurate estimation of system level reliability requires a thorough understanding of the failure modes of the various components and modules that make up the system and their interactions with each other. A clear definition of Mission profile is necessary to project the test data to use conditions. With the increasing use of smart devices, mobile technologies and ubiquitous computing, the usage scenarios are getting increasingly complex. As a result, JEDEC based standard Qualification methodologies for components cannot be relied upon to ensure reliability at system level during field usage

A comprehensive Silicon Reliability framework using a system based holistic approach will be discussed. This framework comprehends user environment and usage scenarios at system level to make reliability projections and develop solutions for EMC robustness. "Design for Reliability" (DfR) approaches will be presented to enable performance without compromising reliability.

Amit Marathe earned his M.S. and Ph.D. in Materials Science and Engineering from the University of California, Berkeley in May 1991 and August 1996 respectively.

Amit joined AMD in Sunnyvale CA after graduation and then GlobalFoundries in 2009. At AMD and GF, he was leading and managing the Technology & Reliability Development Organization. In 2011, Amit joined Microsoft and was managing the Silicon/Packaging Operations & Reliability Org for all of Microsoft Hardware. Amit joined Google in 2016 where he is heading the SOC/Module Technology and Reliability Engineering Org within the Devices & Services Products Group at Google.

Amit has co-authored over 40 technical research publications as well as a chapter in a book on Moore's Law Scaling Reliability Challenges. He has chaired sessions at IRPS Conf. and presented "Year in Review" on System Reliability. He also gave a tutorial on the same topic in 2018 IRPS. He has given keynotes at other International Conferences. He is a co-inventor of over 15 patents granted and over 50 pending US patents in the area of technology & reliability development.

(Keynote) Thermal and Materials Challenges in 3D Heterogenous Integration – a Process and Process Integration Perspective

Wednesday, April 2, 2025, 9:10 AM – 10:00 AM

Siddarth Krishnan, PhD, Managing Director, IMS Heterogeneous Integration, Semiconductor Product Group, Applied Materials Inc.

As More-than-Moore technologies proliferate across the industry, the excitement of renewed scaling opportunities is tempered by new challenges in the form of managing heat and reliability. While Hybrid Bonding (HB) provides massive improvements in latency and I/O densities, scaling HB pitches may lead to hitherto unseen challenges in stress migration and dielectric breakdown along the bonding interface. Backside power delivery and other forms of 3D integration, such High Bandwidth Memory (HBM), are also making it challenging to remove heat from the chips. This talk will focus on an overview of 3D Heterogenous Integration across Logic and Memory and will provide insight on materials innovations to address reliability concerns in this burgeoning new field.

Siddarth Krishnan is Managing Director at Applied Materials, with an R&D focus on Materials Engineering for Heterogeneous Integration, Power Devices, and alternative memories such as RERAM and FERAM. Prior to working at Applied, Siddarth worked as an engineering manager at IBM on High-K/Metal Gate and FinFET devices and engineering the gatestack and its reliability for IBM's 32nm, 22nm, and 14nm product lines. Siddarth’s experience at Applied includes developing Atomic Layer Deposition (ALD) products for Applied's MDP business unit and working on Power devices (Si and SiC). Siddarth’s current focus is on Heterogeneous Integration and 3D stacking.

Siddarth has a Bachelor of Science in Metallurgical Engineering from IIT Madras, a Masters in Materials Engineering, and a PhD in Electrical and Computer Engineering, both from The University of Texas at Austin.

(Plenary Poster Session) Control, Metrology, and Technology

Wednesday, April 2, 2025, 10:35 AM – 12:30 PM

Moderator: Mohammed Fakhruddin, Google

1A.1 Analysis of ESD Diode Discharge Characteristics Based on Substrate Thickness

Dongseok Shin, Samsung Electronics

Traditional semiconductor memory used single-sided substrates. Modern advanced manufacturing employs die-to-die bonding with TSVs, using both sides and driving wafer thinning for improved performance. TCAD simulations analyzed structure and TLP data for 16 STI thicknesses--from 0.4x to 13.3x the STI depth. In diode structures, degradation begins at twice the STI depth, with Ron rising over 2.5x at 1.2x. A gated diode effectively enables direct surface conduction, thereby preserving robust ESD performance even with thinner substrates.

1A.2 Chip to Chip 2.5/3d Assembly ESD

Eugene Worley, Silicon Crossing

1A.3 I/O Circuit and Sub-5V ESD Protection for Advanced Bonding Interfaces

Miheal Krilčić, imec and University of Zagreb

This study investigates the impact of ESD protection on performance of 2.5D-chiplet and 3D integrated architectures, focusing on 12-nm FinFET devices. Using 1-ns-pulse ESD stress measurements and S-parameter analysis, it assesses trade-offs between ESD protection effectiveness and the corresponding capacitance and layout area penalties. The findings highlight the difficulties in optimizing chiplet interconnects while meeting evolving protection standards.

1A.4 TDDB Characterization of High-k Gate Dielectric on a Sub-nanosecond Timescale

Matt Drallmeier, UIUC

This work presents on-chip pulse generators fabricated in 16-nm and 65-nm CMOS technologies and used to measure the breakdown voltage of high-k and SiO2 gate dielectrics on a sub-nanosecond timescale. The pulse generators produce clean single-shot pulses with amplitude up to 7.5 V and pulse width as short as 100 ps. The sub-ns applicability of established models for TDDB voltage acceleration and area scaling is assessed using the pulse generator.

(Distinguished Panel & Workshop) Foundry ESD Checks and IC Requirements

Wednesday, April 2, 2025, 2:45 PM – 5:45 PM

Moderator: Slavica Malobabic, Cirrus
Panelists: Takeo Tomine, Ansys; Michael Thompson, Cadence; Matt Hogan, Siemens; Efraim Aharoni, Tower; Vadim Kushner, Skywater; Jam-Wem Lee, TSMC; Stephen Fairbanks, SRF Technologies

At the 2025 US-IEW we would like to discuss the ESD sign off process when it includes foundry rules for all aspects of the ESD sign off process: Latch up, HBM or CDM. In some cases, the foundry checks are not catered to the types of pins that are being protected even when using foundry ESD. In other cases, the foundry checks are not context aware or voltage aware which either creates false flags or misses parasitic device check. How many rules need to be added on top of standard foundry rules for different use cases?

How do you go about waiving foundry rules that are flagging and assessing the risk this may or may not pose? What strategy and tool do you use? An in-house tool? Commercial ESD tools? Do you go with enhanced static checks (cover circuit topology and back end)? How does that look like? Or do you go with dynamic checks which need to include the ESD model of the ESD clamp? What type of the ESD model do you get and use from the foundry? Do you build your own model? What type of SOA information do you get from the foundry that you can readily use? What type of SOA information (not limited to ns time domain) would be useful, but is not readily available?

Of interest to:

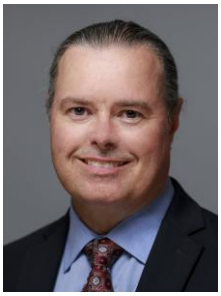
- ESD designers in charge of an ESD sign off process, who can shed light on how the decisions are made and what kind of information is needed to do the analysis.
- Foundry ESD experts who set the rules to clarify the foundry ESD rule deck intent and conditions under which they may or may not waive the standard rules. Are there any waiver rules already available for custom cases?
- EDA and TCAD Tool vendors to offer insight into:
    - a. What types of checks are possible/standard today.
    - b. How much of the information for the checks above comes straight from the foundry and how much involves internal effort.
    - c. How easy it is to add custom checks on top of foundry checks?
- IP Vendors

Efraim Aharoni received the B.Sc. and Ph.D. degrees in Physics in 1989 and 1994 respectively, from the Technion, Israel Institute of Technology. His research was focused on High Temperature Superconducting devices. In 1993 he joined Tower Semiconductor. Efraim worked in Tower Semiconductor in a variety of fields, in both engineering and management, in development as well as manufacturing. Amongst his engineering roles: process, device, yield, and reliability. In the past 15 years, he led the ESD and Latch-Up activities in the company. This involves the development of ESD devices and protection concepts, characterization, design guidelines, ESD PDK, PERC, and customer support. He works closely with the Tower Semiconductor design center, device engineering, PDK group, customers, and production lines in Tower Semiconductor sites worldwide. One of his contributions was developing a simulation ability of circuits containing snapback-based devices, employing behavioral code and 'empirical models' based on measurements. In parallel, he is a senior lecturer in the Electrical Engineering department in the Academic Kinneret College in Israel. During the years 2020-2024 he served as the head of the department. Efraim was a member of the IEW and EOS/ESD Technical Program Committees several times. He is a member of the Industry Council of ESD Standards and co-chair of WG22 working group (ESD parameters).

Trained as an Analog and RF Circuit Designer, Stephen has been developing process specific I/O and ESD libraries for 25 years.

In the early 2000's he managed the I/O and ESD Library Group suppling all IO and ESD solutions for Intel Wireless and Communications products.

During this time, he helped pioneer ESD and IO solutions in first generation 3G RF CMOS front-end as well as many early generation Audiocodecs, Touchscreen interfaces, Bluetooth and WiFi Chipsets. In 2006, he left Intel to found SRF Technologies, an ESD Consulting company; later, in 2009, Certus Semiconductor, an IP provider of custom ESD and IO Libraries in most major foundries. He has designed over 150 IO Libraries in over 40 different process technologies, targeting every major industry including low power IoT, high performance computing, automotive, industrial, consumer electronics, communications and Aerospace and satellite applications.



Matthew Hogan is a Product Management Director for Calibre Design Solutions at Siemens Digital Industries Software, with over two decades of design, field and product development experience. He actively works with customers who have an interest in Calibre® PERC™, Insight Analyzer, IC reliability verification and other reliability topics. Matthew actively volunteers his time with IEEE and other organizations. He has been the past general chair for both the International Electrostatic Discharge Workshop (IEW) and International Integrated Reliability Workshop (IIRW), has previously been on the Board of Directors for the ESD Association (ESDA), contributes to multiple working groups for the ESDA and is an industry advisor to the Center for Advanced Electronics Through Machine Learning (CAEML). Matthew is also a Senior Member of IEEE, and a member of ACM. He holds a B. Eng. from the Royal

Melbourne Institute of Technology, and an MBA from Marylhurst University. Matthew can be reached at matthew.hogan@siemens.com.

Vadim Kushner is a part of the SkyWater Technology Reliability and Design Enablement teams with focus on electron devices development and characterization. He uses his expertise in electron devices, advanced ESD protection and reliability improvements to support SkyWater foundries plug and play technology solutions. He gathered his experience working for companies of different sizes targeting various markets for more than 20 years. It allowed to learn in depth broad scope of silicon technologies for various applications. His thinking outside the box helped to find some original solutions that resulted in multiple patents. Current work involves development of advanced SOI and bulk silicon technologies with additional reliability requirements. Beside having fun advancing new exciting and challenging technologies he enjoys rock climbing, alpine skiing, cycling, and swimming.

Jam-Wem Lee was born in Taitung, Taiwan. He received his B.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 2002, respectively. During this period, he focused on improving the reliability and scalability of nano-scaled thin films. From 2001 to 2002, he worked at United Microelectronics Corporation, Taiwan, as an engineer, where he focused on designing electrostatic discharge circuits. From 2003 to 2007, he was a researcher at the National Nano Device Lab in Taiwan, working on the simulation, design, and fabrication of ESD circuits in nano-scaled devices. Since 2007, he has been with Taiwan Semiconductor Manufacturing Company (TSMC), responsible for ESD/LUP technology development for advanced technologies. He has filed over 100 patents in the ESD and LUP fields.

Takeo Tomine is Principal Product Manager for Analog & Mixed Signal Products at Semiconductor Business Unit at Ansys Inc. His work focusses on product planning for Analog/Mixed Signal simulation products at Ansys and field AE support. He has over 10 years of experience in EDA industry. At Ansys, he has various positions in Applications Engineering and Product Management. His research interest includes power estimation, power noise, reliability and thermal analysis for chip-package and system.

Takeo is a graduate of the University of California, Los Angeles (UCLA) with a Master's in Engineering with a focus in Analog & Mixed Signal IC design emphasis.

Michael Thompson is a Distinguished Engineer in the Virtuoso R&D group at Cadence Design Systems (CDS). His current charter is the development of design solutions for heterogeneous integration across digital, analog, and high-frequency domains. These solutions require complete flows, allowing initial design concepts through detailed design and analysis, verification, manufacturability, and tape-out. He works closely with software developers, end-users, and foundries to implement complete deployable development flows. Before joining Cadence, Michael had various roles in Keysight/Agilent/HP EEsof field organization from AE with specialties in EM, RFIC, and MMIC design, AE District Manager, and Enterprise Account Manager. Before joining HP, Michael was a Senior Specialist at Aerojet ElectroSystems, designing antennas and subsystems for radiometric sensors for the EOS and SSMIS satellite platforms and passive and active sensor antennas and transceivers for the SADARM and STAFF programs. Before Aerojet, he was a member of the technical staff of the Phased Array Antenna Lab at Hughes Aircraft. He was responsible for the design of active and passive beam steering modules. He has a BSECE and MSEE from Cal Poly and did Post-Grad work at USC.

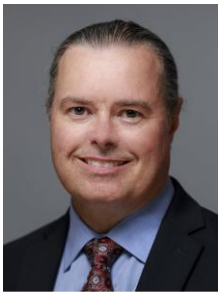
(Keynote) Improving the Fidelity of ESD Margins With Context-Aware ESD Simulation

Thursday, April 3, 2025, 9:10 AM – 10:00 AM

Matthew Hogan, Product Management Director, Siemens

Conservative design rules and constraints are often used in reliability verification flows. By combining the leading solutions for ESD reliability verification and SPICE simulation technologies, SPICE-accurate full-chip simulation becomes possible in a compelling flow for design teams looking to better understand their ESD design margins.

We will explore the challenges of traditional parasitic extraction methods, sourcing appropriate SPICE simulation models, and demonstrate how a context-aware ESD simulation flow can improve the fidelity of results to better understand ESD design margins while performing full-chip SPICE-accurate simulations on ESD paths within your design.



Matthew Hogan is a Product Management Director for Calibre Design Solutions at Siemens Digital Industries Software, with over two decades of design, field and product development experience. He actively works with customers who have an interest in Calibre® PERC™, Insight Analyzer, IC reliability verification and other reliability topics. Matthew actively volunteers his time with IEEE and other organizations. He has been the past general chair for both the International Electrostatic Discharge Workshop (IEW) and International Integrated Reliability Workshop (IIRW), has previously been on the Board of Directors for the ESD Association (ESDA), contributes to multiple working groups for the ESDA and is an industry advisor to the Center for Advanced Electronics Through Machine Learning (CAEML). Matthew is also a Senior Member of IEEE, and a member of ACM. He holds a B. Eng. from the Royal Melbourne Institute of Technology, and an MBA from Marylhurst University. Matthew can be reached at matthew.hogan@siemens.com.

(Seminar) ESDA updates on System Level ESD

Thursday, April 3, 2025, 10:00 AM – 10:25 AM

(Plenary Poster Session) Focus on Design and Simulation

Thursday, April 3, 2025, 10:45 AM – 12:30 PM

Moderator: Derong Yan, Siemens

2A.1 Working Towards a Latch-Up Test User Guide Section on Maximum Stress Voltage (MSV)

Michael (Michi) Stockinger, NXP Semiconductors Austin

The MSV was introduced in JESD78 in 2011 to allow devices that fail post-stress ATE testing with traditional voltage limits to still pass JESD78 if the damage was not caused by latch-up. Determining whether the MSV can be invoked has always been a source of confusion. The planned JESD78 User Guide will contain example I-V plots which will be introduced here together with their interpretations and flow charts guiding users through the MSV decision process.

2A.2 TLP Based Metal Modeling for Circuit Simulation

Eugene Worley, Silicon Crossing

2A.3 HBM Module for Complementary Characterization and Validation of ESD Devices

Efraim Aharoni, Tower Semiconductor

TLP measurements offer limited insight into temporal behavior of ESD devices during HBM events. This raises concerns about triggering time and device turn-off. This work demonstrates a complementary characterization and validation method, utilizing a wafer-level HBM module. The study concentrates on two cases: Chains of cascaded transistors, used for High-Voltage tolerant protection in 5V CMOS technology, and chains of SCR's in SOI technology, employed as ESD power-clamps for operation voltages up to hundreds of Volts.

2A.4 Novel Trigger Circuit & SCR Device Co-Engineering Based Local (I/O-VSS & I/O-VDD) ESD Clamp Concepts with Improved Latch-up Susceptibility, Lower Leakage and Lower Capacitance for Ultra High Speed I/Os

Mitesh Goyal, Indian Institute of Science, Bangalore

In this work, a novel SCR is presented which is co-engineered with trigger circuit to reduce the latch-up susceptibility and reduce the capacitance, leakage and trigger voltage over a conventional design. The novel design is implemented in Samsung 28nm low power bulk planar technology. Its TLP/vfTLP characterization and ESD measurement data along with the design trade-offs are presented and compared with an established reference SCR protection concept for CDM protection in high speed I/Os.

2A.5 Proposal to Achieve the Ultimate Holding Voltage Tunability in Silicon Controlled Rectifiers (SCRs) for a Wide Range of ESD Protection Applications

Mayank Yadav, Indian Institute of Science, Bangalore

A novel silicon-controlled rectifier (SCR) concept for ESD protection is proposed with holding voltage tunability from 2V to 10V. The novel proposal replaces the standard N+/P+ implants in N-Tap/Cathode and P-Tap/Anode by P+ -N+ and N+ -P+ implants. Physical insight of the proposed concept with several derivative concepts, explaining the trigger and holding voltage tunability. Besides, additional, rather refined, tunability is depicted by engineering the junction profile of the P+ -N+ and N+ -P+ implants.

(Distinguished Panel & Workshop) Standardized ESD Compact Models

Thursday, April 3, 2025, 1:30 PM – 3:50 PM

Moderator: Michi Stockinger, NXP
Panelists: Shudong Huang, UIIC; Stephen Fairbanks, Certus Semiconductor; Steven Poon, TSMC; Michi Stockinger, NXP

The Compact Model Coalition (CMC) of the Si2 has been working on ESD models, with the first one (the “ASM-ESD” diode model) released in 2022, and another one (the “ESD FET” snapback model) currently being worked on. Accurate ESD models for SPICE simulations have become increasingly important for “first time right” ESD designs, especially for advanced CMOS technologies having very low Gate breakdown voltage levels and MOSFETs that fail immediately after snapback, even during CDM stress. The need for ever higher IO speed and its tradeoff with ESD performance due to parasitic capacitance of ESD devices also puts a high cost on ESD “over design”. Standardized ESD models offer a great opportunity for the industry to “speak a common modeling language”, for example, through their adoption in foundry PDKs.

Of interest to:

- ESD designers familiar with ESD compact models (especially the ASM-ESD model by the CMC), describing model capabilities and providing feedback on ease-of-use.
- ESD designers unfamiliar with ESD compact models, highlighting model complexities and “asking the right questions”.
- Modeling experts, giving insight into state-of-the-art parameter extraction methods that could be used instead of manual step-by-step parameter fitting.
- TLP test engineers, focusing on the ESD device characterization methods needed for accurate model extraction (e.g. capturing overshoot effects due to extremely fast pulses).
- Foundry ESD device/modeling engineers, providing insight about the PDK landscape and a possible “path to success” for adopting standard ESD models.

Trained as an Analog and RF Circuit Designer, Stephen has been developing process specific I/O and ESD libraries for 25 years.

In the early 2000’s he managed the I/O and ESD Library Group suppling all IO and ESD solutions for Intel Wireless and Communications products.

During this time, he helped pioneer ESD and IO solutions in first generation 3G RF CMOS front-end as well as many early generation Audiocodecs, Touchscreen interfaces, Bluetooth and WiFi Chipsets.

In 2006, he left Intel to found SRF Technologies, an ESD Consulting company; later, in 2009, Certus Semiconductor, an IP provider of custom ESD and IO Libraries in most major foundries.

He has designed over 150 IO Libraries in over 40 different process technologies, targeting every major industry including low power IoT, high performance computing, automotive, industrial, consumer electronics, communications and Aerospace and satellite applications.

Shudong Huang is a PhD candidate from the ECE department at University of Illinois at Urbana-Champaign. Advised by Professor Elyse Rosenbaum, Shudong's primary research interests include CDM-reliable broadband IO circuits, ESD circuit/device design, and compact modeling of ESD devices.

Steven S. Poon has dedicated his career to electrostatic discharge (ESD) and latch-up (LU) since late 1999. He received the B.Sc. and M.Eng. degrees in Electrical Engineering from Cornell University, Ithaca, NY. He joined Intel Corporation thereafter, and was responsible for various ESD/LU-related functions at different parts of his career there including protection structure development, process certification, design rules and guidelines, product co-design and sign-off, EDA tools, and system-level ESD design. His experience at Intel spanned all technologies nodes from 0.13um to 5nm, including the ESD/LU development work enabling the smooth transition to copper interconnect, high-k/metal gate, FinFET and 3DIC. While at Intel, he pioneered the use of ESD simulation techniques not just for IP co-design, but also chip-level sign-off. He has published various papers at IEEE-sponsored conferences, and contributed to tutorials and industry technical reports. He later joined the Quality and Reliability organization of TSMC in 2021, and responsible for ESD-related functions handled by the organization.

Michael "Michi" Stockinger received his PhD in electrical engineering with highest honors from Vienna University, Austria, in 2000. His doctoral research focused on the optimization of ultra-low-power CMOS transistors. In 2000, he joined Motorola's semiconductor sector, which became Freescale Semiconductor in 2004 and NXP Semiconductors in 2016. Michael is currently a Technical Director with NXP's Advanced Chip Engineering division located in Austin, Texas, focusing on ESD protection and LU prevention for advanced CMOS products. His on-chip ESD solutions have been implemented in the Kinetis, i.MX, ColdFire, and MCX product lines. Michael was awarded several EOS/ESD Symposium awards: 2001 Best Paper, 2003 Best Paper & Best Presentation, 2013 Best Paper & Outstanding Paper, and 2020

Best Paper. He received the 2023 Industry Pioneer Recognition Award by the ESD Association. Michael has authored over 40 technical papers and holds over 30 patents. He has served in the TPCs of several EOS/ESD Symposia, International Reliability and Physics Symposia, and International ESD Workshops, and has taught several ESDA tutorials and online courses. Michael is chair of the JEDEC JESD78 latch-up testing workgroup and Si2's CMC ASM-ESD diode model workgroup.

Schedule

	TUESDAY ● APRIL 1		WEDNESDAY ● APRIL 2		THURSDAY ● APRIL 3
	Regency Main		Regency Main		Regency Main
8:00 AM	General Chairs Welcome & Introduction Program Chair: Overview of Technical Program Awards Keynote 1: Min Cao, TSMC, Taiwan Keynote 2: Choon Heung Lee, Intel, USA	8:00 AM	Keynote 3: Elif Balkas, Wolfspeed, USA	8:00 AM	Keynote 4: Shankar Venkataraman, Applied Material, USA
8:45 AM		8:45 AM	BREAK & EXHIBITS International Foyer	8:45 AM	BREAK & EXHIBITS International III & IV
			Windjammer I		Windjammer I
		9:05 AM	IEW Intro	9:05 AM	IEW Intro
		9:10 AM	IEW Keynote 2: Siddarth Krishnan, Applied Material, USA	9:10 AM	IEW Keynote 3: Matt Hogan, Siemens
10:05 AM	BREAK & EXHIBITS Regency Terrace	10:00 AM	BREAK & EXHIBITS Regency Terrace	10:00 AM	Seminar 1: ESDA updates on System Level ESD
10:35 AM	Windjammer I	10:35 AM	IEW Plenary Poster session 1	10:25 AM	BREAK & EXHIBITS ● Regency Terrace
10:40 AM	IEW Intro			10:45 AM	IEW Plenary Poster Session 2
11:05 AM	IEW Keynote 1: Amit Marathe, Google Follow on discussion on the topic				
12:20 PM	12:00 PM - 1:30 PM ● LUNCH ●	12:30 PM	12:00 PM - 1:30 PM ● LUNCH ●	12:30 PM	12:00 PM - 1:30 PM ● LUNCH
	IEW Afternoon		Joint IRPS Session		IEW Windjammer I
1:30 PM	Outdoor Networking activities	1:30 PM	ESD and Latchup	1:30 PM	IEW Distinguished Panel 2: "Standardized ESD Models" and workshop
		2:20 PM	BREAK & EXHIBITS ● Regency Terrace		
			IEW Windjammer I		
		2:45 PM	IEW Distinguished Panel 1: "Foundry ESD checks and IC Requirements" and workshop		
				3:50 PM	BREAK & EXHIBITS ● Regency Terrace
					Regency Main
				4:10 PM	Closing Ceremony, Prize Drawing & 2026 Introduction
6:15 PM	Workshop Reception ● Mark Thomas Foyer	5:45 PM	IRPS Poster Reception ● Monterey Ballroom	4:25 PM	Adjourn Conference
6:15 PM	Workshops 1-6				
7:15 PM	BREAK				
8:15 PM	Workshops 7-12				
9:30 PM		9:00 PM			

2025 International ESD Workshop (IEW-US)

April 1-3, 2025

Hyatt Regency Monterey
1 Old Golf Course Rd.
Monterey, CA, USA

		IRPS Tech	IRPS Tutorials + Year in Review	IRPS Bundle	IRPS Bundle + IEW	IRPS Tech + IEW
IRPS Tutorial			✔	✔	✔	
Year in Review			✔	✔	✔	
Main conference		✔		✔	✔	✔
Poster session		✔		✔	✔	✔
Workshop		✔		✔	✔	✔
IEW (ESD workshop)					✔	✔
Fee for early registration (before 2/28)	Non-member	$900	$980	$1,780	$2,130	$1,250
	IEEE member	$720	$790	$1,430	$1,780	$1,070
	Student non-member	$360	$390	$710	$760	$410
	IEEE student member	$290	$310	$570	$620	$340
	IEEE Lifetime Member	$290	$310	$570	$920	$640
Fee for standard registration	Non-member	$1,030	$1,130	$2,050	$2,400	$1,380
	IEEE member	$820	$900	$1,640	$1,990	$1,170
	Student non-member	$410	$450	$820	$870	$460
	IEEE student member	$330	$360	$660	$710	$380
	IEEE Lifetime Member	$330	$360	$660	$1,010	$680

Register online: https://cvent.me/599QkN