EOS/ESD Association, Inc. White Paper

Electrostatic Discharge (ESD)/Electrostatic Attraction (ESA) Considerations in Semiconductor Wafer Fab and Associated Facilities

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TABLE OF CONTENTS

1.0 INTRODUCTION AND PROBLEM STATEMENT 1

2.0 CURRENT STATUS OF ESD/ESA CONTROLS IN ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT MANUFACTURING FACILITIES (NON-SEMICONDUCTOR FABS) 1

2.1 ANSI/ESD S20.20 OVERVIEW 1
2.2 SEMI E78 (MINI-ENVIRONMENT), E129 (LARGER FAB - CLEANROOM), E163 (RETICLE) 2
2.2.1 SEMI E78 2
2.2.2 SEMI E129 3
2.2.3 SEMI E163 3

3.0 SEMICONDUCTOR MANUFACTURING ESD/ESA CHALLENGES/CONSIDERATIONS .. 3

3.1 ESA-RELATED CONTAMINATION 3
3.1.1 Electrostatically Driven Micro-Contamination 3
3.1.2 Electrostatic Fields 4
3.1.3 Charges in the Environment 5
3.1.4 Field Penetration of Insulating Enclosures 5
3.1.5 Moving Charges and Moving Grounds 5
3.1.6 Electrostatic Bonding 6
3.1.7 Rules for Controlling Electrostatically Driven Contamination 6
3.2 RETICLE HANDLING 6
3.2.1 The Physics of Photolithography 6
3.2.2 Transmission Photolithography 9
3.2.3 EUV (Reflection Photolithography) 12
3.2.4 Implementation 13
3.3 200-MM VERSUS 300-MM FABS; OPEN CASSETTE VERSUS SMIFF/FOUP CARRIERS 13
3.4 BACKSIDE POWER DELIVERY NETWORK AND ESD IMPLICATIONS 21
3.5 DIE-TO-DIE AND WAFER-TO-WAFER BONDING 21

4.0 GENERALLY ACCEPTED ESD/ESA CONTROL PRACTICES FOR A SEMICONDUCTOR FAB 24

5.0 COMPARISON OF ESD MANUFACTURING CONTROLS CERTIFIED ACCORDING TO ANSI/ESD S20.20 OR IEC 61340-5-1 VERSUS SEMICONDUCTOR MANUFACTURING ESD/ESA CONTROLS BEST PRACTICES 26

6.0 CONCLUSION AND RECOMMENDATIONS 27

7.0 BIBLIOGRAPHY 27

Figures

Figure 1: Calculation of Various Deposition Velocities 4
Figure 2: Field Lines from a Charged Wafer 4
Figure 3: Electric Fields Penetrating the FOUP Wall 5
Figure 4: Force on a Particle With Ten Electrons of Charge 6
Figure 5: Principles of Photolithography 7
Figure 6: The Electromagnetic Spectrum Used in Photolithography 8
Figure 7: Diffraction With Constructive and Destructive Interference 8
Figure 8: Image Showing the Reticle Has Many Chrome Pieces and a Guard Ring to Frame 9
Figure 9: Reticle Damage at the Guard Ring (the Ring of Fire) 10
Figure 10: Atomic Force Microscope Images of Various Damage Levels on One Structure of a Canary Reticle 10
Figure 11: Numerical Simulation of Voltage Contours on the Reticle Shaped By Adjacent Objects 11
Figure 12: Pellicle Location 12
Figure 13: A Schematic of the Main Components of an EUV Lithography System 12
Figure 14: Airflow With a Perforated Floor 13
Figure 15: Airflow in an Edge Return Cleanroom 14
Figure 16: A Teflon Cassette 14
Figure 17: A PEEK Cassette 15
Figure 18: An Open Cassette Process Tool Input Port 16
Figure 19: An Open Cassette Tool With Four Dissipative Cassettes Loaded 16
Figure 20: A SMIF Pod 17
Figure 21: A SMIF Loader 17
Figure 22: A FOUP With Wafers 18
Figure 23: A 300-mm Tool With an EFEM 18
Figure 24: The Inside of an EFEM 19
Figure 25: Mechanism for Loading and Unloading FOUPs From the OHV 20
Figure 26: A PGV 20
Figure 27: Cross-Section Depicting FEOL Device on Wafer Frontside and BSPDN Power, Ground Contacts, and Wiring 21
Figure 28: 2.5D and 3D ICs 22
Figure 29: Various 2.5D and 3D Stacking Techniques 22
Figure 30: Roadmap of CDM Target Levels for D2D Interfaces 23

EOS/ESD Association, Inc.'s White Paper – Electrostatic Discharge (ESD)/Electrostatic Attraction (ESA) Considerations in Semiconductor Wafer Fab and Associated Facilities

1.0 INTRODUCTION AND PROBLEM STATEMENT

The purpose of this document is to present the differences between ANSI/ESD S20.20 (and the similar IEC 671340-5-1) requirements and recommendations for best practices for electrostatic discharge (ESD) / electrostatic attraction (ESA) control in semiconductor wafer fab and mask house facilities.

Several semiconductor integrated device manufacturing (IDM) representatives have stated that their customers have requested that the IDMs provide proof and/or certification that their established ESD/ESA control program is sufficient for their respective semiconductor manufacturing processes.

ANSI/ESD S20.20 has been in place for over 24 years to establish a certifiable ESD control program for electronics manufacturing facilities that handle and process ESD sensitive electronic components. Typically, ANSI/ESD S20.20 has not been used to certify semiconductor wafer fab and mask house facilities. However, other documents published by SEMI that address best practices for such facilities are presented in this document.

While semiconductor fabs have some ESD/ESA controls, most do not have a certified ANSI/ESD S20.20 ESD control program. ESD/ESA control methodologies in a fab are covered in different areas of responsibility (quality, manufacturing, process control, tool maintenance, etc.), so it can be challenging to pull together a consensus document that would prove that the facility has proper controls in place for all ESD/ESA risks.

Besides ESD/ESA risks to products, an electrostatic shock to personnel, although not usually causing injuries, can cause a startled reflex, perhaps damaging nearby objects, causing pain, or being a nuisance. The proper layout of a building greatly reduces the effects of ESD, but when changes are made, ESD issues may arise if not considering their potential. Materials or solutions that seem appropriate from a non-ESD perspective may not be safe from an ESD perspective and end up causing problems for personnel (for example, gym pads for padding, floor wipes for cart cloths, etc.). People are the most important element of effective ESD control. Therefore, awareness of what ESD is and how to prevent it must always be considered.

This document reviews ESD/ESA challenges, considerations, and best practices in semiconductor manufacturing. It compares and contrasts semiconductor wafer and mask house manufacturing ESD/ESA best practices to those for electronics manufacturing and assembly, which ANSI/ESD S20.20 is designed for. Other areas closely linked to a semiconductor fab, like die-to-die and wafer-to-wafer bonding, reticles, and backside power delivery networks, are also discussed. Standards and limits may be addressed in later documents.

2.0 CURRENT STATUS OF ESD/ESA CONTROLS IN ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT MANUFACTURING FACILITIES (NON-SEMICONDUCTOR FABS)

2.1 ANSI/ESD S20.20 Overview

ESD control programs, as defined in ANSI/ESD S20.20, are based on three fundamental principles for handling ESD sensitive (ESDS) components in an ESD protected area (EPA):

- Ground or bond all conductors together.
- Control charge on all process essential insulators.
- Use protective packaging for transit and storage.

A detailed ESD control plan document that addresses administrative and technical requirements must be developed to implement these three fundamental principles.

For the administrative requirements, the organization must complete the following:

- Establish a written ESD control plan document that addresses all aspects of the ESD control program.

- Establish a training plan and associated education program that supports the written ESD control plan document for all personnel.
- Establish a product qualification plan to ensure the ESD control items used in the ESD control program meet the requirements of ANSI/ESD S20.20 as tested per the appropriate standard test method.
- Define a compliance verification program that ensures ESD control items meet the requirements defined in ANSI/ESD S20.20 and tested per ESD TR53.

The main technical requirements of the ESD control plan are as follows:

- Ground or bond together all ESDS items, personnel, and conductors that come into contact with ESDS items.
- Handling of ESDS items without ESD protective packaging shall be performed in an EPA.
- A packaging plan shall be established to define packaging requirements inside and outside the EPA.

Semiconductor fabs are, for the most part, automated, with little or no human contact with wafers. However, there are several specific areas in which ESD might be a concern and which are potentially considered as an EPA. The EPAs also need to consider ESA risks. These include wafer probes, bare reticle handling/inspection, and finished wafer shipping/handling. These areas require clear EPA demarcation. ESDS items shall be packaged in ESD protective packaging when taken out of the EPA.

2.2 SEMI E78 (Mini-Environment), E129 (Larger Fab- Cleanroom), E163 (Reticle)

Semiconductor Equipment Manufacturing International (SEMI) has published many documents that support the semiconductor manufacturing industry. Three documents published related to the measurement and control of electrostatic charge are:

- SEMI E78 - Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment
- SEMI E129 - Guide to Assess and Control Electrostatic Charge in a Semiconductor Manufacturing Facility
- SEMI E163 - Guide for the Handling of Reticles and Other Extremely Electrostatic Sensitive (EES) Items within Specially Designated Areas

All three documents address static charge issues focusing on different items. There is significant overlap, but these documents make up a good suite of documents to assist manufacturers, original equipment manufacturers, and other suppliers to the industry in developing static control programs for semiconductor wafer fabrication facilities.

2.2.1 SEMI E78

SEMI E78 is "equipment focused" and provides guidelines for semiconductor equipment manufacturers when designing, building, and testing equipment such as wafer handling systems and similar equipment. It provides methods for semiconductor manufacturers to check equipment performance and verify its conformance with procurement specifications. The performance specifications on static charge limits are tied to the International Roadmap for Devices and Systems (IRDS).

In addition to the main document, SEMI E78 also has an extensive set of appendices:

- Appendix 1 – Developing the Recommendations for Electrostatic Levels
- Related Information 1 – Static Charge Problems – ESD Damage, ESA, and Equipment ESD Issues
- Related Information 2 – Static-Control Methods
- Related Information 3 – Example for Adding Electrostatic-Compatibility Requirements to Purchasing Documents for Manufacturing Equipment
- Related Information 4 – Field-Induced Damage Mechanisms in Reticles

2.2.2 SEMI E129

SEMI E129 is more "factory focused". It provides guidelines to semiconductor manufacturers and cleanroom facility designers when designing and building manufacturing facilities to control static charge levels below what is needed during semiconductor manufacturing. The International Roadmap for Devices and Systems (IRDS) defines the levels of allowable static charge in the facility based on the technology node being manufactured. Test methods are provided to verify that all facility items meet target static charge levels, such as:

- Product, reticles, and carriers
- Facility construction materials, including furniture
- Personnel
- Packaging and transport of materials
- Equipment (pointing to SEMI E78)

In addition to the information provided in the main document, several appendices provide additional useful information:

- Appendix 1 – Developing the Recommendations for Electrostatic Levels
- Related Information 1 – Static Charge Problems – ESD Damage, ESA, and Equipment ESD Issues
- Related Information 2 – Static-Control Methods. (This is a listing of many external documents available for static control and a general discussion found in basic static control training and documentation)
- Related Information 3 – Measuring Electromagnetic Interference from ESD

2.2.3 SEMI E163

The purpose of SEMI E163 is to be a complementary document to E78 and E129 for handling items extremely sensitive to electrostatic effects, particularly electrical fields. Reticles have been identified as being one of these items.

SEMI E163 defines testing procedures similar to SEMI E129 and SEMI E78 but focuses on electrical field mitigation through ionization and shielding rather than grounding. Grounding has been identified as a risk for reticles and similar structures.

A large appendix to SEMI E163 discusses computer simulation of electric field interactions with reticles.

3.0 SEMICONDUCTOR MANUFACTURING ESD/ESA CHALLENGES/CONSIDERATIONS

3.1 ESA-Related Contamination

3.1.1 Electrostatically Driven Micro-Contamination

Unlike electronic printed circuit board (PCB) assemblies and packed semiconductor devices, the greatest detriment to successful manufacturing of semiconductor front end (wafer level manufacturing) is electrostatically attracted contamination in the cleanroom rather than damage due to electrostatic discharge. Theoretically and experimentally, it has been shown that electric fields drive microparticles [1] and represent a contamination hazard.

The speed at which particles drift toward a charged object through the air is a function of the field strength and the particle size. The difficulty in grasping the effect is that macroscopic (≥ 1 mm) particles are insignificant except at very high electric fields, which do not occur in typical manufacturing areas. In contrast, microscopic particles (≤ 1 mm) are strongly driven by modest electric fields. In [2], it is shown that the forces on an aerosol are diffusional, gravitational, and electrical. The parameter "deposition velocity" is a measure of the effect of each of these forces in the microscopic aerosol (see Figure 1). It accounts for particles colliding with air molecules and recoiling. Donavan et al. [2] calculate that the attraction of 1-mm particles to a charged wafer with a moderate field of 1000 volts/inch (40 kilovolts/m) at its surface is roughly the same strength as that of gravity.

In contrast, for a 0.1-mm particle approaching the same charged wafer, the electrostatic forces are 100x that of gravity on the particle. The difficulty is that the forces on microscopic particles are unrelated to those on larger particles. Thus, the concept of electrostatically driven small particles is not completely intuitive.

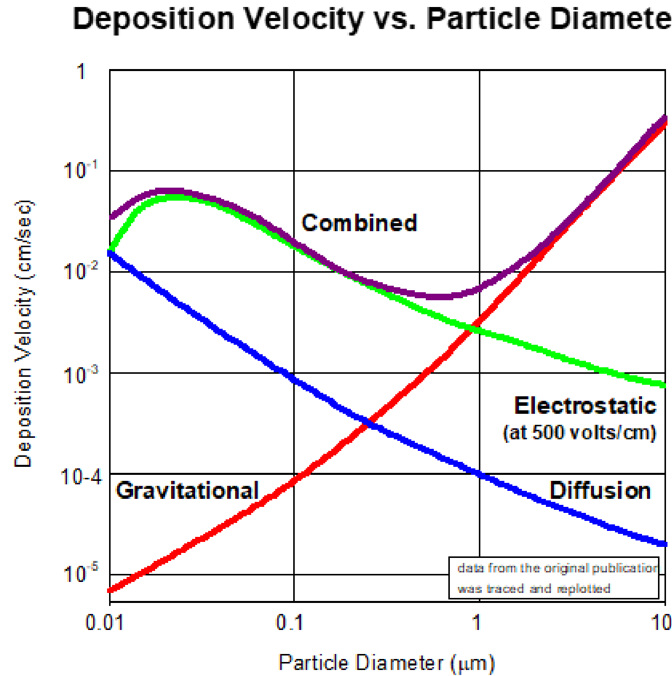

Figure 1: Calculation of Various Deposition Velocities [2]

3.1.2 Electrostatic Fields

This is complicated by the fact that the electric field extends from a 300-mm charged wafer by more than 300 mm (see Figure 2). Further, the electric field surrounding the wafer is invisible. That means a modestly charged wafer draws the particles near it out of the atmosphere.

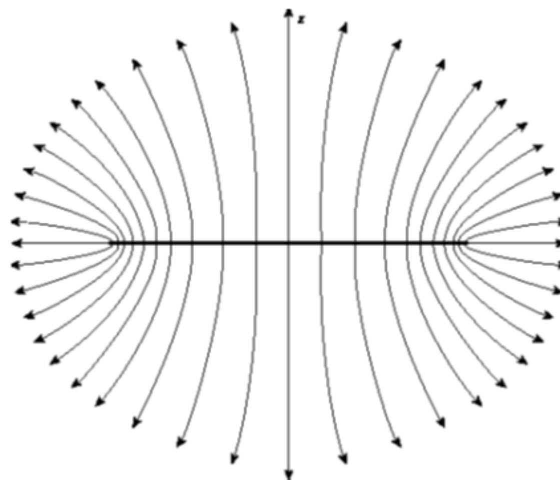

Figure 2: Field Lines from a Charged Wafer

3.1.3 Charges in the Environment

While the micro contamination caused by charged wafers is treated in the literature, other field-based contamination effects must be dealt with in the semiconductor fab. A charged object like a mini-environment wall also produces electric fields which extend from the wall. Further, the walls of a process tool are larger than the wafer it encloses, so the fields extend further than those from the wafer itself. These field lines often defeat the cleansing action of unidirectional airflow within the process tool. Charged windows or walls create horizontal forces on airborne contaminants and cause these to move perpendicular to the unidirectional airflow of a cleanroom.

3.1.4 Field Penetration of Insulating Enclosures

It is also important to realize that electric field lines penetrate insulating material. That means that a charged object in the vicinity of a plastic enclosure, like a standard mechanical interface (SMIF) or a front opening unified pod (FOUP), passes electric field lines that penetrate the enclosure. Any particles on the inside walls of the enclosure can be electrostatically dislodged and then land on the wafers. For this reason, in a mini-environment fab, wafers and reticles stored in protective plastic boxes are not safe from contaminating forces from externally generated fields that intersect the boxes. Charges on objects in the environment, such as windows, walls, and curtains, are a potential contamination hazard and must be eliminated (see Figure 3).

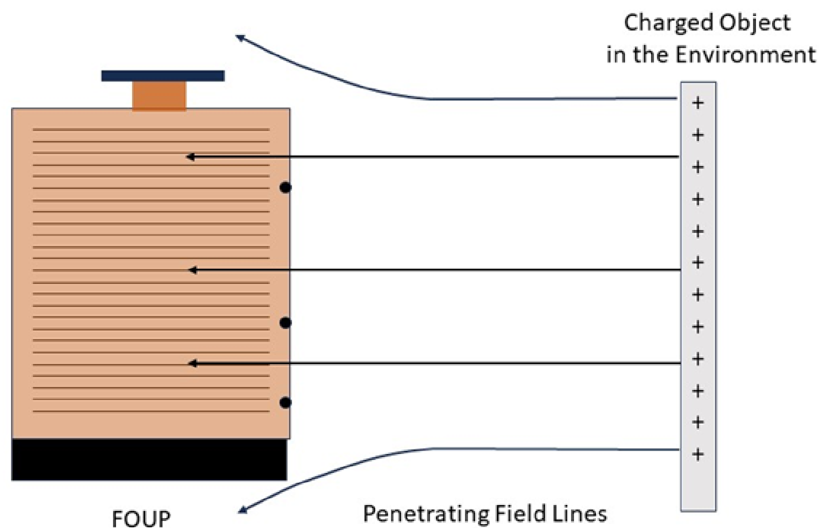

Figure 3: Electric Fields Penetrating the FOUP Wall

3.1.5 Moving Charges and Moving Grounds

An object with charge on it carries its electric fields with it. This can be, for example, a plastic chemical cart moving through a bay of the fab. As the cart approaches a cassette, field lines point toward or away from the cassette. After the cart passes, the lines point in the opposite direction. Consequently, particles are pushed back and forth by movements in the fab and can easily be broken loose to go hunting for a wafer to contaminate. This is very much like the action of an agitator in a washing machine.

Conversely, if the object is a grounded conductor, the field lines from an adjacent charged object terminate on the conductor and, if moving, have the same effect on contamination as the moving insulator.

3.1.6 Electrostatic Bonding

Moderately charged particles that land on a wafer can be electrostatically bonded to the wafer. This effect is stronger for smaller particles. The particle sits on the surface of the wafer and induces an equal image charge of opposite polarity since the wafer acts as a mirror. The force is shown in Figure 4 for 1-nm to 200-nm particles. This force is eight to nine orders of magnitude greater than gravity on the particle! This means that even minimally charged particles may not be removed from the wafer by any conventional means of cleaning. Low particle removal efficiency is well known [4], and this Coulomb force can explain this effect.

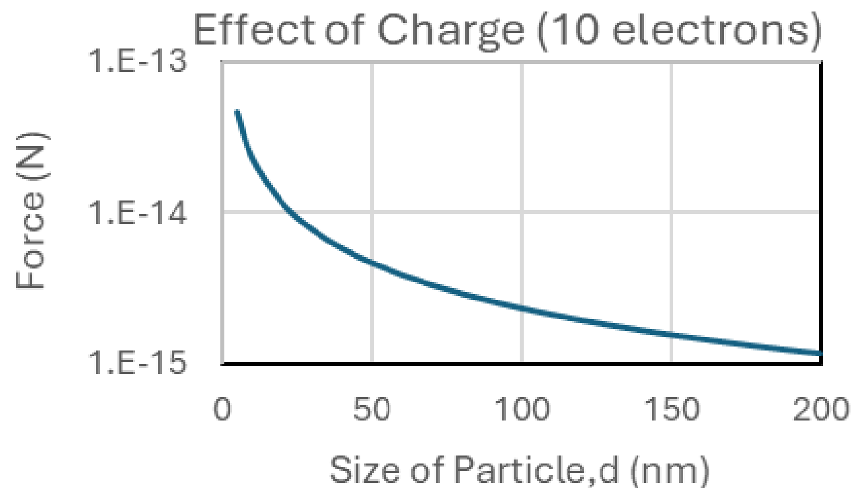

Figure 4: Force on a Particle With Ten Electrons of Charge

NOTE: $1.E^{-13}$ is 1.0×10^{-13}

3.1.7 Rules for Controlling Electrostatically Driven Contamination

It is clear from the above discussion that dealing with electrostatic forces plays a major role in contamination control. This means that the wafers being processed must be kept to a low level of charge. According to SEMI E78 [5], for 2023, state-of-the-art wafers with a critical dimension or node of 8.9 nm are limited to an electrostatic field of 8.9 volts/cm in the vicinity of the wafer (electrostatic damage) and 0.12 nC (contamination control). Charge levels should be measured with a large Faraday Cup capable of holding a 300-mm wafer, and fields should be measured using an appropriate instrument such as an electrostatic voltmeter. These are extremely stringent requirements and are difficult but possible to achieve.

3.2 Reticle Handling

3.2.1 The Physics of Photolithography

Semiconductor front-end manufacturing utilizes photolithography to project reticle patterns onto the wafer surface. An image is projected onto the wafer surface so that the pattern on the wafer is much smaller than the pattern on the reticle. Reticles are typically 150 mm x 150 mm x 6 mm (6 inches x 6 inches x 0.25 inches). Reticles are very sensitive to electrostatic fields, and a damaged reticle causes non-functional or marginally functional components to be manufactured.

Every year, new chip designs are created that utilize smaller and smaller feature sizes (critical dimension or CD) to advance the performance and economics of the manufactured components. These modern designs place greater demands on the optical technology required to create such small structures. This requires a higher resolution, which leads to more fragile reticles. ESD sensitivity grows with smaller features

The principle of patterning with lithography is straightforward, although the details become more complex each year. The pattern from the reticle is projected onto the wafer surface as either a negative or positive image (see Figure 5). Achieving good yield with photolithography demands perfect reticles.

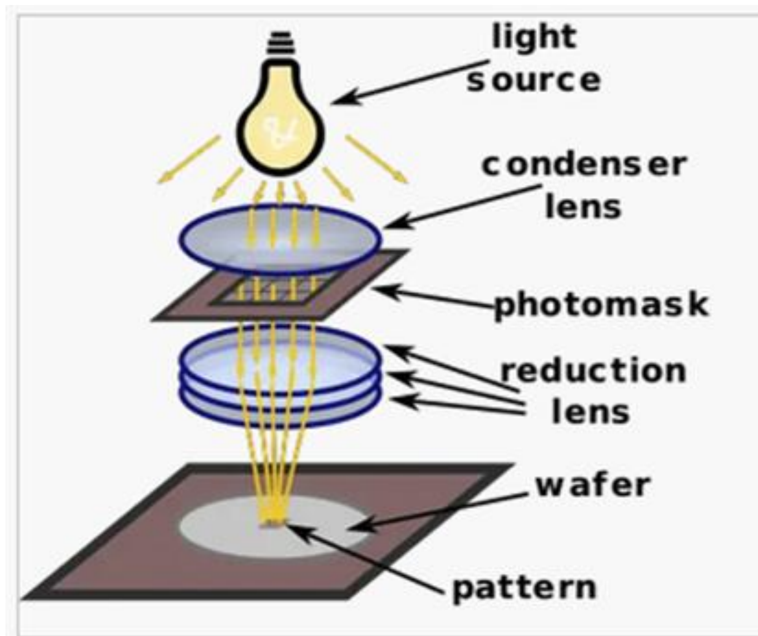

Figure 5: Principles of Photolithography

The structures on the reticle surface are quite small and fragile. If any structure on the reticle becomes damaged, the foundry mass produces chips that either work with limited functionality (under-spec products and "walking wounded") or chips that do not function at all. Technology does exist for repairing reticles, but until the reticle is scanned to reveal damage or parts come off the production line damaged, the fab lithography engineer is unaware of the issue and the need for a replacement. The total cost of a damaged reticle is quite large.

The technology employs monochromatic light and precision optics to reproduce the pattern from the reticle to the wafer. In the past, visible light was used to create patterns, but as designs moved to smaller and smaller features, the wavelength of visible light became a challenge. It became necessary to use shorter wavelengths to achieve the smaller size pattern (see Figure 6).

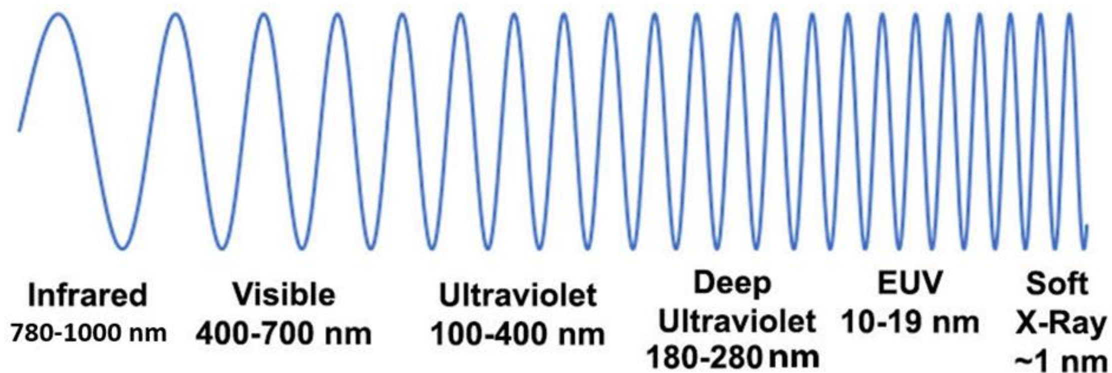

Figure 6: The Electromagnetic Spectrum Used in Photolithography

The limiting factor for photolithography is diffraction. This effect occurs because light bends as it passes around small structures like those on reticles. The incident light passing one of the structures on the reticle interacts with light passing around adjacent structures (see Figure 7). Certainly, a simple image projected onto the silicon does not produce an image suitable for a CD of 20 nm. Phase shift technology must be used to image such structures.

Two techniques push the minimum feature size at or beyond the diffraction limit. One is to put Molybdenum-Silicon alloy on the edges of the quartz structures (called MoSi reticles). This introduces phase shifts, which can be made to sharpen the silicon image. The other is for the optical designer to "work backward" to determine what pattern must be placed on the reticle to get the required image. This involves adding extra small structures very close to the pattern on the reticle. These extra structures are quite small and, hence, fragile. This is called optical proximity correction (OPC). MoSi and OPC reticles have very small features that are more susceptible to electric field damage than traditional chrome on quartz reticles. The effects of an electric field are discussed later.

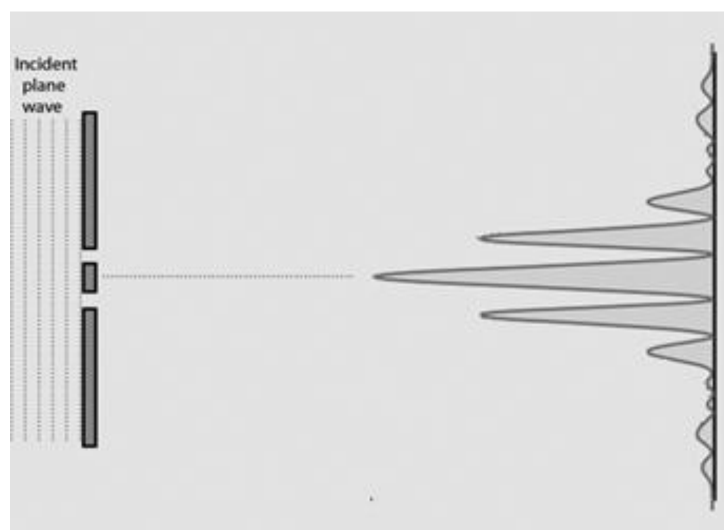

Figure 7: Diffraction With Constructive and Destructive Interference

Most of the chips manufactured today have modern feature sizes (<< 100 nm) and utilize deep UV (DUV) light sources of 365 nm, 248 nm, or 193 nm (along with OPC and MoSi). That technology has reached its limit, and new technology is required to print even smaller structures. The next step is extreme ultraviolet lithography (EUV), which will be discussed later.

3.2.2 Transmission Photolithography

Lithography from the visible spectrum down to the ultraviolet (≤193 nm) utilizes transmission techniques. This includes OPC reticles. All such structures consist of chrome on quartz. The quartz gives the reticle excellent dimensional stability, and the chrome is relatively easy to machine with a laser. Such structures represent the majority of reticles in use today. Since the reticles comprise huge numbers of tiny conducting structures on a very good insulating surface, they are highly susceptible to ESD damage from electric fields.

A transmission-type reticle is shown in Figure 8. The reticle has a chrome ring around its periphery called a guard ring. Typically, scanning a production reticle with a guard ring shows the most frequent damage between the structure's edges and the guard ring. See Figure 9. This early evidence led to the conclusion that electrostatic discharge caused the damage. It is well known that conductors that are close together withstand very little potential difference without sparking [6,7]. More comprehensive studies [8,9] using the Canary Reticle tool showed [10] that damage resulted from induced voltages on individual chrome structures. The Canary Reticle was a reticle layout that maximized the field sensitivity of the chrome structures on the substrate; the mechanism for damage is voltage induction caused by electric fields across the reticle surface. Fields are caused by a surface charge on the quartz but more commonly by external sources such as a charge on reticle pods or adjacent charged objects. The field lines are shaped by grounded structures such as slots in a reticle stocker, grounded guard rings, or any grounded structure on the reticle storage pod.

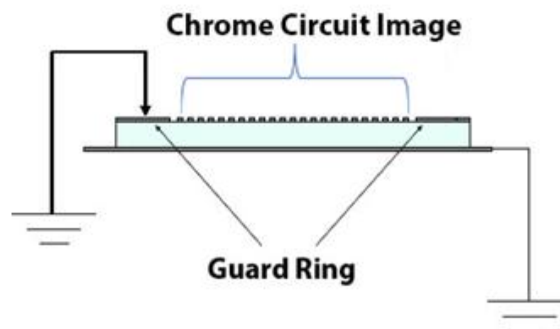

Figure 8: Image Showing the Reticle Has Many Chrome Pieces and a Guard Ring to Frame

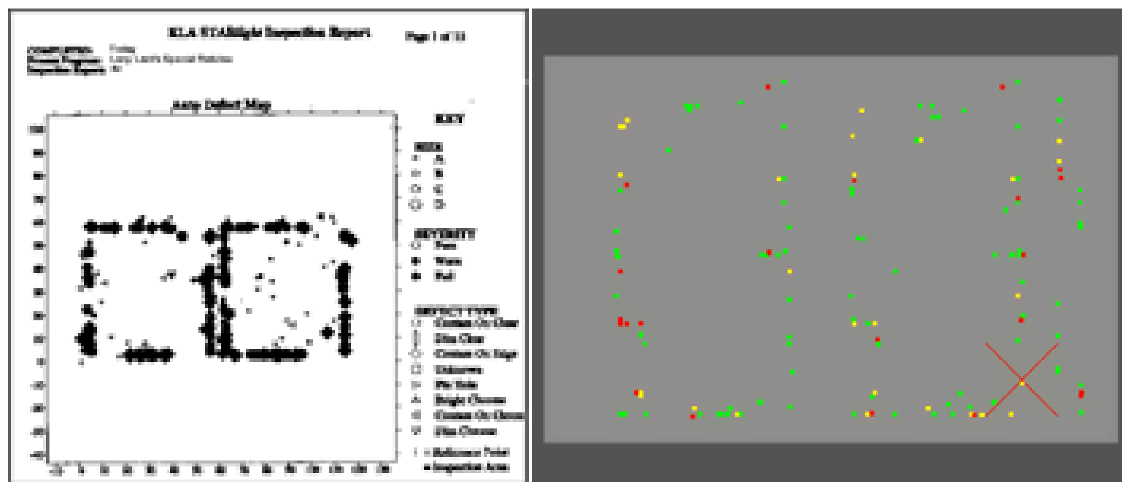

Figure 9: Reticle Damage at the Guard Ring (the Ring of Fire)

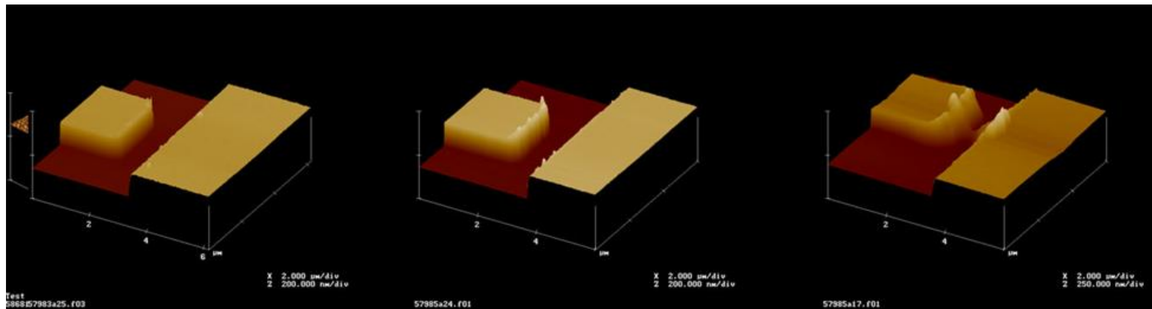

Figure 10: Atomic Force Microscope Images of Various Damage Levels on One Structure of a Canary Reticle

Independent analysis of the Canary structures and numerical simulations have been done [11] (see Figures 11 and 12) on the reticle/reticle pod system [12]. These studies have allowed the calculation of voltage contours on the reticle based on charged objects and grounds in the environment. They have produced a variety of conclusions. These include:

1. Reticle damage is caused by electric fields from nearby charged objects. Care, therefore, must be taken to avoid floating conductors and charged insulators in the neighborhood of the reticle, such as the reticle stocker.
2. Grounding the guard ring promotes reticle damage.
3. Charges adjacent to a reticle drive damage on the reticle.
4. Charge on a reticle pod drive discharges on the reticle.
5. Grounds in the immediate vicinity of a reticle will "amplify" the electric field strength at the reticle and enhance the prospect of discharge on the reticle surface.
6. Besides reticle damage due to electrostatic discharge, another damage mechanism called electric field migration (EFM) is a hazard. Damage accumulates with the presence of a constant electric field over time.

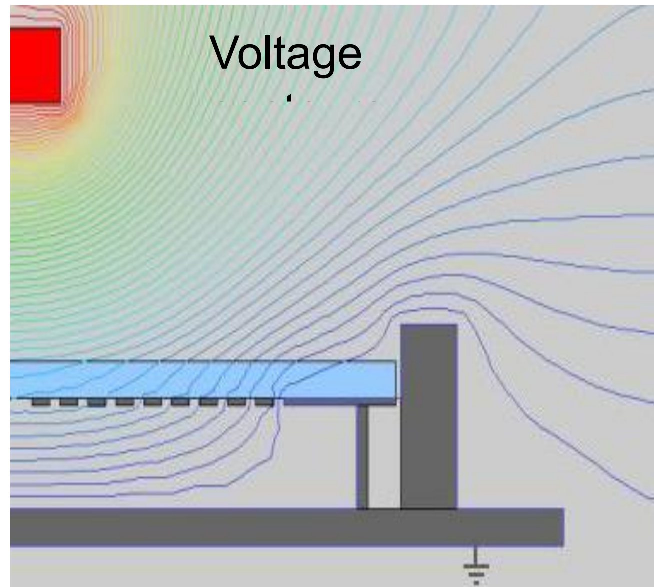

Figure 11: Numerical Simulation of Voltage Contours on the Reticle Shaped by Adjacent Objects
(Picture Credit: Gavin Rider)

Some reticle pods are made of dissipative plastic and, as such, carry away surface charge when grounded. This storage structure is a good idea as it eliminates one source of stray fields. Two items of note are:

- The dissipative storage pod must be grounded to dissipate the static surface charge on the pod.
- A dissipative pod provides virtually no shielding from external electric fields in the area [13]. Any charge near a pod creates fields within the pod.
- A charged reticle in a grounded dissipative pod is an ESD discharge hazard.

Any debris on the surface of the reticle is projected onto the wafers being manufactured. Hence, microcontamination on the reticle surface is a detriment to manufacturing yield. For this reason, the reticle has a transparent plastic cover intended to keep such contaminates out of the focal plane. This reduces their impact on the production yield. These covers are called pellicles (see Figure 12). Two matters of note about the electrostatic properties of pellicles are important:

1. Pellicles are insulators and, as such, are susceptible to contamination due to ESA. Implementation of air ionization is important to keep them clean. This applies at the mask shop and the fab at the inspection tool. Unless care is taken to avoid all contact with the pellicle, air ionization should be implemented where the reticle pod is opened. Pellicles should be exposed to air ionization as part of the pellicle repair process.
2. As insulators, pellicles isolate the air volume between the pellicle and the reticle, so adding air ionization does not cleanse the reticle surface.

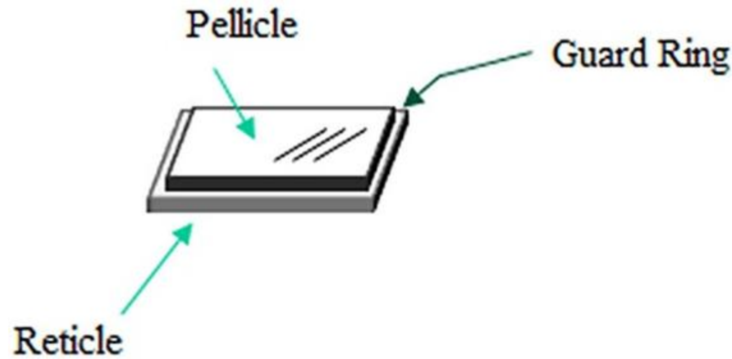

Figure 12: Pellicle Location

3.2.3 EUV (Reflection Photolithography)

This cutting-edge technology is emerging and used only by the highest technology fabs. The present technology implementation utilizes 13.5-nm photons to achieve the small feature sizes of very modern integrated circuits. It is performed in a vacuum since both air and nitrogen are opaque to EUV light. It uses reflections from the reticle surface since quartz is also opaque to 13.5-nm photons. Rather than lenses, EUV lithography utilizes non-planar mirrors to create negative magnification to achieve a small image size that reaches the wafer surface (see Figure 13). EUV reticles have pellicles for contamination control, just as transmission reticles do.

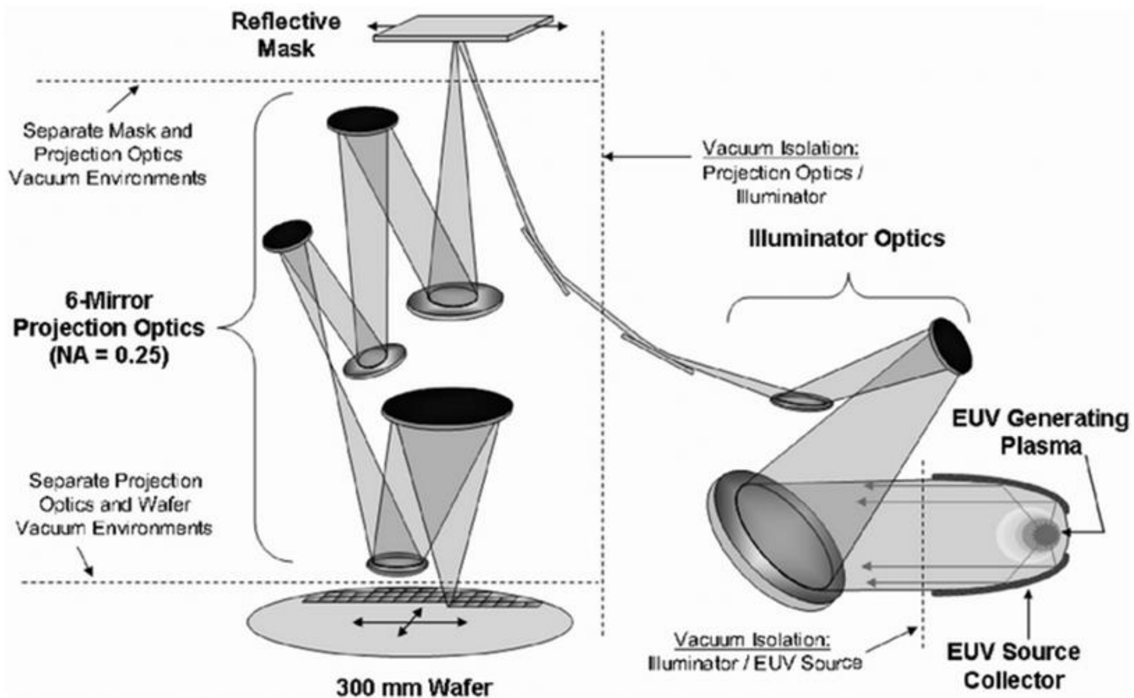

Figure 13: A Schematic of the Main Components of an EUV Lithography System

EUV technology has been studied at many national laboratories, but a few companies are commercially supporting this technology today.

3.2.4 Implementation

The rules discussed above are important to follow to avoid reticle damage issues. This means good static control practices are important in the reticle stocker and the exposure tool (stepper). These controls must also be applied to automated reticle inspection tools, manual microscope stations, laser repair tools, and pellicle replacement tools.

While a good static control program includes:

1. Eliminating insulators wherever possible.
2. Utilizing dissipative materials when possible
3. Using appropriate air ionization for the process required insulators
4. Grounding all conductors near the path of reticles

In the case of reticles, however, the following facts must also be taken into consideration:

1. Transmission reticles are made of quartz and chrome.
2. The quartz is a process-required insulator.
3. The chrome features are electrically isolated and, as such, cannot and should not be grounded.
4. The guard ring should remain floating, but air ionization should be used
5. The features on the reticle under the pellicle are electrically isolated and cannot be discharged by air ionization
6. Air ionization on the reticle surface must only be implemented when the pellicle is absent.
7. The volume between the pellicle and the reticle cannot be discharged with ionization because it is isolated.

3.3 200-mm Versus 300-mm Fabs; Open Cassette Versus SMIF/FOUP Carriers

A cleanroom used for semiconductor front-end manufacturing utilizes a controlled airflow of highly filtered air to cleanse the wafers. Details of the configuration of this airflow determine the configuration of the cleanroom. These cleanrooms employ a HEPA or ULPA matrix of fan-filter units (FFU) and a return air system, either a perforated floor or a set of louvers at the floor's edges (see Figures 14 and 15).

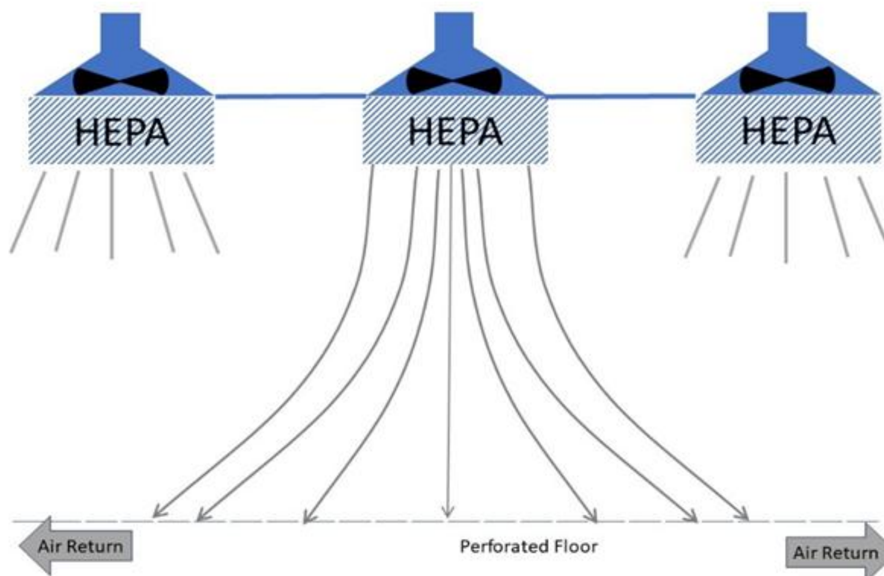

Figure 14: Airflow With a Perforated Floor

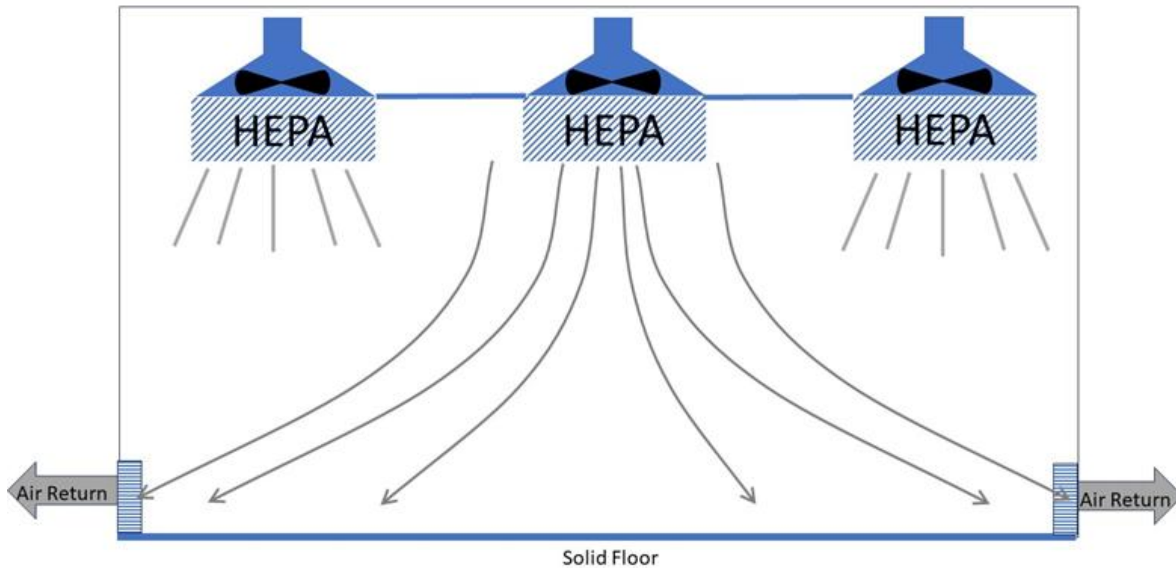

Figure 15: Airflow in an Edge Return Cleanroom

Early and more recent cleanrooms utilize this airflow, although the perforated floor version is generally better from a contamination control standpoint.

In the 1980's, wafers were 150 mm in diameter and stored in wafer cassettes. PTFE was believed to be a good choice for cassettes since it is impervious to most caustic chemicals and easy to wash and clean. As can be seen in Figure 16, PTFE is incredibly electronegative and tribocharges aggressively.

Figure 16: A Teflon Cassette

There are electrostatically improved cassettes for 150-mm and 200-mm wafers made of dissipative plastic, most often Polyether Ether Ketone (PEEK) (see Figure 17). These cassettes provide a path to ground for the wafers they contain. Good practice dictates that dissipative cassettes are used for 150-mm and 200-mm wafers wherever possible, depending on the details of the process. Dissipative cassettes are incompatible with acid and high temperatures. Thus, these cannot be used in acid etch or warm water cleaning like a spin rinser drier (SRD).

Figure 17: A PEEK Cassette

Open cassette fabs are cleanrooms that use this type of cassette without an enclosure. Open cassette fabs with dissipative cassettes benefit greatly when the nest they sit in at each tool provides a path to ground for the cassette (see Figures 18 and 19). These also benefit from ceiling air ionizers, which dissipate any surface charge from insulators on the surface of the wafer. Grounding the nest provides no benefit when using Teflon cassettes, but ceiling ionizers are good for minimizing contamination on the wafers in PTFE cassettes.

Figure 18: An Open Cassette Process Tool Input Port

Figure 19: An Open Cassette Tool With Four Dissipative Cassettes Loaded

During the 200-mm wafer era, a new configuration called a mini-environment configuration was adopted in many fabs. This involved using sealed containers to hold wafer cassettes full of wafers. These containers are called standard mechanical interfaces (SMIF) (see Figures 20 and 21). This way, the wafers and cassettes are isolated from the fab atmosphere. Employing ionization within the SMIF pod is impractical, but good practice dictates that air ionization is strategically placed within the process chamber. The cassette is deployed by lowering the base of the SMIF with the cassette attached to the process chamber. The top of the SMIF remains in place and serves as a seal for the process tool. When the process step is complete, a robot raises the cassette back into the SMIF enclosure. An operator manually transfers the full SMIF to the next tool in the process. Because of the isolation provided by the SMIF, there is a lower contamination risk than the open cassette fab, and it requires less stringent cleanroom cleanliness.

Figure 20: A SMIF Pod

Figure 21: A SMIF Loader

With the evolution of the 300-mm wafer fab, the mini-environment isolation concept has evolved and been strengthened. An enclosure designed to hold 25 300-mm wafers has been defined as a FOUP (see Figures 22 and 23). The FOUP holds up to 25 wafers horizontally in a static dissipative structure. The FOUP has a front cover that seals the wafers inside. The mount for the FOUP at each tool is designed to make electrical contact with the liner holding the wafers, thus grounding the wafers.

Figure 22: A FOUP With Wafers

Figure 23: A 300-mm Tool With an EFEM

The sealed FOUP is transferred from tool to tool. At each tool, it docks to a structure that feeds the wafers into the process chamber. This structure is called an equipment front end module (EFEM).

The opening from the EFEM to the process chamber is called the mail slot (see Figure 24). When a FOUP is docked to an EFEM, the automation within the EFEM removes the FOUP cover and lowers it out of the way. This allows the robot within the EFEM to access the wafers and load these into the process chamber individually. At the end of the process, wafers are returned to the FOUP, and after all are returned, the FOUP cover is raised and docked to the FOUP.

Figure 24: The Inside of an EFEM

Since a full FOUP weighs over 18 kg (40 pounds) and the wafers are so large and fragile, the FOUPs are rarely moved by operators. Instead, these are automatically lifted to an overhead track called the overhead vehicle (OHV), transported to the next tool, and lowered onto its EFEM load port (see Figure 25). Sometimes, FOUPs are transferred by an operator who uses a cart designed for the job. These conveyances are called personnel-guided vehicles (PGVs) (see Figure 26).

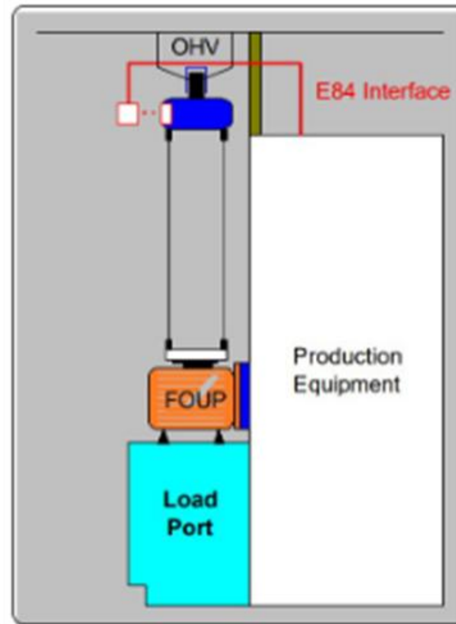

Figure 25: Mechanism for Loading and Unloading FOUPs From the OHV

Figure 26: A PGV

The mechanism of airborne particles landing on wafers between tools in a FOUP is eliminated because the wafers are isolated from the cleanroom's air. Thus, the benefits from ceiling ionization are eliminated. There remains the mechanism of electrostatic movement of particles from the inner walls of the FOUP to the wafers. For this reason, static electric fields should be eliminated by the standard rules of static charge control.

- Eliminate insulators wherever possible by replacing them with grounded dissipative material.
- Ground all conductors wherever possible.
- Ionization should be placed within the EFEM and, if practical, within the process chambers of all tools.

Photolithography bays follow different rules. Areas containing reticle stockers or photolithographic steppers should have ceiling ionizers in addition to the above-mentioned steps.

3.4 Backside Power Delivery Network and ESD Implications

Backside power delivery networks (BSPDN) take advantage of the previously unused area on the backside of semiconductor wafers by running wiring (rails) through this region (see Figure 27). Contact to the front side of the wafer devices is made using nano through silicon vias (nTSVs).

The objective of a BSPDN is to reduce the area required in standard cells for back-end-of-line (BEOL) power and ground wiring on the front side of a semiconductor logic chip. Moving the power and ground rails to the backside of the wafer results in a much more efficient arrangement of the interconnects and, therefore, helps to shrink the sizes of the logic standard cells. Because backside power networks can be designed larger than the front side of wafers and because these are closer to the device, the result is a significant reduction of the on-chip IR drop.

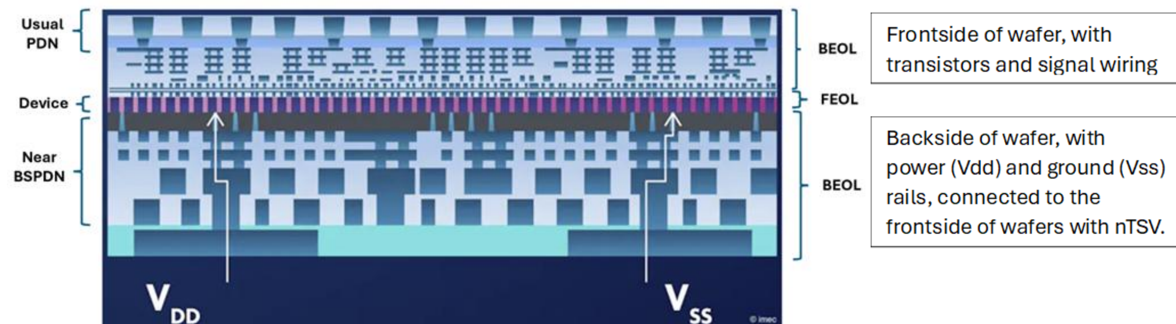

Figure 27: Cross-Section Depicting FEOL Device on Wafer Frontside (top of image) and BSPDN Power, Ground Contacts, and Wiring (bottom of image)

The processing of BSPDN structures uses the same tools as processing front metals. This requires implementing similar ESD process controls and procedures used on the front side of wafers, such as ionization and proper chuck/equipment grounding. In addition, antennae design rules for BSPDN must be modified to mitigate the impact of etch processing that can result in plasma damage to FEOL devices by placing antennae diodes.

Future development of BSPDNs could involve implementing ESD protection devices on the wafer backside and metal-insulator-metal (MIM) decoupling capacitors.

3.5 Die-to-Die and Wafer-to-Wafer Bonding

Heterogeneous integration (specifically, 2.5D and 3D stacking or bonding) is a semi-fab assembly technology that directly connects dies (also called chiplets) into one package. This leads to a much higher packing density, increased performance, and lower power consumption due to shorter connections. It can also give greater flexibility to meet the customers' needs as only the necessary chiplets are added to the overall integrated circuit (IC) package.

2.5D stacking involves placing multiple chiplets side by side on an interposer. The interposer connects the chiplets at a higher density than traditional printed circuit board (PCB) connections.

3D stacking involves placing multiple chiplets on top of each other. The connections between them are even shorter than 2.5D stacking, and the horizontal surface area is reduced as the chiplets are

stacked vertically on each other (see Figure 28). Note that the industry has started using the "hybrid bonding" technology next to micro-bump technology, which does not require soldering. Instead, the dielectric of the two chiplets is bonded, and the electrical connection is through direct copper-to-copper contact.

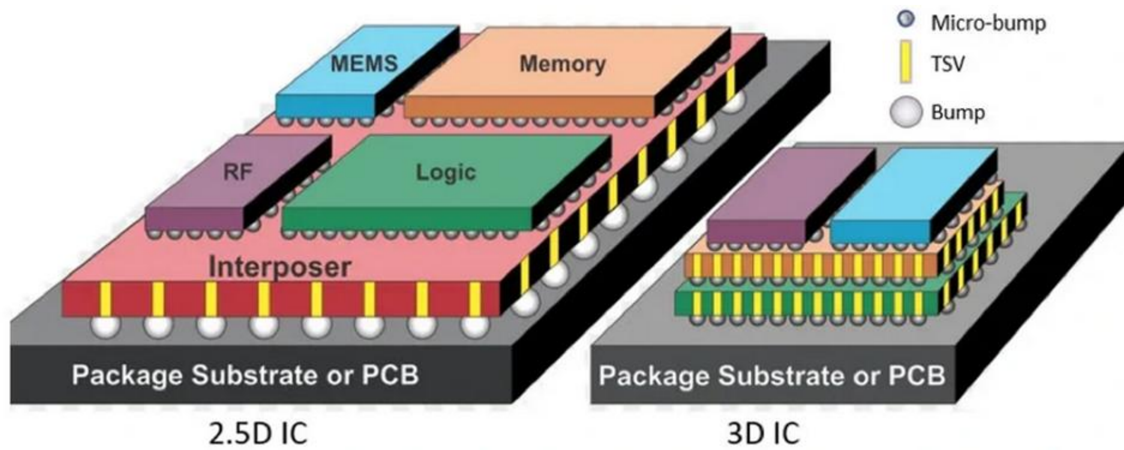

Figure 28: 2.5D and 3D ICs

In the factory, the 2.5D and 3D stacking can be accomplished wafer-to-wafer (W2W), chip-to-wafer (also referred to as die-to-wafer (D2W)), or chip-to-chip (also referred to as die-to-die (D2D)) (see Figure 29).

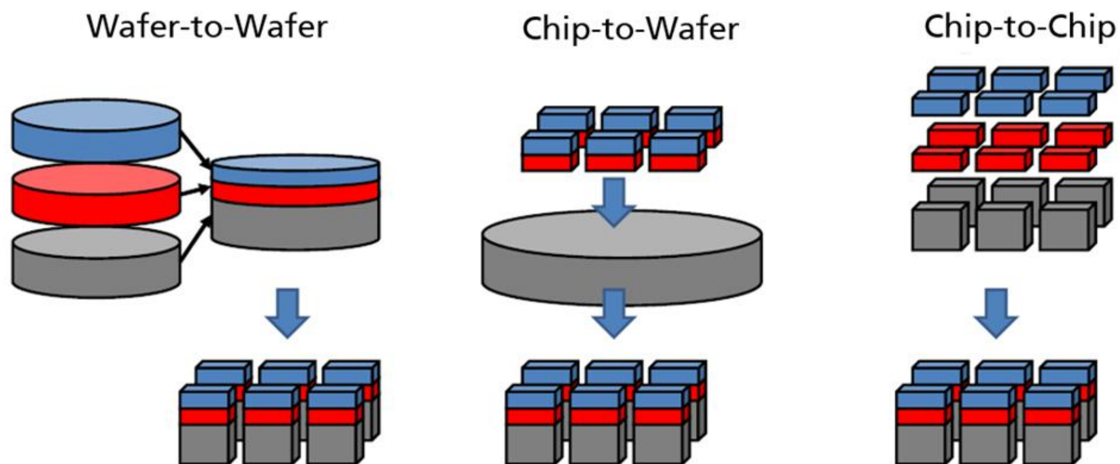

Figure 29: Various 2.5D and 3D Stacking Techniques

The ESD risk comes if the wafers, dies, or substrates being put together are at a different potential. The best way to prevent an ESD discharge is by grounding the objects being put together and using ionization. If this is not sufficient, a change to the process may be needed, like reducing the speed of the operation or using a dissipative material for tooling that contacts the potentially charged devices. [14]

Due to the large number of interfaces per IC, the internal ESD protection of each chiplet is limited. This has led to a reduction in the industry's ESD robustness targets. The Industry Council on ESD

Target Levels has published White Paper 2: A Case for Lowering Component-level CDM ESD Specifications and Requirements. Part II: Die-to-Die Interfaces. [15] This white paper presents an industry-wide survey on the need for a common roadmap for assessing the ESD risk of 2.5D and 3D stacking. Most of the information in this section is taken from this white paper and a few other reference papers.

The results of a CDM tester evaluating the ESD robustness of traditional ICs differ from the discharge of a chiplet in a CDM tester and the actual discharge during the 3D stacking process. This is primarily because the CDM tester pogo pin impedance does not exist in the real-world D2D discharge and thus gives a higher peak current at a given voltage. There are other ways to characterize the ESD robustness of D2D interfaces currently in development. These include:

- very fast transmission line pulse (VF-TLP)
- capacitively coupled TLP (CC-TLP)
- low-impedance contact charged device model (LICCDM)
- electromagnetic (EM) event detection with an antenna [16,17]

The interconnect pitch is also expected to drop below 10 µm soon, making direct TLP evaluations at the chiplet-level almost impossible. Some companies today package chips/chiplets into a "test" package for testing purposes. That kind of testing is always possible, but some argue it is not good because of the added package, which normally is not used.

To make matters more severe, the Industry Council white paper roadmap anticipates that the CDM target level starting in 2024 will be as low as 5 volts and eventually drop to 3 volts by 2028 (see Figure 30).

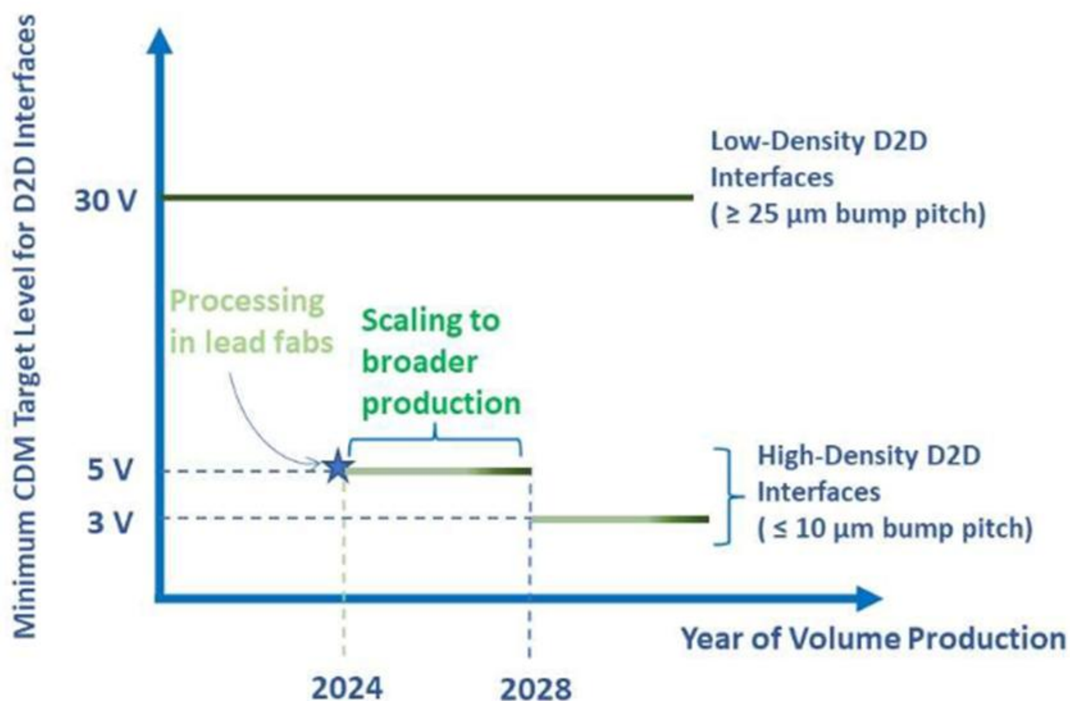

Figure 30: Roadmap of CDM Target Levels for D2D Interfaces

An effort has been made to measure die-to-die interface waveforms [16,18]. Discharge events have been shown to have a peak current from 100 milliamperes to over 1 ampere with a rise time from 10 ps to over 100 ps. The amount of discharge depends on things like initial source capacitance, the charge on the die, size, and design of the die.

There are no standards for determining the ESD protective measures needed in a production line for D2D interfaces. A standard with defined requirements would be impossible because it would be valid for one specific process step with one specific tool. There might also be differences in materials or the process itself that could affect the ESD risk. It is best to assess each process individually using the steps outlined in ANSI/ESD SP17.1 [19].

One useful advantage of the D2W and W2W designs is that the larger capacitance of the wafer creates a capacitive coupling of the die or wafers. This causes voltage suppression as the dies or wafers come together in assembly [17,18,20]. Some argue that there is still an exchange of charges, although the voltage is reduced. If so, this exchange of charges at contact is likely slower for the same reason.

Ionization is a primary way to reduce the charge on dies or wafers before assembly. As stated previously, the withstand voltages are as low as 5 volts. If not constantly monitored, ionizers must be carefully maintained to ensure the balance is kept as close to zero as possible, or the ionizer could charge the die or wafer beyond its withstand voltage [17]. Using "inherently balanced" ionizers, like soft x-ray ionizers (photon-ionizers) or alpha ionizers, could also ensure the balance is always zero.

4.0 GENERALLY ACCEPTED ESD/ESA CONTROL PRACTICES FOR A SEMICONDUCTOR FAB

Many of the same principles in ANSI/ESD S20.20 apply to semiconductor fabrication facilities. However, some of the key differences that affect the scope of ANSI/ESD S20.20 and a similar program in wafer fabrication facilities are driven by the ease and ability to inject damaging energy into the device. Devices with wire bonds, pins, and packaging can have energy more easily injected into the device's circuitry. Wafers, as they are being built, are typically more susceptible to ESA of particles than to damaging ESD. However, ESD events can still damage these, particularly those with the extreme energy seen when no static control principles are applied. In some cases, electrostatic surface voltages over 20,000 volts can be found in wafer fabrication facilities when no static control principles are used. Attenuating these fields can reduce the risk of damaging ESD events and the reduction of ESA on critical surfaces.

As the wafers near the final processing, moving to backend assembly operations, the focus on static control becomes more important for ESD than ESA. However, controls for both may still be needed.

This section focuses on controls commonly used for static control in semiconductor wafer fabrication facilities for ESA. Many of these controls also reduce the risk of ESD damage as well.

As stated in a previous section on ANSI/ESD S20.20, grounding those items is the primary method of removing charge from conductive materials. While this may sound simple initially, it can become more complicated as one investigates the details.

Tool surfaces and stainless-steel tables are common conductors that should be grounded. What may be less obvious is conductive wafer-handling robots that move and may be more difficult to ground. Other less obvious items are static dissipative materials used as part of tool surfaces, wafer carriers, FOUP, etc. Static dissipative items such as these must be grounded similarly to conductive materials to bleed off any accumulated charge.

Another conductive item addressed in ANSI/ESD S20.20 is personnel grounding. In more manual operations, particularly backend assembly and testing, the grounding of personnel is imperative. In wafer fabrication facilities, unless personnel are directly involved in handling the product, the grounding of personnel may not be as critical. However, the requirement for grounding personnel, such as wrist straps or static dissipative footwear on a dissipative floor (and the method to ensure a connection to the operator's skin), can be costly. Engineering must examine the pros and cons based on the infrastructure, amount of personnel involvement, charge generation on items, and many other factors.

If the decision is made to ground personnel, many other considerations must be evaluated. In most wafer fabrication facilities, grounding wrist straps is not desirable as tethering personnel to a common point ground can be unwieldy and dangerous.

When needed, personnel can be grounded through the floor/footwear system. It should be noted, though, that accomplishing grounding in a cleanroom garment system is not trivial and must be carefully engineered to work effectively through the life of the garment system. In addition, the floor must be conductive or static dissipative and designed to work with the footwear chosen to ground personnel. Other considerations are the conductivity of the garment systems, gloves, and hand tools to ensure all are grounded when handled.

One of the largest problems in wafer fabrication facilities is the prevalent use of charge-generating and accumulating insulative materials. Materials inert to the many chemicals used in wafer processing are needed in many processing locations. Many of these materials are insulative and accumulate significant charge when moved or handled. If possible, the best solution is to re-engineer the items with static dissipative materials. If these are made from static dissipative materials, grounding of the items must be considered. Windows in tools and EFEMs have traditionally been made from acrylic and similar materials and charge significantly when touched. Static dissipative versions of these materials are available and are becoming more prevalent in these applications.

However, many static dissipative materials may not be inert or clean enough for ultra-clean wafer processing. In addition, the wafers have insulative features that can attract contaminants through ESA. The best solution for these situations is to provide sufficient air ionization to neutralize the charge on insulative materials and the processed wafers.

Many different forms of ionization are used in wafer fabrication facilities for ESA and ESD control. EFEMs typically have ionization bars installed in the air stream above the wafer-handling robots. In manufacturing, room system ionization is utilized in many wafer fabrication facilities to control the charge on wafers and other insulative materials. In addition, room system ionization is sometimes used in the gowning rooms to reduce the charge on garments and airborne particles to prevent dragging contaminants into the process on garments. Likewise, equipment transfer rooms may have ionization (room and/or local blow-off ionization) to ensure that the material coming in through these rooms is as clean as possible before entering the fab.

One of the current requirements in ANSI/ESD S20.20 is that the offset voltage of all ionization must be less than ± 35 volts. This requirement stems from the need to control voltage on ungrounded conductive items, including printed circuit boards and packaged devices in contract manufacturers, backend assembly, test, and printed circuit board assembly operations. In most cases, this requirement is not needed in front-end semiconductor wafer manufacturing, and the benefit of using room and in-tool ionization that may not meet the ± 35 volts requirement far exceeds not using ionization. As stated earlier, in many cases, we are attempting to reduce ± 10 kilovolts or more to manageable levels of ± 100 volts in wafer production areas. It should also be noted that the demarcation between "front-end" and "backend" is becoming less clearly defined as 3D and chip-on-silicon processing is becoming more prevalent. Careful evaluation of the process steps and needs for static control must be done as the wafers near their final processing steps.

Packaging materials are another area where controls may be necessary. The packaging does not just apply to outgoing product packaging. Process chemicals, photolithographic cassettes, reticle carriers, and reticles are commonly made from insulative materials. These must be considered when evaluating the facility for static dissipative materials and ionization. The packaging design must also be considered when evaluating the risk of packaging and handling materials sensitive to ESD. Reducing the risk of personnel contacting areas sensitive to ESD damage by having a proper design of pickup/contact point(s) is desired. In-process packaging, such as FOUPs and wafer carriers, must also be considered. Ideally, these can be made out of conductive or static dissipative material that can be grounded. That is the first choice. Ionization may be needed, though, as often these must be made out of insulative materials.

Reticles are in a special category as these must be handled carefully; in many cases, putting these into a grounded carrier may worsen the risk of damage. More details can be found in the reticle section of this document.

Finally, another section of ANSI/ESD S20.20 that applies is compliance verification. A program must be implemented to ensure that items used for static control continue to work properly

throughout the item's life. All items used for static control must be checked regularly to ensure these are still working per the specifications.

5.0 COMPARISON OF ESD MANUFACTURING CONTROLS CERTIFIED ACCORDING TO ANSI/ESD S20.20 OR IEC 61340-5-1 VERSUS SEMICONDUCTOR MANUFACTURING ESD/ESA CONTROLS BEST PRACTICES

The purpose of the ANSI/ESD S20.20 standard is to address "the requirements necessary to establish, implement, and maintain an electrostatic discharge (ESD) control program for activities that manufacture, process, assemble, install, transport, package, label, service, test, inspect, or otherwise handle electrical or electronic parts, assemblies, and equipment susceptible to damage by electrostatic discharges…". As stated earlier in this document, some of the key differences that affect the scope of ANSI/ESD S20.20 versus an ESD/ESA control program in a front-end-of-line (FEOL: pre-dicing or packaging) semiconductor fab is driven by the ease and ability to inject damaging energy into the device. Finished devices with wire bonds, pins, and packaging can have energy more easily injected into the device circuitry, potentially causing catastrophic damage. In FEOL semiconductor fabs, wafers are predominantly susceptible to ESA-induced contamination, which results in yield loss. Semiconductor fab ESD/ESA best practice calls for controlling static charge levels in the regions where wafers transit in the manufacturing process and on the wafers. The primary reason for these controls is to reduce static charge-induced contamination in the manufacturing process that impacts product yields. A secondary concern is that ESD events in the fab can damage the wafers, impacting yields and device reliability. Finally, ESD events in the fab can cause ESD-induced electromagnetic interference (EMI). EM pulses propagating from such events can lead to in-tool computer controller interruptions, resulting in unplanned tool downtime and a major impact on fab productivity.

This document lists the three fundamental principles of handling ESD sensitive devices per ANSI/ESD S20.20. These three principles can also function as the basis for a FEOL semiconductor fab ESD/ESA control plan. Examples are illustrated as follows:

1. Ground or bond all conductors together. In the case of semiconductor manufacturing, this can be interpreted as tools and associated components that must be properly grounded and routinely certified. When a tool is moved, there must be a plan to recertify the tool grounding before wafer processing is restarted.
2. Control charge on all process essential insulators. Tool purchase specification documents must define requirements that, were possible, static dissipative materials be used instead of insulating materials and then be properly grounded. This is particularly important for tool windows from a contamination perspective. Where process required insulators are in the path of the wafer transit or on the wafers, ionization must be implemented to reduce static charge levels to ~ 100 volts. Ionizers should be designed to reduce static charge levels on wafers when they come out of the process, typically in an EFEM area. All ionizers must be tested when installed, and a maintenance plan with recurring calibration and verification tests must be established.
3. Use protective packaging for transit and storage. Semiconductor wafers in a fab are typically transported in static dissipative boxes (≤ 200-mm wafers) and in FOUPs for 300-mm wafers. FOUPs may or may not be static dissipative. However, most FOUPs have a grounded comb structure made of static dissipative material in which the wafers lie in a stack. This grounding extends outside the FOUP and is designed so that the FOUP comb is always grounded in transit in the automated materials handling system.

A semiconductor FEOL fab can use the principles of ANSI/ESD S20.20 to establish an ESD/ESA control plan following the three principles listed above. The plan would require tailoring to address special circumstances, such as grounding personnel when required to handle wafers and reticles in case these get lodged and must be extracted from a tool in an emergency.

To pursue ANSI/ESD S20.20 certification for a FEOL semiconductor fab, it would take significant resources to develop the plan document, establish the required training program, and implement the compliance verification program. Even if ANSI/ESD S20.20 certification is not the goal, it is very beneficial to have a documented and monitored ESD/ESA control plan for a FEOL semiconductor

fab with some level of training and compliance verification to avoid yield loss and reliability exposure, as well as to be able to demonstrate to customers that ESD/ESA controls are being addressed. The ownership of the plan should be at a sufficient level of management to oversee all the functional areas involved (process, maintenance, quality, test) to ensure all aspects of the plan are accounted for.

6.0 CONCLUSION AND RECOMMENDATIONS

Throughout this document, it has been shown that the ESD/ESA considerations in semiconductor wafer fab and mask house facilities differ from the typical considerations for the facilities that ANSI/ESD S20.20 was made for. Recommendations for the future are:

- Organize a small team of wafer fab experts to outline all the special ESD/ESA considerations required in the semi-fab environment.
- Determine how these differences can be put into a standard requirements format.
- Suggest to EOS/ESD Association, Inc. how these differences should be codified in a new standard or supplemental document to ANSI/ESD S20.20.
- Investigate whether a new standards working group should be started within the ESDA.

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