EOS/ESD Symposium Outstanding Paper (Best Presentation) Awards

The EOS/ESD Symposium Outstanding Paper Award is presented to a person or persons to encourage a high degree of effort toward technical excellence in the writing and presentation of their paper. The award is voted on by EOS/ESD Symposium attendees based on originality, relevance to practice or further research, critical analysis of concepts, theories, and findings, and clarity of presentation. Awards are given in the manufacturing and device categories.

1983 "The Room Air Ionization System, a Better Alternative than 40% Relative Humidity"
C. F. Mykkanen and D.R. Blinde

1984 "The Effectiveness of Antistatic Bags in Screening Semiconductor Components Against ESD Transients"
TIE **G.C. Holmes**

1984 "A Realistic and Systematic ESD Control Plan"
G.T. Dangelmayer

1985 "A Technique for Real-Time Examination of Sub-Surface EOS/ESD Damage in Integrated Circuits"
C.T. Amos and C.E. Stephens

1986 "Thick Oxide Device ESD Performance Under Process Variations"
R.A. Mc Phee, C. Duvvury, R.N. Rountree, H. Domingos

1987 "ESD Protection Structures to Survive the Charged Device Model (CDM)"
L.R. Avery

TIE
1988 "A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes"
Robert Rountree, Charvaka Duvvury, Tatsuro Maki, Harvey Stiegler

1988 "Triboelectricity and Surface Resistivity Do Not Correlate"
Steven L. Fowler

1989 "Understanding Pink Poly"
Marvin R. Havens

1990 "Electrostatic Discharge Protection for a 4-Mbit DRAM"
Mark D. Jaffe

1991 "Implementation of Computer-Based ESD Training: A Case Study Comparing the Computer Approach With

Traditional Classroom Techniques"
Joanne Woodward-Jack

1992 "ESD Protection In a 3.3V Sub-Micron Silicided CMOS Technology"
David Krakauer and Kaizod Mistry

1993 "The Identification and Analysis of Latent ESD Damage on CMOS Input Gates"
Jim Colvin

1994 "The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design"
Ajith Amerasekera and Charvaka Duvvury

1995 "Advanced CMOS protection Device Trigger Mechanisms During CDM"
Charvaka Duvvury and Ajith Amerasekera

1996 "Recommendations to Further Improvements of HBM ESD Component Specifications"
Koen Verhaege, Christian Russ, G. Groeseneken, Donna Robinson-Hahn, Don Lin, Marty Farris, Jeff Scanlon, J.Veltri

1997 "ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced SemiConductor Technology"
Steven Voldman

1998 "Magneto Optical Static Event Detector"
N. Jacksen, Wayne Tan, Don Boehm

1999 "An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events"
Jeremy Smith

2000 "Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices"
Koen Verhaege, Christian Russ

2001 "Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling"
Markus P. J. Mergens, Koen G. Verhaege, Christian C. Russ, John Armer, Phillip C. Jozwiak, Girija Kolluri, Leslie R. Avery

2002 "Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 μm ESD Protection Circuits"
G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.

2003 " Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies"
M. Stockinger, J.W. Miller, M.G. Khazhinsky, C.A. Torres, J.C. Weldon, B.D. Preble, M.J. Bayer, M. Akers, Motorola; V.G. Kamat, Synopsis, Inc.

2004 "Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies"
M.G. Khazhinsky, J.W. Miller, M. Stockinger, J.C. Weldon Freescale Semiconductor, Inc.

2005 Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window
G. Boselli, J. Rodriquez, C. Duvvury, J. Smith, Texas Instruments, Inc.

2006 HBM Stress of No-Connect IC Pins and Subsequent Arc-Over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed Neighbor Pins
H. Kunz, C. Duvvury, J. Brodsky, P. Chakraborty, A. Jahanzeb, S. Marum, L. Ting, J. Schichl, Texas Instruments, Inc.

2007 CDM Peak Current Variations and Impact Upon CDM Performance Thresholds
Agha Jahanzeb, Yen-Yi Lin, Steve Marum, Joe Schichl, Charvaka Duvvury

2008 HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike
Melanie Etherton, James Miller, Freescale Semiconductor, Inc.; Victor Axelrod, Haim Marom, Freescale Semiconductor Isreal; Tom Meuse, Thermo Fisher Scientific

2009 A DRC-based Check Tool for ESD Layout Verification
T. Smedes, N. Trivedi, J. Fleurimont, A.J. Huitsing, P.C. de Jong, W. Scheucher, J. van Zwol, NXP Semiconductors

2010 The Relevance of Long-Duration TLP Stress on System Level ESD Design
Gianluca Boselli, Akram Salman, Jonathan Brodsky, and Hans Kunz, Texas Instruments, Inc.

2011 Voltage Monitor Circuit for ESD Diagnosis
Nathan Jack, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

2012 Chasing a Latent CDM ESD Failure by Unconventional FA Methodology
Harshit Dhakad, Harald Gossner, Bernhard Stein, Christian Russ, Intel Mobile Communications; Stefan Zekert, Infineon Technologies

2013 An Active MOSFET Rail Clamp Network for Component and System Level Protection
Michael Stockinger, Wenzhong Zhang, Kristen Mason, James Feddeler, Freescale Semiconductor, Inc.

2014 Do Devices on PCBs Really See a Higher CDM-like ESD Risk?
Reinhold Gärtner, Infineon Technologies; Wolfgang Stadler, Josef Niemesheim, Oliver Hilbricht, Intel Mobile Communications

2015 Low Impedance Contact CDM
Nathan Jack, Timothy J. Maloney,Intel Corporation

2016 EDA Approaches in Identifying Latch-up Risks
Michael Khazhinsky, Silicon Labs; Kzysztof Domanski, Harald Gossner, Intel Deutschland GmbH; Guido Quax, Scott Ruth, NXP Semiconductors; Farzan Farbiz, Texas Instruments; Nitesh Trivedi, Infineon

2016 Predict the Product Specific CDM Stress Using Measurement-Based Models of CDM Discharge Heads
Friedrich zur Nieden, Kai Esmark, Stefan Seidl, Reinhold GärtnerInfineon Technologies AG

2017 An ESD Case Study with High-Speed Interface in Electronics Manufacturing and its Future Challenge
Rita Fung, Richard Wong, James Tsan, Jatin Batra, Cisco Systems, Inc.

2017 FinFET SCR: Design Challenges and Novel Fin SCR Approaches for On-Chip ESD Protection
Milova Paul, B. Sampath Kumar, Mayank Shrivastava, Indian Institute of Science; Christian Russ, Harald Gossner, Intel Deutschland GmbH

2018 Study of the Discharge Current Created by an Ionizer
Stefan Seidl, Friedrich zur Nieden, Reinhold Gaertner, Infineon Technologies AG

2018 Undesired Effects of CDM Stressing Non-Connected Pins
Theo Smedes, Bob Knoppers, Richard Derikx, NXP Semiconductors; Artemio Garcia, Greg O'Sullivan, Micron Technology

2019 Towards Standardization of Low Impedance Contact CDM (Device)
Nathan Jack, Brett Carn, Josh Morris, Intel Corporation

2019 Are ESD Chairs Good Enough to be Used as Primary Means of Personnel Grounding? (Mfg)
Reinhold Gartner, Magdalena Hilkersberger, Infineon Technologies AG; Jurgen Speicher, Wolfgang Warmbier GmbH & Co. KG

2020 Cable Discharge Event Simulation and Measurement Methods (Device)
Pasi Tamminen, EDR&Medeso

2020 A Thin Film Storage Device to Characterize the CDM Event Distribution of a Process (Mfg)
Matt Lauderdale, Emmanuel Onyegam, Brad Smith, Jane Yater, NXP Semiconductors; Scott Ruth, AMD

2021 Enablement, Evaluation and Extension of a CDM ESD Verification Tool for IC Level Methods (Device)
Christian Russ, Kai Esmark, Patrick Huff, Jens Schneider, Gernot Langguth, Infineon Technologies AG; Lena Zeitlhöfler, Technical University of Munich; Meruzhan Cadjan, Yuri Feinberg, Silicon Frontline Technology, Inc.

2021 (Tie) ESD Characterization of Non-Powered Hand Tools (Mfg)
Magdalena Hilkersberger, Reinhold Gärtner, Infineon Technologies AG; Wolfgang Stadler, Intel Deutschland GmbH

2021 (Tie) Practical Aspects of Managing EMI-Caused EOS in IC Handlers and Similar Equipment (Mfg)
Jose Juan Montalban, Gilberto Raul Flores, Gabriela Enriques, Skyworks; Humberto Hernandez; Vladimir Kraz, OnFILTER

2022 The HBM Tester Parasitics Problem (Device)
Theo Smedes, Marcin Grad, Sheela Verwoerd, Jian Gao, NXP Semiconductors; Greg O'Sullivan, James Davis, Micron Technology, Inc.

2022 Detection of Electrostatic Discharge with Limited Measurement Bandwidth (Mnfg)
Toni Viheriäkoski, Cascade Metrology Oy; Pasi Tamminen, Danfoss

2023 Voltage to Current Correlation for CDM Testing (Device)
Lena Zeitlhoefler, Theresa Lutz, Friedrich zur Nieden, Kai Esmark, Reinhold Gaertner, Infineon Technologies AG

2023 Die-to-Die ESD Discharge Current Analysis (Mnfg)
Pasi Tamminen, Danfoss; Toni Viheriäkoski, Cascade Metrology

EOS/ESD Symposium Best Paper Awards

The EOS/ESD Symposium Best Paper and Best Student Paper Awards are presented to a person or persons to encourage a high degree of effort toward technical excellence in the writing and presentation of their paper. Each subcommittee nominates a paper and student paper they believe has outstanding value in originality, relevance to practice or further research, critical analysis of concepts, theories, and findings, and clarity of presentation. Student papers are eligible for both nominations. Nominated papers are reviewed and voted on by a selected committee (TPC awards committee) led by the TPC chair and comprised of subcommittee chairs, vice general chair, and general chair.

1979
O. McAteer
An Effective ESD Awareness Program

1980 Tie
J. Keller
Protection of MOS Integrated Circuits From Destruction By Electrostatic Discharge

S. Halperin
Facility Evaluation Isolating Environmental ESD Problems

1981
B. Unger, R. Chemelli
P. Bossart, M. Hudock
Evaluation of Integrated Circuit Shipping Tubes

1982
O. McAteer, R. Twist, R. Walker
Latent ESD Failures

1983
R. Enoch, R. Shaw, R. Taylor
ESD Sensitivity of NMOS LSI Circuits and Their Failure Characteristics

1984
L. DeChiaro
Device Susceptibility Testing and Design Hardening

1985
D. Pierce
Electro-Thermomigration as an Electrical Overstress Failure Mechanism

1986 Tie

A. Rubalcava, D. Stunkard, W. Roesch
Electrostatic Discharge Effects on
Gallium Arsenide Integrated Circuits

T. Maloney
Contact Injection: A Major Cause
of ESD Failure in Integrated Circuits

1987 Tie

E. Lai, J. Plaster
ESD Control in the Automotive
Electronics Industry A Case Study

Y. Fong, C. Hu
The Effects of High Field Transients
on thin Gate Oxide MOSFETS

1988 TIE

C. Duvvury, R. Rountree
Output ESD Protection Techniques
for Advanced CMOS Process

R. Renninger, D. Lin, M. Jon, T. Diep, T. Welsher
A Microwave Bandwidth Waveform
Monitor for Charged- Device Model Simulators

1989

R. Renninger, M. Jon D. Lin, T. Diep, T. Welsher
A Field-Induced Charged Device Model Simulator

1990

T. Maloney
Enhanced P+ Substrate Tap Conductance in the Presence of NPN Snapback

1991

R. Renninger
Mechanisms Of Charged- Device Electrostatic Discharges

1992

K. Bock, H. Hartnagel Circuits for High-Frequency Devices Fieldemitter-Based ESD-Protection and IC's

1993

K. Verhaege, P. Roussel, G. Groeseneken, H. Maes, H. Gieser, C. Russ, P. Egger, X. Guggenmos, F. Kuper
Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model

1994 TIE

A. Amerasekera, C. Duvvury
The Impact of Technology Scaling on
ESD Robustness and Protection
Circuit Design

M. Chaine, C. Liong, H. San
A Correlation Study Between Different
Types of CDM Testers and "REAL"
Manufacturing In-Line leakage Failures

1995

A. Wallash, T. Hughbanks, S. Voldman
ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads

1996

H. Gieser, M. Haunschild
Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model Submicron CMOS Processes

1997

J. Chen, A. Amerasekera, C. Duvvury
Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS processes
Presented in 98, photo in 1999 Proceedings

1998

V. Gupta, A. Amerasekera, S. Ramaswamy, A. Tsao
ESD-related Process Effects in Mixed-Voltage Sub- 0.5 μm Technologies
Presented in 99, photo in 2000 Proceedings

1999
J. Smith
An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events
Presented in 00, photo in 2001 Proceedings

2000
J. Miller, M. Khazinsky, J. Weldon
Engineering the Cascoded NMOS Output Buffer for Maximum V t1
Presented in 01, photo in 2002 Proceedings

2001
C. Torres, J. W. Miller, M. Stockinger, M. D. Akers, M. G. Khazhinsky, J. C. Weldon
Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies
Presented in 02, photo in 2003 Proceedings

2002
G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.
Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 μm ESD Protection Circuits
Presented in 03, photo in 2004 Proceedings

2003
M. Stockinger, J. W. Miller, M. G. Khazhinsky, C. A. Torres, J. C. Weldon, B. D. Preble, M. J. Bayer, M. Akers, Motorola; V. G. Kamat, Synopsis, Inc.
Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
Presented in 04, photo in 2005 Proceedings

2004
M. G. Khazhinsky, J. W. Miller , M. Stockinger, J. C. Weldon; Freescale Semiconductor, Inc.
Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies
Presented in 05, photo in 2006 Proceedings

2005
ESD Evaluation of the Emerging MuGFET Technology
C. Russ, H. Gossner, T. Schulz, N. Chaudhary, K. Schruefer , Infineon Technologies;
W. Xiong, A. Marshall, C. Duvvury, C. R. Cleavelin, Texas Instruments
Presented in 06, photo in 2007 Proceedings

2006
Ultra-thin Gate Oxide Reliability in the ESD Time Domain
A. Ille, Infineon Technologies and Université de Provence-ISEN; W. Stadler, A. Kerber, T. Pompl, T. Brodbeck, K. Esmark, Infineon Technologies; A. Bravaix, Université de Provence-ISEN
Presented in 07, photo in 2008 Proceedings

2007
Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections During Fast TRansients
T. Smedes, N. Guitard, NXP Semiconductors
Presented in 08, photo in 2009 Proceedings

2008
A study of Term Pulses and Cabled MR Sensors
Icko Eric Timothy Iben, IBM
Presented in 09, photo in 2010 Proceedings

2009
Characterization and Simulation of Real-World Cable Discharge Events
Wolfgang Stadler, Tilo Brodbeck, Josef Niemesheim, Reinhold Gaertner, Infineon Technologies; Kathleen Muhonen, Penn State College, The Behrend College
Presented in 10, photo in 2011 Proceedings

2010
On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD
Yiqun Cao, Ulrich Glaser, Joost Willemen, Stephan Frei, and Matthias Stecher, Infineon Technologies, and Technische Universität Dortmund
Presented in 11, photo in 2012 Proceedings

2011
ESD Simulation with Wunsch-Bell based Behavior Modeling Methodology
Yiqun Cao, Infineon Technologies and Technische Universität Dortmund; Ulrich Glaser, Joost Willemen, Filippo Magrini, Michael Mayerhofer, Matthias Stecher,
Infineon Technologies; Stephan Frei,Technische Universität Dortmund
Presented in 12, photo in 2013 Proceedings

2012
ESD Characterization of Atomically-Thin Graphene
Hong Li, Wei Liu, Kaustav Banerjee, University of California; Christian C. Russ, David Johnsson, Harald Gossner, Intel Mobile Communications
Presented in 13, photo in 2014 Proceedings

2013
An Active MOSFET Rail Clamp Network for Component and System Level Protection
Michael Stockinger, Wenzhong Zhang, Kristen Mason, James Feddeler, Freescale Semiconductor, Inc.
Presented in 14, photo in 2015 Proceedings

2014
Theory of Active Clamp Response to Power-On ESD and Implications for Power Supply Integrity
Robert Mertens, Nicholas Thomson, Yang Xiu, Elyse Rosenbaum, University of Illinois at Urbana-Champaign
Presented in 15, photo in 2016 Proceedings

2015
An Off-chip ESD Protection for High-speed Interfaces
Guido Notermans, Hans-Martin Ritter, Joachim Utzig, Steffen Holland, Zhihao Pan, Jochen Wynants, Paul Huiskamp, Wim Peters, Burkhard Laue, NXP Semiconductors
Presented in 16, photo in 2017 Proceedings

2016
Gun Tests of a USB3 Host Controller Board
Guido Notermans, Hans-Martin Ritter, Burkhard Laue, Stefan Seider,NXP Semiconductors
Presented in 17, photo in 2018 proceedings

2017
Risk Assessment of Cable Discharge Events
Wolfgang Stadler, Josef Niemesheim, Andreas Stadler, Sebastian Koch, Harald Gossner, Intel Deutschland GmbH
Presented in 18, Photo in 2019 Proceedings

2018
Device Failure from the Initial Current Step of a CDM Discharge
David Johnsson, Krzysztof Domanski, Harald Gossner; Intel Deutschland GmbH
Presented in 19, Photo in 2020 Proceedings

2019
Towards Standardization of Low Impedance Contact CDM
Nathan Jack, Brett Carn, Josh Morris, Intel Corporation
Presented in 19, Photo in 2022 Proceedings

2020
Increased Latch-Up Susceptibility of ICs Using Reverse Body Bias (Tie)
Sandeep Vora, Elyse Rosenbaum, University of Illinois at Urbana Champaign; Michael Stockinger, NXP Semiconductors
Presented in 21, Photo in 2022 Proceedings

Damage to Electrostatic Discharge Sensitive Electronic Devices by Charging Electrostatic Fields (Tie)
Jeremy Smallwood, Electrostatic Solutions Ltd
Presented in 21, Photo in 2022 Proceedings

2021
Automotive High-Speed Interfaces: Future Challenges for System-level HV-ESD Protection And First-Time-Right Design
Sergej Bub, Markus Mergens, Andreas Hardock, Steffen Holland, Ayk Hilbrink, Nexperia Germany GmbH
Presented in 22, Photo in 2023 Proceedings

2022
Advanced CDM Simulation Methodology for High-Speed Interface Design
Umair Ishfaq, Krzysztof Domanski, Susanne Heber, Harald Gossner, Intel Deutschland GmbH
Presented in 2023, photo in 2024 proceedings

2023
Die-to-Die ESD Discharge Current Analysis (Mnfg)
Pasi Tamminen, Danfoss; Toni Viheriäkoski, Cascade Metrology
Presented in 2024, photo in 2025 proceedings

International EOS/ESD Symposium on Design & System Best Paper Awards

2021
Investigation on Fabrication-induced High-leakage Issue of an Overdrive ESD Power Clamp in Advanced FinFET Technology
Guangyi Lu, Lihui Wang, Ling Wang, Xin Gao and Mei Li, Hisilicon Technologies Co. LTD.

EOS/ESD Symposium Best Student Paper Awards

The EOS/ESD Symposium Best Paper and Best Student Paper Awards are presented to a person or persons to encourage a high degree of effort toward technical excellence in the writing and presentation of their paper. Each subcommittee nominates a paper and student paper they believe has outstanding value in originality,

relevance to practice or further research, critical analysis of concepts, theories, and findings, and clarity of presentation. Student papers are eligible for both nominations. Nominated papers are reviewed and voted on by a selected committee (TPC awards committee) led by the TPC chair and comprised of subcommittee chairs, vice general chair, and general chair.

2000	"Chip-Level Simulation for CDM failures in Multi-Power ICs" **Jaesik Lee, University of Illinois**
2001	"Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test" **P. Galy, Pole Universitaire Leonard de Vinci**
2002	"ESD Characterization of Grounded-Gate NMOS with 0.35 μm/18 V Technology Employing Tranmission Line Pulser (TLP) Test" B-C Jeon, S-C Lee, J-K Oh, S-S Kim, M-K Han, Seoul National University; Y-I Jung, H-T So, J-S Shim, K-H Kim, Hynix Semiconductor Inc.
2003	"Comprehensive ESD Protection for RF inputs" S. Hyvonen, S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign
2004	"Study of CDM Specific Effects for a Smart Power Input Protection Structure" M. Etherton, N. Qu, J. Willemen, W. Wilkening, S. Mettler, M. Dissegna, R. Stella, L. Zullino, A. Andreini, h. Gieser, H. Wolf, W. Fichtner Swiss Federal Institute of Technology
2005	"SCR Operation Mode of Diode Strings for ESD Protection" U. Glaser, M. Ciappa, W. Fichtner, ETH Zurich; K. Esmark, C. Russ, M. Streibl, Infineon Technologies; K. Domanski, Infineon Technologies and Nicolaus Copernicus University
2006	"Transmission Line Pulse (TLP) Testing of Radio Frequency (RF) Micro-machined Micro-Electro-Mechanical-Systems (MEMS) Switches" A. Tazzoli, V. Peretti, E. Zanoni, G. Meneghesso, University of Padova
2007	**"**Reliability Aspects of Gate Oxide under ESD Pulse Stress" Adrien Ille, Université de Provence and Infineon Technologies, Wolfgang Stadler, Thomas Pompl, Harald Gossner, Tilo Brodbeck, Kai Esmark , Philipp Riess, David Alvarez,Infineon Technologies; Kiran Chatty, Robert Gauthier, IBM; Alain Bravaix, Université de Provence
2008	**"**Design Methodology of FinFETDevices that Meet IC-Level HBM Target" S. Thijs, G. Groeseneken, IMEC vzw and Katholieke Universiteit Leuven; C. Russ, H. Gossner, Infineon Technologies AG; D. Trémouilles, LAAS/CNRS; A. Griffoni, University of Padova; D. Linten, M. Scholz, N. Collaert, R. Rooyackers, M. Jurczak, IMEC vzw; M. Sawada, T. Nakaei, T. Hasebe, Hanwa Electronics Ind. Co. Ltd; C. Duvvury, Texas Instruments Inc.
2009	**"**ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology" James Di Sarro, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Yang Yang, Dimitris Ioannou, George Mason University; Kiran Chatty, Robert Gauthier, Souvick Mitra, Junjun Li, IBM; Christian Russ, Infineon Technologies

2010 "Investigation of Current Flow During Wafer-Level CDM Using Real-Time Probing"
Nathan Jack and Vrashank Shukla, Advisor – Prof. Elyse Rosenbaum, University of Illinois at Urbana-Champaign

2011 "ESD Simulation with Wunsch-Bell based Behavior Modeling Methodology"
Yiqun Cao, Infineon Technologies and Technische Universität Dortmund

Advisor: Stephan Frei,Technische Universität Dortmund, Co-authors: Ulrich Glaser, Joost Willemen, Filippo Magrini, Michael Mayerhofer, Matthias Stecher, Infineon Technologies

2012 "ESD Characterization of Atomically-Thin Graphene"
Hong Li, Kaustav Banerjee, Wei Liu, University of California; Christian C. Russ, David Johnsson, Harald Gossner, Intel Mobile Communications

2013 "Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Micro-Electronic Components"
Vrashank Shukla, University of Illinois at Urbana-Champaign Advisor: Elyse Rosenbaum, University of Illinois at Urbana-Champaign Co-Authors: Gianluca Boselli, Mariano Dissegna, Charvaka Duvvury, Raj Sankaralingam, Texas Instruments, Inc.

2014 "Do Devices on PCBs Really See a Higher CDM-like ESD Risk?"
Robert Mertens, University of Illinois at Urbana-Champaign Advisor: Elyse Rosenbaum University of Illinois at Urbana-Champaign Co-authors: Nicholas Thomson, Yang Xiu University of Illinois at Urbana-Champaign

2015 "CDM-Reliable T-coil Techniques for High-Speed Wireline Receivers"
Min-Sun Keel, University of Illinois at Urbana-Champaign; Advisor: Elyse Rosenbaum University of Illinois at Urbana-Champaign

2016 "An Automated Tool for Chip-Scale ESD Network Exploration and Verification"
Benjamin Viale, STMicroelectronics, CNRS-UMR Advisor: Bruno Allard CNRS-UMR

2017 "On-Chip Sensors to Measure Level of Transient Events"
A. Patnaik, M. Suchak, R. Seva, K. Pamidimukkala, D. Beetner, Missouri University of Science and Technology; G. Edgington, R. Moseley, J. Feddeler, M. Stockinger, NXP Semiconductors

2018 "Hardware and Software Combined Detection of System-Level ESD-Induced Soft Failures"
Sandeep Vora, Rui Jiang, Prajwal Mysore-Vijayaraj, Keven Feng, Yang Xiu, Shobha Vasudevan, Elyse Rosenbaum, University of Illinois Urbana-Champagne

2019 "Mechanism of Sequential Finger Triggering of Multi-Finger Floating-Base SCRs Due to Inherent Substrate Currents"
Hasan Karaca, TU Wien, Clement Fleury, Dionyz Pogany, Steffen Holland, Hans-Martin Ritter, Guido Notermans, Nexperia Germany GmbH

2020 "Increased Latch-up Susceptibility of ICs Using Reverse Body Bias"
Sandeep Vora, Elyse Rosenbaum, University of Illinois at Urbana Champaign; Michael Stockinger, NXP Semiconductors

2021 "1 Ω Disk Resistor Full Wave Modeling for JS-002 Standard"
Daryl Beetner, Missouri University of Science and Technology; David Pommerenke, Graz University of Technology, Silicon Austria Labs; Hossein Rezaei, Matthew Drallmeier, Jared R. Floyd, Wei Huang, ESDEMC Technology LLC

2022 Analysis of Input Receiver Transistors Behavior During a CDM Event
Chloé Troussier, STMicroelectronics SA, University Grenoble Alpes
Advisors: Emmanuel Simeu, Jean-Daniel Arnould, University Grenoble Alpes, CNRS
Co-authors: Johan Bourgeat, Blaise Jacquier, STMicroelectronics SA

2023 Distributed Protection for High-Speed Wireline Receivers
Matthew Drallmeier, University of Illinois Urbana-Champaign
Advisor: Elyse Rosenbaum, University of Illinois Urbana-Champaign

International EOS/ESD Symposium on Design & System Best Student Paper Awards

2021 "Study of ESD Device Modeling Based on Neural Network"
Yize Wang, Yunhao Li, Yuan Wang, Institute of Microelectronics, Peking University