International Electrostatic Discharge Workshop (IEW)

12 – 16 May 2025

Hotel Dubrovnik, Gajeva ulica 1, Zagreb, Croatia

Setting the Global Standards for Static Control

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Group photo from 2023 IEW in Tutzing, Germany

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The IEW Experience

Dear Colleagues and ESD Enthusiasts,

Welcome to the 18th annual International ESD Workshop (IEW)! This year, we are thrilled to invite you to join us at the Hotel Dubrovnik in the vibrant city of Zagreb, Croatia, from 12 to 16 May 2025. This event promises to be an exciting opportunity to delve into the latest advancements and challenges in the field of Electrostatic Discharge (ESD) and Electrical Overstress (EOS).

The IEW continues to be a cornerstone for innovation and collaboration within our community. Our focus ESD focus topics this year will be on IC design, chip-level and system-level ESD, EDA, automotive applications, failure analysis, EMC, testing, and advanced technologies. We are particularly excited about our keynote and invited speakers who will bring light to new developments in the ESD field.

Our program is designed to stimulate discussions and provide a platform for presenting both completed research and open research questions. The program will include discussion groups, invited talks, technical presentation sessions and special interest groups. Each technical session will begin with a five-minute teaser presentation, followed by an engaging poster-based discussion, ensuring opportunities for interaction and idea exchange in a relaxed environment.

Join us in exploring the future of ESD and EOS, as we bring together experts from both industry and academia to share their insights and experiences. The IEW is closely aligned with the EOS/ESD Symposium, enhancing our collaborative efforts and broadening the scope of our discussions.

We look forward to your participation and to the vibrant discussions that will undoubtedly emerge from this year's workshop. Let's shape the future of ESD together!

Marko Simicic
imec
Management Committee Chair
on behalf of the IEW management committee

Keynote: ESD – Expectations, Surprises and Discoveries

Karim T. Kaschani, Robert Bosch GmbH

While electrostatic charging and electrostatic discharges (ESD) are among the oldest physical phenomena on earth, they drew attention to the design of integrated circuits due to unexpected device failures just about 45 years ago. We have learned a lot about ESD control and ESD protection since then. However, we are still often surprised to see that our expectations turn out to be wrong and that there is so much more to learn. This keynote reviews some of these expectations and surprises taken from the different branches of the extremely diverse fields of ESD and EOS.

Karim T. Kaschani received his Ph.D. for his research in the field of semiconductor power devices in electrical engineering from the Technical University in Brunswick in 1996. He worked for almost eight years for Siemens Semiconductors and Infineon Technologies as a development engineer and project leader in advanced ICs for switch-mode power supplies. He also worked on concept engineering of high-voltage SOI technologies and developing high-voltage ICs. Afterward, he joined Atmel Automotive and worked for almost 7 years as head of the ESD test and consulting group and as product quality engineering manager. Thereafter, he joined Texas Instruments and worked for more than 9 years as a senior ESD engineer responsible for regional ESD and EOS support in Europe. He then worked for 2.5 years as leader of the ESD team for Elmos Semiconductors S.E. and is currently working as senior ESD engineer for Robert Bosch GmbH in Germany. He is a member of the steering council and also a member of the managing board of the ESD FORUM e.V. He holds several patents and is the author or co-author of several papers, conference presentations, and tutorials in the fields of semiconductor power devices, ICs, semiconductor technologies, ESD and EOS.

Invited Talk: Make Your EMC & ESD Solutions Compatible!

Patrice Besse, EMC & ESD Manager – Fellow, NXP Semiconductors

Electronic modules should not create disturbance and should be immune against transient aggressions and electromagnetic interference (EMI), keeping functions safe during ESD or EMI. Systems and integrated circuits should pass multiple EMC and ESD standards specific to the application domains and over the globe. At each development step, from the technology to the validation, the ESD strategy and the EMC design must be fully compatible to provide a common solution. In this talk, Patrice presents the basics of EMC requirements and how EMC and ESD solutions can interact.

Patrice Besse was born in France and obtained post-graduation in compatibility electromagnetic (EMC) in 2000. In 2004, Patrice defended a PhD on ESD for HV analog in collaboration with Motorola and LAAS-CNRS, Toulouse, France. Then, Patrice joined the Analog Design Group of Freescale Toulouse (France) as an ESD engineer. In the last 20 years, Patrice has led ESD & EMC developments for different businesses with a main focus on automotive applications. Patrice is the author of more than 40 publications and a book chapter and has 42 patents granted in the fields of EMC, ESD, and analog design. Since 2014, Patrice has managed EMC & ESD activities within NXP semiconductors, including technology development, ESD/EMC libraries and models, design for EMC and ESD, lab validation with pre-certification, and customer support.

Seminar: ESD Design Support in Practice: A Few Real-Life Examples

Gijs De Raad – Notable Inventor, NXP Semiconductors

Providing ESD design support is something you can only learn in practice. There is no school for it. Also, exactly what the design support looks like is quite variable: it depends on the type of IC being made, the ESD building blocks and verification tools available, and things like project timeline and even design habits or culture of the design group you work with. This talk gives a few real-life examples of what ESD design support can look like, emphasizing how often very simple simulations can have a big impact.

Gijs de Raad was born in Ede, the Netherlands, on October 26, 1969. He received his MSc in applied physics in 1995 at the University of Groningen, the Netherlands. He received a PhD in physics in 2001 at the Technical University of Eindhoven, the Netherlands, on the thesis "Voltage-dependent Scanning Tunneling Microscopy on the {110}-surfaces of GaAs, AlGaAs, and their heterostructures". Since 2000, he has worked at Philips Semiconductors, which later became NXP Semiconductors. He has been active as an ESD engineer since 2005, with a particular interest in the physics of ESD devices. Today, Gijs specializes in ESD solutions for high-voltage and power ICs in mature technologies. These ICs typically have significant analog content and, in many cases, require a custom ESD solution. Gijs started ESD work at the age of 35 literally from scratch, and so embodies the phrase "You're never too old to learn". For students, he likes to add, "You're never too young to teach".

Invited Talk: Challenges in ESD Discharge Risk Reduction to Support Advanced Packaging Manufacturing Roadmap

Dr. Philippe Muller, Suss MicroTec

There can be several ESD risks during packaging and die-to-die bonding. This talk covers the typical process flows during temporary bonding and laser debonding of thinned wafers. It also discusses dicing and Cu-Hybrid bonding with the two main approaches, ' wafer to wafer' and 'die to wafer'. The talk focuses on the associated hardware aspects to depict possible areas where charging might occur. Further, some of the preliminary measures taken to reduce the risks of ESD are presented.

Philippe Muller graduated with his PhD in 2004 at the University of Science and Technology of Lille, France (USTL), in collaboration with Thales Research and Technologies, Palaiseau, France. He developed a high-power RF MEMS using Gold-gold wafer level packaging based on Karl Suss's early MA/BA/SB6 wafer bond-aligner. Philippe joined then IMEC, Belgium, as a 3D packaging research engineer working on RF MEMS packages, above-IC MEMS, and RF-IPD integration. In 2009, he joined Lynred Palaiseau, France, where he started as a Flip-chip expert within the hybrid packaging excellence center. Philippe developed down to 10 um pitch Indium bump assemblies for cooled IR sensors manufacturing. In 2015, he became the technical product manager of the InSb MWIR focal plane arrays product line, leading the engineering support team and ensuring the technical qualifications of the products in interface with the customers. In 2019, Philippe joined Huawei Belgium Research Center, Leuven, as the Lead 3D Integration Research & Development engineer. He collaborated closely with IMEC teams to develop nanoTSV, BSPDN, hybrid bonding, and FoWLP technologies. He evaluated thermal aspects and architecture optimizations for high performance and Sparking Neuronal Networks neuromorphic computing applications. In 2023, Philippe joined Suss MicroTec in Germany as a technology scout in the System Architecture and Innovation team. His role is now to help introduce rising advanced packaging technologies in the Suss MicroTec portfolio and support product roadmap definitions and developments in the permanent, temporary bonders, inkjet printing, and imprint/lithography/metrology product lines of Suss MicroTec.

Seminar: ESD Risks During PCB Assembly Processes

Istvan Kovalik, Harman

PCB assembly processes from SMT lines to final assembly and test stations have many different production equipment and process steps. In some places, it is clearly visible if there is an ESD risk in the process, but problems can also arise where we would not even suspect it at first glance. During this talk, we walk along the PCB assembly processes and examine some examples of identified risks in the production lines. Some risk assessment conceptions and questions are also represented.

Istvan Kovalik began his work in the field of ESD control in 2003. He has fallen in love with this topic and started to go deeper into it. He's been working as an ESD coordinator at Harman for 10 years and is responsible for all aspects of ESD control in three facilities in his country. He performs volunteer work for ESDA and received his ESD Program Manager Certification in 2023. Istvan recently started standardization work in the IEC TC 101 committee's WG5 group.

Seminar: Optimization of ESD and Signal Integrity on System Level for Automotive Applications

Andreas Hardock, Sergej Bub, Nexperia

This talk briefly introduces the basics of electrostatic discharge. It uses modern simulation methods to demonstrate practical tools and methods for improving the ESD and SI performance of typical consumer and automotive applications.
In the first part, classical methods of signal integrity such as S-parameter, time domain reflectometry, and eye diagrams are introduced, and their application to various ESD protection components is presented. It discusses how modern ESD protection elements behave in the time and frequency domain and how they can be analyzed with the help of simulations. In the second part, the methodology of System Efficient ESD Design (SEED) simulations of transient ESD events is applied to automotive applications such as 1000BASE-T1 Ethernet using the concept of fully dynamic behavioral SEED models. In this context, the impact of system components such as CMCs and the positioning of ESD protection components is analyzed.

Andreas Hardock studied nanostructure technology at the Julius Maximilian University of Würzburg and did his PhD in functional vias at the Technical University of Hamburg-Harburg. He started his career in 2015 in the automotive sector as an EMC engineer at Behr-Hella Thermocontrol. From 2016 to 2020, he was at Continental Automotive GmbH in Babenhausen, where he was responsible for SI/PI, and EMC and ESD topics in the role of hardware architect in product development. In 2020, he joined Nexperia as an application marketing manager, focusing on ESD and EMC topics and products for the automotive market. Andreas has been a member of the IEEE EMC Society since 2011. Since 2019, he has been an active member of the German EMC Chapter, where, from 2019 to 2020, he was responsible for organizing professional talks. Since 2020, Andreas has been the treasurer of the executive team.

Sergej Bub is a principal system level ESD expert at Nexperia Germany GmbH in Hamburg. He graduated with an M.Sc. in electrical engineering at the Technical University of Hamburg, specializing in nanoelectronics and microsystems technology. He is working at Nexperia in the research and development department in the ESD Protection and Filtering group. His work covers modeling and simulation for System Efficient ESD Design (SEED) of high-speed application systems and discrete ESD protection components for automotive, mobile, consumer, and computing areas, extended by development and optimization of dedicated ESD protection solutions for such applications as well as project management activities for R&D projects.

Seminar: ESD in the Automotive Industry– A Proposal for Lowering Risks During System Level ESD Qualification and Reducing Component Cost

Steffen Holland, Nexperia

Often, IC manufacturers get requests from their Tier 1/OEM customers to provide ESD robustness levels according to ISO10605. The ISO10605 test has a contact and air discharge part. Due to the wide specification of the test generators (=ESD guns) and the stochastic nature of an air discharge, the pulse form of the current pulses varies a lot. Additionally, the ISO10605 test is not specified for components, creating an even wider variability due to different setups. This results in a situation where a comparison between different parts is basically impossible, posing the risk of a failed system level ESD qualification. Customers often respond by requesting costly higher ESD robustness levels of the components.

In this talk, a proposal is made to provide a repeatable test characterization for IC components, which roughly correlates to the contact discharge of ISO10605. By providing this information with SEED models, Tier 1 and/or OEM customers can perform virtual prototyping to optimize the system level ESD robustness and lower the risk of a failed ESD qualification. Additionally, cost savings are possible because the active area in the IC needed for ESD protection could be reduced.

Steffen Holland received a Ph.D. in physics from the University of Hamburg, Hamburg, Germany, in 2004. Until 2005, he was a research member with the University of Hamburg. Afterward, he joined the process development group of Philips Semiconductors, Hamburg, Germany. He is currently with Nexperia Semiconductors, Hamburg, Germany, and working on discrete ESD protection devices as a system architect. His main research interests include device physics and modeling.

Technical presentations

A Case Study on ESD Trigger Circuit Latch-On Prevention
Marcin Grad, Paul Hendrik Cappon, Jian Gao, Sander Sluiter, Damien Fournier – NXP

AI-Driven TLP Data Analysis – A Case Study
Hossein Hosseini, Mehrdad Nourani, Theo Smedes, Charvaka Duvvury, UT Dallas

CDM & CC-TLP on Bare Dies Fabricated in Leading-Edge FIN-FET Technology Nodes
Ellen Merkel, Heinrich Wolf, Bahar Youssefi, David Burnel, Fraunhofer EMFT

CMOS-Technology: ULL RC SCR Clamps Voltage Overshoot and impact of Supply Capacitance
Nandha Kumar Subramani, Alain Loiseau, Globalfoundries

Development of a New Latch-Up Measurement System for Advanced LSIs
Teruo Suzuki, Kazuya Okubo, Hiroyuki Koike, Hideaki Miura, Masanori Sawada, Socionext, Hanwa Electronic Ind. Co., Ltd.

ESD Case Study: Pin-to-pin HBM Failure Investigation and Solution
Gaurav Singh, Jan Otten, Prantik Mahajan, Renesas

ESD Characterization in D-mode GaN RF Devices for RF ESD Protection Design in IC Consideration
Wei-Min Wu, Chin-Ya Su, Dongyang Yan, Bertrand Parvais, Nadine Collaert, IMEC

ESD HBM Robustness Response to Barrier Layer Conditions in Schottky-based GaN-on-Si HEMTs
Chin-Ya Su, Wei-Min Wu, Hao Yu, Bertrand Parvais, Partrick Reynaert, Nadine Collaert, IMEC

ESD Risk Evaluations in 2.5D/3D IC Stacking With TCAD Simulation
Shane Lin, Marko Simicic, Nicolas Pantano, Piet Wambacq, IMEC

Evaluation of ESD Diode Performance in Sub-300 nm Thin Si Substrate
Wen-Chieh Chen and Marko Simicic, IMEC

Exploring distributed ESD Protection With Low ESD Voltage Targets for Heterogeneous IC Packages
Liesl Spruyt, Marko Simicic, Dragomir Milojevic, Nicolas Pantano, IMEC

How to Develop ESD Robust Systems in an Efficient Way?
Barak Hasan Kara, Michael Ammer, Kendrik Emkel Ginting, Infineon

Impact of Diode Overshoot for ESD Protection During D2D and D2W Bonding Process
Emanuele Groppo, Harald Gossner, Umair Ishfaq, Nicolas Richaud, Intel

Investigations of Transient-Induced Latchup in DTCO/STCO Technology Options
Kateryna Serbulova, Wen-Chieh Chen, Marko Simicic, Dimitri Linten, IMEC

Method of ESD Characterization and Modeling of ESD Network for CDM Predictive Simulation
Nicolas Richaud, Umair Ishfaq, Ritesh Agarwal, Harshit Dhakad, Krzysztof Domanski, Robert Haeussler, Florian Klotz, Harald Gossner, Intel

Modular ESD Protection for Distributed Fail Safe ESD Strategy
Chloe TROUSSIER, Johan Bourgeat, Sebastien Dedieu, Frederic Bailleul, STMicroelectronics

Nanosecond ESD Robustness of Advanced Silicon Photonics Devices
Po-Yen Lin, Marko Simicic, Kristof Croes, Piet Wambacq, IMEC

Study of the Impact of Different Parameters on the CC-TLP Waveform
Vladislav Bukhanevich, Ellen Merkel, Heinrich Wolf, Fraunhofer EMFT

System-Level ESD Characterization for CAN-Transceiver Using Modular SEED Board
Kendrik Emkel Ginting, Michael Ammer and Barak Hasan Kara, Infineon

Towards Data-driven Dynamic SPICE Models for ESD Devices
Renaud GILLON, Patricia JORIS – Sydelity

Discussion Groups and Schedule to be Announced Soon!

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Registration Fee*: $1,995
Discount before March 21, 2025: members $1,795 / non-members $1,895

*The registration fee includes full workshop attendance, materials, meals Monday dinner through Friday breakfast, and lodging Monday night through Thursday night.

No lodging required? Use discount code COMMUTER2024 to receive the commuter discount.

Register online: https://cvent.me/qlYDDl

Sponsorship Opportunities Available! Contact info.eosesda@esda.org for more information.