41st EOS/ESD Symposium and Exhibits

September 15 - 20, 2019

Riverside Convention Center
3637 5th St
Riverside, CA 92501 USA

EXPLORE.

Technical Sessions
Tutorials
Manufacturing Track
Workshops

INNOVATE.

Featured Keynote
Hands-on Demonstrations
Invited Talks
Year-in-Review
IoT Workshop

NETWORK.

Industry Professionals
Social Receptions
Contests
Exhibition

IEEE EMC SOCIETY

Co-sponsored by IEEE, EMC Society, The Electron Devices Society, and Reliability Society.

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3 Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

Welcome

Dear EOS/ESD colleagues,

On behalf of EOS/ESD Association, Inc. and the 2019 Symposium Steering Committee, it is my honor to welcome you to the 41st Annual EOS/ESD Symposium and Exhibits at the Riverside Convention Center, in Riverside, California. The EOS/ESD Symposium represents the world's leading forum on Electrostatic Discharge and Overstress. The 41st Symposium awaits you with a dense program packed with tutorials, exhibits, workshops, discussion groups, technical sessions, invited talks, and hands-on sessions. We have maintained the structure of the Symposium in separate design and manufacturing tracks which we started two years ago. In addition, we will follow up on last year's success and organize our second Workshop on Robustness of IoT Devices.

Here is a brief overview of the highlights of the Symposium:

35 Tutorials: World-class experts, in all areas oo EOS and ESD, have been preparing a unique tutorial program. Tutorials are offered around the Symposium, on Sunday, Monday, and Thursday. In addition to classics on Advanced on-chip Protection, ESD Circuits, and TCAD Fundamentals, we have an increasing focus on System Level Protection, and Electrical Overstress (EOS). New tutorials include System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations. Many previously offered tutorials have been refreshed with updated material, including ESD Controls for CDM and Ultra-Sensitive Devices and Circuit Boards.

Our industry exhibits display a wide variety of ESD solutions from established products to leading-edge innovations. Representatives from over 40 different companies welcome you to introduce their products and services with the help of short presentations and live demonstrations. The exhibition starts in the exhibit hall during the welcome reception on Monday evening and continues until Wednesday afternoon. The exhibitors offer a unique opportunity for face-to-face discussions with professionals and hands-on experience on static control methods, evaluation techniques, ESD testing hardware, and many other ESD solutions. You can even bring your samples to find out whether a particular solution works for you.

Technical Program:

Following the Awards Breakfast, we are proud to present this year's Keynote on "Modeling Systems with Quantum Computing" by Dr. Rudy Wojtecki of the IBM Almaden Research Center.

In the Design Track we will have 30 Peer-reviewed + 1 Invited Technical Paper: These will be presented from Tuesday through Thursday in 12 sessions covering current research topics in the areas of advanced CMOS, RF/HV/MEMS, system-level ESD/ modeling/ soft failures, ESD transient analysis, ESD case studies, EOS/ESD EDA tools, numerical modeling, and ESD testing. The papers are presented by experts from industry and academia driving leading edge research and development.

In the Manufacturing Track we will have 13 Peer-reviewed papers in two technical sessions. Furthermore, the Manufacturing Track includes 2 Sessions with 5 short tutorials, 2 hands-on sessions, and 3 discussion groups.

This year's program again features two year-in-review presentations. Dave Swenson of Affinity Static Control & Consulting will talk about "Test, Evaluate and Support Implantation of Materials, Process and Procedures Used for ESD Control" and Alan Righter of Analog Devices will summarize the "Relationships and interactions between ESD and EMC".

Eight symposium Workshops, which take place on Tuesday and Wednesday evenings, offer an interactive forum for sharing experiences, exchanging knowledge, and exploring potential solutions. The topics cover a wide range from CDM testing to Machine Learning in ESD Check Tools. Even several ESD Myths and Misconceptions will be debunked. Each workshop allows participants the opportunity to learn different perspectives from other colleagues in the field to discuss sometimes controversial topics in an informal environment. Two of the workshops will be held in the popular world café style, which effectively lowers the threshold for every participant to actively engage in a fruitful discussion.

After last year's successful introduction of the "Robustness of IoT Devices" Workshop, we have decided to keep this workshop on the Symposium program. Several invited speakers with unique industry-wide IoT expertise will cover the numerous challenges of meeting reliability and robustness requirements. Join us to learn and network with industry experts.

I most warmly invite every one of you to the General Chair's Reception on Wednesday September 18th from 7:00 PM to 9:00 PM.

The EOS/ESD Symposium is the premier international event for professionals in industry and academia to meet their peers and learn about the latest technical findings and innovative designs. Come, learn, and have fun!

Sincerely,
Guido Notermans, Nexperia

2019 EOS/ESD Symposium General Chair

Table of Contents

Click here

Register Online! http://www.cvent.com/d/86qf9q

On-Site Registration Hours

Registration will be open at the following times:

Sunday, September 15	7:30 a.m. - 5:00 p.m.
Monday, September 16	7:30 a.m. - 5:00 p.m.
Tuesday, September 17	7:30 a.m. - 5:00 p.m.
Wednesday, September 18	7:30 a.m. - 5:00 p.m.
Thursday, September 19	7:30 a.m. - 5:00 p.m.

Save by registering in advance! This will facilitate your registration upon your arrival at the Symposium. Early registration and member discounts* are valid only if received no later than July 15, 2019.

Symposium $800

(Includes technical sessions, workshops, and exhibits)
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $600/Non-Members $700

Tutorials $710

(Sunday, Monday, OR Thursday (Full Day))
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $510/Non-Members $610

Bundled Fees $2,465

(Symposium plus Sunday, Monday, and Thursday full tutorial days)
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $1,765/Non-Members $2,165

ESD Program Development and Assessment (ANSI/ESD S20.20) $1,710

(Attendance limited to first 30 registrants)
This two-day tutorial is not included in the bundled fee.
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $1,510/Non-Members $1,610

*Membership discounts apply to those who participate as members all year long and are current at the opening of symposium registration. Memberships processed after this date will not apply. You will receive a complimentary 2020 membership with your Symposium registration which will allow you to enjoy the full benefits of membership in 2020.

Register 5 or more people from one company at the same time and save $100 per person. Please contact EOS/ESD Association, Inc. prior to registering. Refunds cannot be issued.

Student Fees

EOS/ESD Association, Inc., offers a fifty percent discount and waived fees to all Symposium tutorials for full-time students (first author only). Proof of enrollment required. Student fees apply only to symposium and tutorial registration and do not apply to bundled fees or ANSI/ESD S20.20 two day tutorial.

General Information

Symposium Proceedings

Each paid registrant receives one electronic copy of the proceedings.

Tutorial Notes

Customized, full color tutorial notes will be provided to each tutorial registrant.

General Information continued

Hospitality Suites

To maintain the objectives of the Symposium, EOS/ESD Association, Inc. encourages all exhibitors and guest organizations to schedule their hospitality and other social events at times that do not conflict with the Symposium presentations and educational activities.

Age Limits

No one under 18 years of age will be admitted to the exhibit hall.

Unauthorized Solicitation

Solicitation of business on the premises during the EOS/ESD Symposium by manufacturers or others who are not participating as exhibitors is prohibited.

Recording

Video and/or audio recording of Symposium events is prohibited without the prior written authorization of EOS/ESD Association, Inc.

Welcome Reception

A welcome reception for all attendees will be held on Monday, September 16, at 6:00 p.m. in the exhibit hall. Network with your colleagues, share your ESD work experiences with others, view the exhibits, or simply pass the time meeting new people and making new friends. The 2019 Steering Committee will greet you and answer any questions regarding the Symposium.

Annual Meetings and Awards Breakfast

The annual meeting and awards breakfast for all registered attendees and exhibitors will be held Tuesday, September 17, at 7:30 a.m. Following breakfast, General Chair, Guido Notermans, will officially open the Symposium. Vice General Chair, Lorenzo Cerati, will present the 2018 EOS/ESD Symposium paper awards. Technical Program Chair, Wolgang Stadler, will cover highlights of the 2019 technical program. Association President, Ginger Hansel, will present the Association's annual report. Awards Chair, Charvaka Duvvury, will present the 2019 Association awards.

Professional and Technical Women's Reception

The Professional and Technical Women's Reception provides a friendly environment where women in the field of ESD can network and share work experiences. This year's reception will be held on Monday, September 16, from 5:00 p.m. to 6:00 p.m.

University Students/Professors Invited to Wednesday Breakfast with ESDA Management

Wednesday, Septmber 18, 7:00 a.m-8:00 a.m

First Time Attendee Social Hour

Wednesday, September 18, 12:30 p.m.-1:30 p.m

General Chair's Reception

Guido Notermans invites attendees and exhibitors to the general chair's reception on Wednesday, September 18, from 7:00 pm to 9:00 pm. **Poster presentations of technical papers from all sessions will be on display.** Don't miss this opportunity to network and share informal conversation with authors, industry professionals, and peers.

SUNDAY, SEPTEMBER 15, 2019

Registration	7:30 a.m. - 5:00 p.m.	
S20.20	8:00 a.m. - 5:00 p.m.	FC340: ESD Program Development and Assessment (ANSI/ESD S20.20) (PrM) (Day 1)
Tutorials	8:00 a.m. - 5:00 p.m.	FC390: Basics of ESD Process Assessment
	8:30 a.m. - 4:30 p.m.	FC100: ESD Basics for the Program Manager
	8:30 a.m. - 12:00 p.m.	DD103: An Overview of Integrated Circuit ESD: The ESD Threat, Testing, Design Concepts and Debugging
	8:30 a.m. - 12:00 p.m.	DD200: Charged Device Model Phenomena, Design, and Modeling
	8:30 a.m. - 12:00 p.m.	DD/FC240: System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations
	8:30 a.m. - 12:00 p.m.	FC140: System Level for the Program Manager
	1:00 p.m. - 4:30 p.m.	DD204: ESD Design in HV Technologies
	1:00 p.m. - 4:30 p.m.	DD201: ESD Protection and I/O Design
	1:00 p.m. - 4:30 p.m.	DD/FC130: System Level ESD/EMI: Testing to IEC and Other Standards
	1:00 p.m. - 4:30 p.m.	FC220: Device Technology and Failure Analysis for the Program Manager

MONDAY, SEPTEMBER 16, 2019

Registration	7:30 a.m. - 5:00 p.m.	
S20.20	8:00 a.m. - 5:00 p.m.	FC340: ESD Program Development and Assessment (ANSI/ESD S20.20) (PrM) (Day 2)
Tutorials	8:30 a.m. - 4:30 p.m.	FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements (PrM)
	8:00 a.m. - 12:00 p.m.	DD110: ESD From Basics to Advanced Protection Design
	8:30 a.m. - 12:00 p.m.	DD231: ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures
	8:30 a.m. - 12:00 p.m.	DD300: Circuit-Level Modeling and Simulation of On-Chip Protection
	8:30 a.m. - 12:00 p.m.	DD115: Latch-up Basics and Testing
	8:30 a.m. - 12:00 p.m.	FC360: Electrical Overstress in Manufacturing and Test
	8:30 a.m. - 12:00 p.m.	DD/FC380: Electrostatic Calculations for the Program Manager and the ESD Engineer
	1:00 a.m. - 4:30 p.m.	DD117: TCAD Fundamentals and First Applications to ESD
	1:00 a.m. - 4:30 p.m.	FC121: - Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting
	1:00 p.m. - 4:30 p.m.	DD340: Integrated ESD Device and Board Level Design
	1:00 p.m. - 4:30 p.m.	DD302: Troubleshooting On-Chip ESD Failures
	1:00 p.m. - 4:30 p.m.	FC200: Packaging Principles for the Program Manager
	1:00 p.m. - 4:30 p.m.	DD/FC165: ESD Control Concepts for Design, Validation, and Test Engineers
Reception	5:00 p.m. - 6:00 p.m.	Professional and Technical Women's Reception
Welcome Reception	6:00 p.m. - 9:00 p.m.	Exhibits Open

TUESDAY, SEPTEMBER 17, 2019

Registration	7:30 a.m. - 5:00 p.m.	
Awards Breakfast	7:30 a.m. - 9:45 a.m.	Annual Meeting and Awards Breakfast
Keynote	9:00 a.m. - 9:45 a.m.	Modeling Systems with Quantum Computing Rudy J Wojtecki
Exhibits Open	9:30 a.m. - 5:30 p.m.	
Technical Sessions	10:00 a.m.-10:10 a.m.	Exhibitor Showcase in Session 1A and 1B
	10:10 a.m.-12:15 p.m.	1A: Advanced CMOS EOS/ESD and Latch-Up
	10:10 a.m.-12:15 p.m.	1B: Manufacturing I
	1:25 p.m. - 2:50 p.m.	**Hands-On Session I Manufacturing Track** **ESD TR53 - Compliance Verification of ESD Protective Equipment and Materials**
	1:25 p.m. - 1:35 p.m.	Exhibitor Showcase in Sessions 2A and 2B
	1:35 p.m. - 2:50 p.m.	2A: EOS/ESD Failure Analysis, Troubleshooting and Case Studies I
	1:35 p.m. - 2:50 p.m.	2B: Full-Custom and Application Driven ESD Concepts
	3:20 p.m. - 3:30 p.m.	Exhibitor Showcase in Sessions 3A and 3B
	3:30 p.m. - 4:45 p.m.	3A: EOS/ESD Failure Analysis, Troubleshooting and Case Studies II
	3:30 p.m. - 4:50 p.m.	3B: Manufacturing II
Study Session	5:00 p.m. - 6:00 p.m.	Calculations and ESD Scenarios Review for ESD Program Manager Exam Preparation (STUDY SESSION)
Workshops A	5:45 p.m. - 7:00 p.m.	A.1 Sub-150V CDM Testing A.2 Machine Learning and More: Advancement in Simulation and EDA methods for ESD Verification A.3 3rd Party IP and Coundry Deliveries – Problem Solved for Seamless, ESD Safe IC Top Level Integration? A.4 EOS Best Practices

WEDNESDAY, SEPTEMBER 18, 2019

Invited Breakfast	7:00 a.m. - 8:00 a.m.	University Students/Professors Invited to Breakfast with ESDA Management
Registration	7:30 a.m. - 5:00 p.m.	
Exhibits Open	8:30 a.m. - 1:30 p.m.	
Technical Sessions	8:00 a.m. - 8:40 a.m.	Year in Review: Packaging Materials for Shipment of ESD Susceptible Items
	8:55 a.m. - 9:05 a.m.	Exhibitor Showcase in Session 4A & 4B
	9:05 a.m. - 11:10 a.m.	4A: System Level EOS/ESD/EMC I
	9:05 a.m. - 11:10 a.m.	4B: Manufacturing III
Reception	12:00 p.m. - 1:30 p.m.	First Time Attendee Reception
	1:40 p.m. - 1:50 p.m.	Welcome to the IoT Workshop
	1:50 p.m. - 4:55 p.m.	IoT Workshop Session
	1:50 p.m. - 2:30 p.m.	Invited Talk
	2:30 p.m. - 3:10 p.m.	Invited Talk
	3:55 p.m. - 4:15 p.m.	Invited Talk
	4:15 p.m. - 4:55 p.m.	Invited Talk
	1:40 p.m. - 1:50 p.m.	Exhibitor Showcase in Session 5A
	1:40 p.m. - 3:40 p.m.	**Hands On Session II Manufacturing Track**
	1:40 p.m. - 1:50 p.m.	**II.A Grounding Measurements**
	1:50 p.m. - 2:00 p.m.	**II.B Assessing the Risk of Insulators and Isolated Conductors**
	2:00 p.m. - 2:40 p.m.	**II.A, II.B Demo Session**
	2:40 p.m. - 2:50 p.m.	**II.C ESD Field Meter Pitfalls and Voltage Suppression Demonstration**
	2:50 p.m. - 3:00 p.m.	**II.D Gloves**
	3:00 p.m. - 3:40 p.m.	**II.C, II.D Demo Session**
	1:50 p.m. - 3:05 p.m.	5A: System Level II
	3:30 p.m. - 3:40 p.m.	Exhibitor Showcase in Session 6A
	3:40 p.m. - 4:55 p.m.	6A: Numerical Modeling and Electronic Design Automation I
	3:55 p.m. - 5:05 p.m.	**Tutorial Session I: Manufacturing Track**
	3:55 p.m. - 4:30 p.m.	**I.A Product Qualification**
	4:30 p.m. - 5:05 p.m.	**I.B Product Qualification vs. Complance Verification**
Workshops B	5:20 p.m. - 6:35 p.m.	B.1 Adapting to the Demands of Automotive – From an ESD Perspective
		B.2 IEC Testing
		B.3 ESD Myths and Misconceptions
		B.4 IoT Workshop
Reception	7:00 p.m. - 9:00 p.m.	General Chair's Reception *Open to all Symposium Attendees and Exhibitors!*

THURSDAY, SEPTEMBER 19, 2019

Registration	7:30 a.m. - 5:00 p.m.	
Technical Sessions	8:00 a.m. - 8:40 a.m.	Year in Review: Relationships and interactions between ESD and EMC
	8:55 a.m. - 10:10 a.m.	**Discussion Group Session Manufacturing Track**
		DG.A The ESD Control Program, AH-HA! I Didn't Think About That!
		DG.B ESD Process Assesment
		DG.C ESD Packaging / Reuse of tthe Packaging
	8:55 a.m. - 9:05 a.m.	Exhibitor Showcase in Session 7A
	9:05 a.m. - 9:55 a.m.	7A: Numerical Modeling and Electronic Design Automation II
	10:20 a.m. - 10:30 a.m.	Exhibitor Showcase in Session 8A
	10:30 a.m. - 12:10 a.m.	8A: Device Testing: Testing, methods, and Correlation Issues
	10:35 a.m. - 12:20 p.m.	**Tutorial Session II Manufacturing Track**
	10:35 a.m. - 11:10 a.m.	**II.A TR2020 Handbook**
	11:10 a.m. - 11:45 a.m.	**II.B Measurements Errors and Uncertainties in High Resistance Measurements**
	11:45 a.m. - 12:20 p.m.	**II.C Importance of Equipment Verification**
Tutorials	8:30 a.m. - 12:00 p.m	DD319: Physical Process, Device, and Circuit Simulation (TCAD) Methodologies in Application to Industrial ESD Research and Design
	8:30 a.m. - 12:00 p.m.	DD260: Design for EOS Reliability
	8:30 a.m. - 12:00 p.m.	DD150: Introduction to RF ESD Design
	8:30 a.m. - 12:00 p.m.	FC120: Ionization Issues and Answers for the Program Manager (PrM)
	8:30 a.m. - 12:00 p.m.	DD/FC250: What Information Needs to be Exchanged for Potential EOS Problem
	8:30 a.m. - 12:00 p.m	FC210:ESD Standards Overview for the Program Manager
	1:00 p.m. - 4:30 p.m.	DD220: Transmission Line Pulse (TLP) Basics and Applications (DD)
	1:00 p.m. - 4:30 p.m.	FC365: Practical Applications of Ionization
	1:00 p.m. - 4:30 p.m.	FC150: Hands-on ESD Measurements & Instruments - Uses and Pitfalls
	1:00 p.m. - 4:30 p.m.	FC166: ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths
	1:00 p.m. - 2:30 p.m.	DD381: Electronic Design Automation (EDA) Solutions for ESD
	3:00 p.m. - 4:30 p.m.	DD382: Electronic Design Automation (EDA) Solutions for Latch-up

FRIDAY, SEPTEMBER 20, 2019

8:00 a.m. - 5:00 p.m. Device Design Certification Exam
8:00 a.m. - 5:00 p.m. Program Manager Certification Exam

KEYNOTE

Tuesday, September 17
9:00 a.m. - 9:45 a.m.

Modeling Systems with Quantum Computing

Rudy J. Wojtecki, IBM

The physical realization of multiqubit quantum computers (QCs) are extremely challenging as it requires the ability to control, manipulate and accurately measure an element exhibiting a quantum behavior. Recent work has demonstrated this with superconducting transmon qubits that behave like artificial atoms, acting as the quantum element capable of displaying properties of like superposition and entanglement but are macroscopic in size and composed of elements that can be handled in existing semi-conductor fabrication methods. While efforts to improving the quality of these devices have yielded progress to providing more powerful quantum computers capable of addressing more and more complex problems. While these QCs are a nascent technology, even on a system composed of 6 qubits IBM reported the development of software and uses the unique QC hardware that enabled the accurate modeling quantum systems H2, LiH and BeH2. Furthermore, the use of QC in a variety of simulations have been demonstrated that have implications in machine learning as well as artificial intelligence. As QC systems scale, the ability to simulate increasingly complex, and more useful, quantum systems will be realized. This talk will provide an introduction to QC hardware and the ability to exploit these systems in modeling complex systems.

Dr. Wojtecki graduated from Case Western Reserve University in 2013 with a Ph.D. in Macromolecular Science & Engineering under the auspices of Stuart J. Rowan (now at the Univ. of Chicago) and the support of a NASA GSRP fellowship. Dr. Wojtecki joined IBM – Almaden Research Center after completion of his graduate work, as an engineer, and promoted to Research Staff Member in 2015. He is author of 23 peer reviewed scientific publications including a Nature Materials Review article with more than 800 citations. In 2017 he was recognized as an IBM Master Inventor for work highlighted in over 100 patent and patent applications. Dr. Wojtecki's current research efforts are geared to address the fabrication of superconducting qubits for quantum computers and ongoing challenges for lithographic materials used in the manufacturing of semiconductors.

EOS/ESD Association, Inc. Professional Certification

EOS/ESD Association, Inc. offers professional certification for ESD control program managers and device design technical specialists.

ESD Certified Professional-Program Manager

The impact of the ANSI/ESD S20.20 ESD control program standard on the global industry has been extraordinary. As a result, EOS/ESD Association, Inc. recognizes the need to offer a certification program for individuals that are involved in designing, implementing, managing, and auditing ESD control programs in their facilities. The program manager certification program serves that purpose. In addition, the needs of the technical community for certification of various technical specialists are apparent.

Requirements for certification include attending required prerequisite tutorials and passing a final exam. All of the prerequisite courses cannot be completed by attending only the 2019 Symposium. Details of the certification program are also available at the registration desk.

The preferred tutorial sequence for the program manager curriculum is:

	COURSE TITLE	FACE TO FACE TUTORIAL	ONLINE
1	FC100: ESD Basics for the Program Manager	Symposium, Sunday, Sept. 15	
2	FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements	Symposium, Monday, Sept. 16	
3	FC110: Cleanroom Considerations for the Program Manager		Online Academy
4	FC120: Air Ionization Issues and Answers for the Program Manager	Symposium, Thursday, Sept. 19	Online Academy
5	FC200: Packaging Principles for the Program Manager	Symposium, Monday, Sept. 16	Online Academy
6	FC210: ESD Standards Overview for the Program Manager	Symposium, Thursday, Sept. 19	Online Academy
7	FC140 - System Level for the Program Manager	Symposium, Sunday, Sept. 15	Online Academy
8	FC220: Device Technology and Failure Analysis for the Program Manager	Symposium, Sunday, Sept. 15	Online Academy
9	DD/FC380: Electrostatic Calculations for the Program Manager and the ESD Engineer	Symposium, Monday, Sept. 16	Online Academy
10	FC340: ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)	Symposium, Sunday & Monday, Sept. 15 & 16	

ESD Certified Professional-Device Design

ESD device design certification was developed for individuals that are involved in designing, testing, characterizing, and implementing improved ESD protection designs. Device design certification demonstrates knowledge, experience, and competency in the area of ESD design and test for device protection.

Requirements for certification include attending required prerequisite tutorials and passing a final exam. All of the prerequisite courses are not available in the 2019 Symposium tutorial program. Details of the certification program are also available at the registration desk.

The preferred tutorial sequence for the device design curriculum is:

	COURSE TITLE	FACE TO FACE TUTORIAL	ONLINE
1	DD110: ESD Basics for Advanced Protection Design	Symposium, Monday, Sept. 16	
2	DD301: SPICE-Based ESD Protection Design Utilizing Diodes and Active MOSFET Rail Clamp Circuits		
3	DD211: EOS/ESD Failure Models and Mechanisms		
4	DD102: On-Chip ESD Protection in RF Technologies		Online Academy
5	DD200: Charged Device Model Phenomena, Design, and Modeling	Symposium, Sunday, Sept. 15	Online Academy
6	DD112: Latch-up Fundamentals		Online Academy
7	DD300: Circuit-Level Modeling and Simulation of On-Chip Protection	Symposium, Monday, Sept. 16	
8	DD302: Troubleshooting On-Chip ESD Failures	Symposium, Monday, Sept. 16	
9	DD120: Device Testing--IC Component Level: HBM, CDM, MM, and TLP		
10	DD311: Impact of Technology Scaling on ESD High Current Phenomena and Implications for Robust ESD Design		
11	DD220: Transmission Line Pulse (TLP) Basics and Applications	Symposium, Thursday, Sept. 19	
12	DD/FC130: System Level ESD/EMI: Testing to IEC and other Standards	Symposium, Sunday, Sept. 15	Online Academy

ESDA Certification Exams

The certified professional program manager and device design exams will be held on Friday, September 20. To take the exam, applicants must have a registration form on file with EOS/ESD Association, Inc. headquarters complete with a $50 filing fee prior to the Symposium.

FC340: ESD Program Development and Assessment (ANSI/ESD S20.20)

8:00 a.m. - 5:00 p.m.

Kevin Duncan, Seagate Technology; David E. Swenson, Affinity Static Control Consulting, LLC

Certification: PrM

This seminar provides instruction on designing and implementing an ESD control program based on ANSI/ESD S20.20. The course provides participants with the tools and techniques to prepare for an ESD facility audit. This two-day course is an ESDA certification requirement for in-plant auditors and program managers who are working toward professional ESD certification.
The following topics are covered in this course:

- Overview of ANSI/ESD S20.20
- How to approach an assessment
- Administrative elements
- ESD program assessment
- ESD program techniques for different applications
- Technical elements
- Overview of the assessment process
- The audit checklist and follow-up questions

It is recommended that the ESD Program Development and Assessment (ANSI S20.20) be taken after the certification candidate has taken most of the other program manager related tutorials.

TUTORIALS: SUNDAY, SEPTEMBER 15

FC100: ESD Basics for the Program Manager

8:30 a.m. - 4:30 p.m.

Ron Gibson, Advanced Static Control Consulting

Certification: PrM

This tutorial provides the foundation material for understanding electrostatics and ESD and their role in the manufacturing and handling of ESD sensitive devices. The fundamental properties of charge, electric fields, voltage, capacitance, and current are discussed with a view towards understanding key electrostatic phenomena and electrical processes. These include charge generation and decay, material properties, and induction. An overview of device failure mechanisms is presented, including how these models impact ESD control programs. Finally, the course provides an overview of ESD control procedures during handling and manufacturing and an overview of ANSI/ESD S20.20 program requirements. This full day course is required for those in-plant auditors and program managers who are working toward professional ESD certification. The presentation includes many in-class demonstrations, videos, and animated slides.
Some sample topics covered in this course are:

- Definitions and relationships among important electrical and mechanical properties
- Causes of charge generation and decay
- Field effects and voltages
- Role of capacitance in ESD (Q=CV)
- Overview of key measurements including common pitfalls of some measurements
- Review of ESD failure models
- Understanding and demonstrating electrostatic induction
- Utility and limitations of air ionization
- Basic goals of ESD controls
- Properties of effective ESD control products and materials
- Overview of ANSI/ESD S20.20 ESD program development requirements

Customized, full color tutorial notes will be provided to each tutorial registrant.

FC390 - Basics of ESD Process Assessment

8:00 a.m. - 5:00 p.m.

Reinhold Gaertner, Infineon Technologies; Wolfgang Stadler, Intel Deutschland GmbH

This tutorial gives an introduction to the approach and measurement methodologies for ESD process assessment and ESD risk analysis in typical production processes in semiconductor, printed-circuit board (PCB), and electronic system manufacturing industries. It summarizes the relevant physical parameters (e.g., resistance, charge, electric fields, capacitances, resistances, discharge currents, and ESD event detection by EMI) and discusses their influence on the ESD risks caused by charged personnel, charged devices and boards, and ungrounded conductors. Measurement techniques are explained in detail together with their limitations for the different process steps and strategies for an efficient ESD risk assessment. The application of those measurement techniques to assess possible ESD risks and to solve ESD problems are explained using theoretical and real-world case studies from each of the processes mentioned above. Examples of possible mitigation strategies are discussed with the attendees. The tutorial includes practical demonstrations and a hands-on session for the attendees to get experience and learn pitfalls of the most important measurement techniques used in ESD process assessment.

DD200: Charged Device Model Phenomena, Design, and Modeling

8:30 a.m. - 12:00 p.m.

Michael Chaine, Micron Technology, Inc.; Melanie Etherton, NXP Semiconductors

Certification: DD

This course teaches basic ESD circuit design concepts and ideas required to design ESD protection for charge device model (CDM) ESD tests. The course covers a brief history of CDM ESD development, charge and discharge physics, characterization methods, CDM failures mechanisms, and CDM design-in strategies.

CDM ESD circuit design approaches and simulation setups for CDM failure debugging are presented in this tutorial on the basis of case studies. Insight into CDM circuit simulation requirements and physical aspects of the CDM ESD phenomenon that are important for reproducing the event with circuit simulation will be taught, and modeling approaches for CDM specifi c device physical effects necessary for accurate circuit simulation will be introduced. This course also teaches methods for simplifi ed CDM circuit simulations where detailed information is either not available or too complex to simulate.

The course focuses on what type of circuits fail during a CDM discharge event and teaches the different types of ESD design circuit strategies that can be applied to protect those circuits. This class covers basic to advanced topics for CDM ESD design, but the student is assumed to already have a basic understanding of the CDM test method.

DD103 - An Overview of Integrated Circuit ESD: The ESD Threat, Testing, Design Concepts and Debugging

8:30 a.m. - 12:00 p.m.

Alan Righter, Analog Devices

Many Integrated Circuit (IC) designers do not have a working knowledge of ESD. This tutorial presents aspects of ESD that are relevant to IC designers and will enable them to improve their first time right ESD track record. This tutorial will also be useful for a wide range of specialists including layout designers, I/O designers, test engineers, failure analysis engineers, quality and reliability engineers, and architects as well as ESD design engineers just entering the field. The student will learn the fundamentals of ESD design, know the variables which affect ESD robustness, understand that ESD design needs to be addressed early in the design cycle and be better able to interact with ESD design specialists, understand ESD testing and interpret failure analysis data.

NEW DD/FC240 - System Level ESD/ EMI: Principles, Design Troubleshooting, & Demonstrations

8:30 a.m. - 12:00 p.m.

Jay Skolnik, Skolnik Technical Training

Certification: PrM

System level ESD tutorial about how to reduce ESD effects on systems (boards, chassis, etc.). Real circuits will be demonstrated in class showing techniques to correct the detrimental effects. Theory and real-life examples from recent past will be used to substantiate the methods.

Customized, full color tutorial notes will be provided to each tutorial registrant.

FC140 - System Level for the Program Manager

8:30 a.m. - 12:00 p.m.

John Kinnear, IBM Corporation

Certification: PrM

This tutorial is intended to help those tasked with testing products to IEC and other system level ESD standards by providing detailed information on IEC 61000-4-2, the most widely used standard, and highlighting the harmonization and differences among IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test set-ups, test points, and procedures, and address key issues, including: 1) Differences between "verification" and "calibration" and when is each required; the influence of ESDA WG14 technical report (TR) on IEC and how it affects the calibration and verification procedures. 2) Test set-up requirements, the test environment, ground connections, and return paths and ground plane effects. 3) Testing procedures with demonstration on actual products, how the tester affects test results, and problems with test result variations due to simulator influences. 4) What points need to be tested and why, guidance on determining "operator accessible" points and ports, exempted points and ports, and what to do around connectors and connector pins. 5) ANSI and other ESD standards, the drive toward harmonization with IEC, why standards will probably never be the same as IEC, and the scope of different standards. This system level ESD tutorial will cover several facets of ESD as applied to electronic systems.

DD204: ESD Design in HV Technologies

1:00 p.m. - 4:30 p.m.

Lorenzo Cerati, STMicroelectronics; Ulrich Glaser, Infineon Technologies AG

This tutorial gives an introduction to ESD design in high voltage technologies for integrated circuits with pin voltages from 12 volts upwards. After a short introduction of typical applications and requirements, an overview of different technologies and the typical device portfolios in these technologies will be given. Different ESD protection concepts are introduced, analyzing advantages and disadvantages of the various possible approaches to implement ESD networks (diodes, snapback devices, active clamps, etc.). Finally, HV technology and design related challenges regarding ESD protection are discussed, with a special focus on the formation of parasitic bipolar devices and the impact on the circuit's ESD performance. The attendee will gain a good basic knowledge of the main characteristics of HV technologies, the different ESD protection concepts, and ESD protection challenges that are specifi c for HV technologies. This will be a help for understanding and further development of HV ESD protection. An extensive literature list is provided for further study of various subjects regarding HV ESD.

DD201: ESD Protection and I/O Design

1:00 p.m. - 4:30 p.m.

Michael Stockinger, NXP Semiconductors

This tutorial is intended to provide the attendees with the tools to take a device and circuit level understanding of ESD protection methods and implement them effectively in I/O designs for CMOS bulk technologies. Beginning with a review of common ESD protection strategies, this course will focus more directly on how to build ESD-robust I/O cells and how to integrate them on a full chip. The tutorial will cover various types of I/O pads including analog, RF, and digital pads. Different types of ESD protection strategies and their usage in I/O pad cells will be described, for example, rail clamp, self-contained, and SCR based protection schemes. This course will also discuss the decisions and challenges which ESD and I/O designers typically face when designing I/O pads. More complex ESD solutions will also be described such as stacked rail clamps, ghost rails, and protecting signals that can swing below ground or above the supply. Finally, this tutorial will touch on various supply schemes including multiple power domains and isolated grounding schemes. It will end with discussing pad ring construction aspects for both wire-bond and flip-chip packages.

DD/FC130 - System Level ESD/EMI: Testing to IEC and Other Standards

1:00 p.m. - 4:30 p.m.

Jeff Dunnihoo, Pragma Design, Inc.

Certification: DD

This tutorial is intended to help those tasked with testing products to system level ESD standards by providing first an overview of how real-world system ESD events are simulated in different standards and testers in general, and then provide detailed information on IEC 61000-4-2, the most widely used standard. This introduction will highlight the similarities and differences between IEC, ANSI, Telcordia, and some automotive ESD standards. We will answer common questions regarding test setups, test points, and procedures, and address key issues, including: 1) differences between "verification" and "calibration" and when is each required; 2) test equipment requirements, the test environment, ground connections, return paths, and ground plane effects. 3) Testing procedures with demonstration on actual products, how the tester and procedure affects test results, and problems with test result variations due to simulator influences; 4) definitions of testing failure criteria for the product; 4) what points need to be tested and why, guidance on determining "operator accessible" points and ports, exempted points and ports, and what to do around connectors and connector pins. 5) ANSI and other ESD standards, the drive toward harmonization with IEC, the scope of different standards, and why they are unlikely to converge. This system level ESD tutorial will cover different perspectives on ESD as applied to electronic systems from the user's, the designer's, and even the designer's competitor's points of view.

Customized, full color tutorial notes will be provided to each tutorial registrant.

TUTORIALS: SUNDAY, SEPTEMBER 15

FC220 - Device Technology and Failure Analysis for the Program Manager

1:00 p.m. - 4:30 p.m.

Terry Welsher, Dangelmayer Associates, LLC

Certification: PrM

This tutorial provides an overview of the device technology used to provide ESD protection, ESD protection techniques, and Failure Analysis (FA) techniques to debug non-working ESD protection. This class does not go into the depth necessary to equip the student to be an ESD Protection Designer or an ESD Failure Analysis Engineer. It does familiarize the student with the terms and concepts of ESD protection and FA to allow the student to interact and understand the work being done by the Designer or Failure Analyst. After completing this tutorial the student should be able to understand the basics of device ESD protection design and some of the trade-offs inherent in that process. The student should also be familiar with the most commonly used failure analysis techniques and tools used to identify the root cause of an ESD failure. The topics covered include: the three most common ESD Models: HBM, CDM and System Level (IEC); characteristics of ideal ESD protection; ESD failure analysis schemes; key characteristics of real ESD protection; failure analysis flow; failure analysis tools and how they are applied to ESD failures.

TUTORIALS: MONDAY, SEPTEMBER 16

FC101: How To's of In-Plant ESD Auditing and Evaluation Measurements

8:30 a.m. - 4:30 p.m.

Ted Dangelmayer, *Dangelmayer Associates, LLC*

Certification: PrM

Compliance verification is one of the most important elements of ESD program management and there are many technical and administrative pitfalls that can be avoided. The attendee will learn not only how to make valid auditing measurements in accordance with ESD TR53 – Compliance Verification of ESD Protective Equipment and Materials, but also how to recognize and avoid common pitfalls. Common instruments will be explained as well as the invalid test results that can result when they are used incorrectly. Advanced auditing techniques will also be covered that enable Class 0 devices to be handled successfully. There are many ways to administer effective compliance verification programs. Two successful examples will be presented that were developed independently by different companies. Hidden administrative pitfalls that often result in poor compliance will also be discussed. This tutorial will be highly interactive with live demonstrations, in-plant photographs, and compelling video clips. Students will be encouraged to ask questions and to participate in the discussions.

Customized, full color tutorial notes will be provided to each tutorial registrant.

DD110: ESD From Basics to Advanced Protection Design

8:00 a.m. - 12:00 p.m.

Charvaka Duvvury, ESD Consulting, LLC

Certification: DD

This course gives a comprehensive overview from ESD basics to ESD on-chip design principles, covering up to the latest silicon technologies appealing to a variety of engineers from design to process technology, and failure analysis to quality. The attendee will have an in-depth understanding of the principles of ESD device design along with a full perception of what it takes to address almost every kind of design scenario, how to apply rules of thumb for successful on-chip design, knowledge of lessons learned from case studies, and empowerment to communicate with customers on ESD quality issues. In its complete ESD overview, the course offers emphasis on on-chip protection methods including an understanding of any interactions to the eventual system protection.

DD231: ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures

8:30 a.m. - 12:00 p.m.

David Pommerenke, University of Missouri-Rolla

The tutorial is an expanded version of the previous DD231 tutorial on system level ESD. The main difference is the addition of many experimental demonstrations, update of information, and in-depth discussion on problems of the IEC 61000-4-2 testing, with examples on how to perform this testing and obtain the best possible results and documentation. About half of the time will be spent on experimental demonstrations. Topics will include:

- ESD physics: charging and discharging.
- System level ESD testing
- System level soft failure mechanisms and debugging
- Design for avoiding ESD problems

DD300 - Circuit-Level Modeling and Simulation of On-Chip Protection

8:30 a.m. - 12:00 p.m.

Elyse Rosenbaum, University of Illinois at Urbana-Champaign

Certification: DD

This tutorial addresses modeling of on-chip ESD protection devices and simulation of ESD protection networks. The primary focus is SPICE-type simulation with compact (physics-based) models but a general survey of modeling approaches and simulation techniques will also be provided. The physical operating principles of commonly-used ESD protection devices will be examined. The high-current characteristics and transient responses of those devices will be explored to ascertain what behaviors should be captured by a model intended for circuit-level simulation of ESD.

Specific examples of model implementations will be provided. Techniques for circuit-level modeling of self-heating will be presented. Parameter extraction and model scalability will be addressed. This tutorial assumes some familiarity with device physics. It is directed toward persons with interests in semiconductor device physics, electronic design automation, and on-chip ESD protection circuit design.

REVISED DD115: Latch-up Basics and Testing

8:30 a.m. - 12:00 p.m.

Marty Johnson, Texas Instruments, Inc.

This tutorial will introduce the participant to the basics of latch-up stress testing. The course will cover basic latch-up theory, basic latch-up mitigation techniques, the JEDEC Latch-up Standard (JESD78) and discuss the effects of the standard on stress testing methodology. Also, there will be a discussion of possible differences in set-up when stress testing between digital, mixed signal and analog products. Examples of these set-ups will be described and discussed to aid the student better apply the methods in their stressing environment. Interpretation of the stress data will be described. The future of the standard will also be discussed and how that may impact the philosophy of stressing. This tutorial can be very helpful for a variety of people in the semiconductor industry including circuit designers, product engineers, test engineers, failure analysts, quality / reliability engineers and technicians supporting latch-up stressing.

Customized, full color tutorial notes will be provided to each tutorial registrant.

FC360: Electrical Overstress (EOS) in Manufacturing and Test

8:30 a.m. - 12:00 p.m.

Reinhold Gaertner, Infineon Technologies

Electrical overstress (EOS) is a major cause of device failure in manufacturing and in the field. Despite this, there is relatively little information on the sources of EOS and on prevention practices, particularly for the factory. In this tutorial, the fundamentals of device overstress are reviewed. Relationships among device EOS stressing models, such as the Wunsch-Bell curve, are discussed. The causes of EOS and EOS-like events in manufacturing are described and categorized by source and by stress-type. The difficulties in distinguishing between power-induced EOS and high current ESD events such as charged-board events (CBE) and cable discharge events (CDE) are discussed. Case histories, including failure analysis and root cause determination, are presented and the few relevant industry specifications are reviewed.

REVISED DD/FC380 - Electrostatic Calculations for the Program Manager and the ESD Engineer

8:30 a.m. - 12:00 p.m.

Terry Welsher, Dangelmayer Associates, LLC

This tutorial focuses on the basic calculations and techniques of use to the program manager and the ESD engineer. The content is at the introductory college pre-calculus and introductory college physics level set in the context of electrostatic discharge and its effects. It is suggested that the student gain some familiarity with these subjects prior to the tutorial. Topics covered include the electric force, the electric field and Coulombs law, electric potential, and voltage. Gauss' Law is discussed as it relates to the electric field, induction, and the Faraday cup. The capacitance in Q = CV is used to explain charge sharing. RC decay is discussed as it relates to ESD discharge from humans, devices, wrist straps, and materials. After completing this course, the attendee should leave with a proper understanding of the differences among the calculations for peak current, power, energy, and threshold voltage for a simple device.

REVISED DD117 - TCAD Fundamentals and First Applications to ESD

1:00 p.m. - 4:30 p.m.

Kai Esmark, Infineon Technologies

TCAD (technology computer aided design) tools have become an indispensable utensil for the semiconductor industry. The possibilities to analyze, predict and optimize a certain semiconductor device behavior through modeling semiconductor fabrication (Process TCAD) and semiconductor device operation (Device TCAD) are countless. This includes the area for ESD and Latch-up development, as early access to fundamental device parameters under very high current density and high temperature transients is the key to overcome the conceptual problem of concurrent engineering for ESD engineers.

This tutorial serves as a basic introduction into TCAD tool chain including process and device simulation as well as the creation and integration of compact models for mixed more simulation. Focus points are the capabilities but also limitations of these tools, like the requirements for a 2D/3D simulation approach and the validity of the models describing the fundamental physics, especially in the high temperature regime.

DD340 - Integrated ESD Device and Board Level Design

1:00 p.m. - 4:30 p.m.

Harald Gossner, Intel Deutschland GmbH

The tutorial is a hands-on training course for performing a simulation based optimization of PCB ESD protection design and provides deep understanding of the relevant performance criteria both of TVS diodes and IO circuits. The presented method follows the system effi cient ESD design (SEED) approach as recommended by the Industry Council on Target Levels and JEDEC.

The method allows the achievement of correct first time PCB builds and reduces the respin effort for boards and ICs. Based on a TLP characterization of SoC interface circuits and TVS diodes, simulation models for impedance and clamping behavior, as well as failure threshold, are extracted. These are used to assess design solutions by transient simulations. This is showcased by real world examples.

Customized, full color tutorial notes will be provided to each tutorial registrant.

TUTORIALS: MONDAY, SEPTEMBER 16

DD302 - Troubleshooting On-Chip ESD Failures

1:00 p.m. - 4:30 p.m.

Hans Kunz, Texas Instruments

Certification: DD

Diagnosing and fixing on-chip ESD product qualification failures can often be one of the more challenging aspects of work in ESD. The pressure to quickly find and correct an HBM/MM/CDM failure in order to qualify a product often compounds the inherent difficulty of troubleshooting. Experience diagnosing failures, though not desirable from a product qualification standpoint, can greatly improve troubleshooting skills. This tutorial will build troubleshooting experience and skills by presenting case studies of actual on-chip HBM failures in a workshop format. The evidence for each case will be revealed and the failure analyzed in the same manner as an actual failure. Participants will be led through and allowed to analyze each failure case, interacting with the instructor to determine its root cause and a solution. This tutorial will identify common concepts, methods, and tools useful in failure diagnosis. Participants should be familiar with CMOS technology, on-chip ESD breakdown phenomena, standard ESD protection circuits, and the HBM test procedure. Participants should also be acquainted with basic CMOS circuit design, should be able to read circuit diagrams, and should have a basic understanding of the function of IO circuits.

DD/FC165 - ESD Control Concepts for Design, Validation, and Test Engineers

1:00 p.m. - 4:30 p.m.

Ginger Hansel, Dangelmayer Associates, LLC

Design Engineers strive to incorporate ESD protection into chip designs, but they are often unclear about the best way to handle the physical devices. The Industry Council on ESD Targets documented a need to lower both the HBM and CDM thresholds with the confidence that factories already had the appropriate ESD control programs in place. However, many engineering labs do not understand or follow industry ESD guidelines and are unaware of the potential jeopardy created by these lower thresholds. Anyone doing device testing, characterization, TLP stress testing, board level analysis or upgrading their own computer should know basic ESD control techniques. This seminar will include practical ESD control tips for engineering labs as well as how to set up and monitor a comprehensive ESD control program. Real world examples will show the increased ESD risk of Charged Board Events (CBE), the surprising damage due to hand tools and how to use event detectors to identify ESD threats.

You've spent a lot of effort doing careful designs – now take good care of your valuable test chips and prototype engineering samples.

NEW

FC200 - Packaging Principles for the Program Manager

1:00 p.m. - 4:30 p.m.

Craig Zander, Transforming Technologies

Shipping electronic parts within a factory, to another factory, distributor, or to an end-user has always been an area of uncertainty within the manufacturing process.
To provide clear-cut information on what type of controlled packaging should be used in any situation, EOS/ESD Association, Inc. released a comprehensive revision of the obsolete industry standard EIA 541-1988. The newer document, ANSI/ESD S541, is the focus of this inclusive session. It provides information and guidance, as well as material specifi cations, to assist in the design and implementation of a packaging plan for use within an ANSI/ESD S20.20 based ESD control program. Current and newly released test method standards suitable for packaging material evaluation will be described. Course credit applies to the ESD program manager certifi cation curriculum. Previous attendance at the " FC100: ESD Basics" and "FC101: How To's" tutorials are highly recommended.

NEW

FC121 - Grounding – Variations, Concepts, Nuisances, Equipment & Troubleshooting

1:00 p.m. - 4:30 p.m.

Jay Skolnik, Skolnik Technical Training

Grounding for ESD control seems so simple, yet many times issues arise after a grounding strategy is implemented. This class will cover variations in grounding approaches, concepts to consider when employing a ground system, nuisances and how to troubleshoot them with the correct equipment.

Customized, full color tutorial notes will be provided to each tutorial registrant.

DD260: Design for EOS Reliability

8:30 a.m. - 12:00 p.m.
Charvaka Duvvury, ESD Consulting, LLC

During the design of on-chip protection and latch-up immunity, the consequences to EOS damage susceptibility are often overlooked. This class aims to fi rst clearly establish the nature of EOS and some of the common causes for unintended EOS, followed by the on-chip IC design styles that can lead to EOS damage and customer returns. By way of illustrative examples and case studies, these potential issues are highlighted. These include the designs in low voltage CMOS, mixed voltage technologies, analog designs, and high voltage designs. Some mention of automotive applications leading to EOS and the automotive perspective will also be covered. Finally, the design rules to follow for EOS mitigation; as well as on-going communication tips with customers to achieve these objectives, will be reviewed.

The course aims to give a clear understanding of EOS events, the defi nition of EOS related to on-chip design principles, design improvements to overcome EOS return rates, check lists for EOS avoidance, and tips for customer communications.

NEW

DD150 - Introduction to RF ESD Design

8:30 a.m. - 12:00 p.m.
Kathleen Muhonen, Qorvo

This tutorial is an introduction to RF concepts and RF ESD clamp design. It is intended for ESD engineers who do not have an RF background to come up to speed on the concepts needed to design effective protection circuits. The RF concepts include impedance matching and smith chart basics. RF amplifier operation and load line basics are presented to give a foundation for the RF ESD protection circuit design. The tutorial will also touch briefly on RF switches and filters. The second half of the tutorial will focus on how to design an ESD clamp for an RF application. Concepts will be presented such as calculating the turn-on voltage of the clamp such that it will protect the part but not turn on during normal, RF operation. A clamp's parasitics also needs to be considered in an RF application so that the parasitics do not degrade the product's performance. Finally, some testing tools will be reviewed with respect to testing RF products. The challenges will be highlighted and different testing practices that are used in HBM, TLP and IEC testing of RF products will be reviewed.

DD319 - Physical Process, Device and Circuit Simulation (TCAD) Methodologies in Application to Industrial ESD Research and Design

8:30 a.m. - 12:00 p.m.
Vladislav Vashchenko, Maxim Integrated Corp.

Over the last two decades numerical simulation with commercially available technology CAD (TCAD) tools has been widely applied across industry and research organizations to address ESD protection design challenges, ESD solutions development, test chip design and validation of the device, clamp circuits, and application circuit blocks as well as interpretation of the failure analysis results. Corresponding significant and diverse material has been accumulated in the literature and unpublished industry practices. At the same time the best practices and methodologies were not adequately summarized to bring them a broader audience in an easily accessible and practical, usable way. As a result, these are way underused today. The purpose of this tutorial is provide a comprehensive structured review of the published ESD TCAD results and construct a step-by-step approach to successful methodology and best practices application. The presented material achieves this goal in several steps: (i) means of review and classification of the most relevant studies where the ESD problems have been addressed through TCAD simulation; (ii) derivation of a generic physical simulation workflow based upon either process simulation or parameterized device definition followed by device simulation and mixed-mode analysis in ESD time domain; (iii) outlining and classifying the major application physical ESD problems which can be addressed through 2D or 3D TCAD analysis. The presentation material is supported by numerous easy-to-understand simulation examples.

DD/FC250 - What Information Needs to be Exchanged for Potential EOS Problem

8:30 a.m. - 12:00 p.m.
Reinhold Gaertner, Infineon Technologies;
James Roberts, Stoneridge, Inc.

EOS-like damages represent a significant percentage of components returned by the OEM's to tier1 and semiconductor manufacturers for comprehensive failure analysis in the automotive industry. There is generally a requirement from the OEM to conduct a detailed investigation to determine the root cause of the failure; however, commonly this cannot be done due to missing information and poor communications but blocks a lot of capacity. This tutorial presents information based on case studies why it is not possible to find the root cause for an EOS-like damage without an information sharing between all tier levels. Based on the new guideline a two level support will be introduced based on an information sharing between the OEM, tier1 and semiconductor manufacturers that can lead to a higher chance to identify the root cause of the damage and allows to focus on the important topics.

FC120 - Ionization Issues and Answers for the Program Manager

8:30 a.m. - 12:00 p.m.

Kevin Duncan, Seagate Technology

Certification: PrM

The primary method of static charge control is direct connection to ground for conductors, static dissipative materials, and personnel. Air ionization is also part of a static control program to deal with the problems of isolated conductors and insulating materials. This seminar is a basic course on ionizers, providing an introduction to their use, as well as application information. It examines common problems caused by static charge and the need for ionizers in a static control program. Types of ionizers, their use environments, and performance test methods using the Ionization Standard will be demonstrated. Installation, safety, maintenance, and contamination issues will be presented. Finally, case histories will be analyzed illustrating the use of ionizers in a variety of work environments.

FC150: Hands-on ESD Measurements & Instruments-Uses and Pitfalls

1:00 p.m. - 4:30 p.m.

Ginger Hansel, Dangelmayer Associates, LLC

Accurate data is the foundation of effective ESD program management. This hands-on tutorial will explain and demonstrate the proper use of ESD test equipment such as static locators, resistance meters, charge plate monitors, and event detectors. We will examine pitfalls of using these common instruments that can result in an incorrect representation of the ESD risk. For example, static locators can give misleading readings if the effects of voltage suppression are not taken into account. We will also discuss the effective use of ionization since ionizers that are not measured, maintained, and located correctly may contribute ESD hazards to the work area. Each student will participate in class exercises to perform these tests. The hands-on experience is the best way to understand the seriousness of the pitfalls and the benefits to taking the proper precautions. What you learn will help you avoid frequent auditing problems and improve your compliance verification program.

NEW FC210 - ESD Standards Overview for the Program Manager

8:30 a.m. - 12:00 p.m.

Craig Zander, Transforming Technologies

Certification: PrM

The ESD Association's introduction of the Program Manager Certification curriculum has created a need to modify the Standards Tutorial that has been presented for a number of years, mainly to help individuals prepare for the iNARTE Engineering and Technician Exams. Currently, many of the ESDA Standards and Standard Test Methods are discussed in depth in the individual tutorials related to the specific subject matter. This Standards Tutorial provides an overview of all the Standards, grouped into common test types, based on measurement probe and test instruments. A common methodology is used in this tutorial to cover the requirements, applications and specifications for each Standard and Standard Test Method.

DD220: Transmission Line Pulse (TLP) Basics and Applications

1:00 p.m. - 4:30 p.m.

Evan Grund, Grund Technical Solutions, Inc.

Certification: DD

This tutorial will cover the basics of TLP including underlying theory, the types of TLP systems available, and how I-V curves are extracted from TLP pulses. The tutorial uses examples to show how fundamental device parameters can be measured with TLP. These parameters allow the ESD engineer to understand a technology's properties which can be used to design successful ESD protection circuits. The student will gain an understanding of the purpose of TLP measurements, how TLP relates to HBM and CDM, fundamentals of how TLP systems work, including impedance and refl ections, types of TLP systems, importance of load lines, adaptive ranging, TLP calibration, time dependence from TLP, and biased TLP measurements. The tutorial will present examples of TLP use for nMOS transistors, diodes, oxides/capacitors, and power supply clamps, as well as time dependent TDR-O and VF-TLP examples.

Customized, full color tutorial notes will be provided to each tutorial registrant.

NEW FC166 - ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths

1:00 p.m. - 4:30 p.m.

Ted Dangelmayer, Dangelmayer Associates, LLC

While most companies are acutely aware of the hazards of ESD (electrostatic discharge), few are aware that the ESD QMS Strategy is equally important as the technical requirements. This is especially true for the extreme ESD sensitivities of Class 0 since the trend toward Class 0 devices is escalating rapidly. Furthermore, most companies do not know what their device sensitivities are because 90% of IC datasheets do not include CDM Sensitivity data. The absence of this data and the lack of understanding of ESD QMS best practices has reached a critical stage.

S20.20 (ANSI/ESD S20.20) is the best industry standard available and is an excellent foundation for ESD QMS best practices programs. However, companies with advanced technologies have found they must customize the technical requirements of S20.20 and introduce sound ESD QMS practices to avoid unacceptable failure rates in the factory and field.

Join us for this interactive presentation and learn if you are at risk and how to establish a robust ESD QMS strategy. You will also learn how to obtain ESD CDM & HBM device sensitivity data as well as how to prepare for Class 0.

There are several common misunderstandings and controversies that can have significant impact on costs, quality and reliability of ESD programs. These misunderstandings or "myths" often result in costly unnecessary expenditures and/or a compromise of the program integrity. These same myths are cited by skeptics who do not fully understand the physics involved. Consequently, it is important to identify and dispel these myths.

Latency is a significant reliability consideration that is surrounded with controversy. Some experts will argue that latency is virtually non-existent while others claim that it is the dominant failure mode. Join us for this highly interactive discussion and learn about Latency as well as common myths such as:

Myth: Circuit Boards are Less Sensitive to ESD than Devices
Myth: HBM Data Are Sufficient for Determining Device Sensitivity Levels
Myth: MM Is A Valid Simulation Related To Machines
Myth: Air Flow Causes Charging
Myth: Metalized or Highly Conductive Shielding Layers Are Essential
Myth: Humidity Control is Essential for ESD
Myth: Latency Failures Comprise 90% of ESD Failures

FC365 - Practical Applications of Ionization

1:00 p.m. - 4:30 p.m.

David E. Swenson, Affinity Static Control Consulting, LLC

Ionization is a powerful tool in the toolbox of an ESD control practitioner. Our half-day tutorial, "Ionization Issues and Answers for the Program Manager" goes into depth about the physics of ionization, and general applications. This tutorial builds on the fundamentals and provides added information about applications of ionization that go beyond those mentioned in the original tutorial. The introduction part of this tutorial begins with a review of the physics of ionization before entering the discussion of applications. Ionization is used in a wide variety of industrial applications to reduce charge on plastic and paper films, extrusion processes, pharmaceutical and other powders, petrochemical processing, printing and graphic arts, as well as the wide variety of electronic component and equipment production processes. Numerous demonstrations will help demonstrate the power of ionization to reduce charges on materials. In addition, it is necessary to understand the limitations of ionization and recognize where it is useful and where it is not.

Customized, full color tutorial notes will be provided to each tutorial registrant.

DD381: Electronic Design Automation (EDA) Solutions for ESD

1:00 p.m. - 2:30 p.m.

Michael Khazhinsky, Silicon Laboratories, Inc.

The verification of ESD protection networks in modern integrated circuits is a diffi cult challenge due to increasing design and process complexity, higher pin-counts, and the overall computational difficulties in dealing with large data sets. Most chips today are segmented into multiple power domains, where ESD currents must necessarily be shunted from one domain to another; across multiple-layer interconnect paths that span major portions of the chip. Furthermore, circuit blocks that are traditionally not associated with the I/O ring and which may be far from the I/O circuits themselves, may become damaged as a result of the high voltages and currents produced during an ESD discharge. Relying on manual verification alone poses a signifi cant risk of missing hidden ESD pitfalls. Consequently, automated ESD and latch-up rule checking is highly desired. An optimum verification flow should provide broad and flexible design rule coverage and allow incremental verification as a design progresses to avoid late-stage changes just before tape out. The integration of ESD checking tools into the standard design flow allows these rules to be used directly by IC designers to identify and correct most ESD issues prior to meeting with the ESD experts. This tutorial will outline the essential requirements of the ESD electronic design automation (EDA) verification flow which would be aligned within the IC design community, as discussed in the recently released ESDA technical report ESD TR18.0-01-15 (ESD Electronic Design Automation Checks). The tutorial will give an overview of existing ESD EDA solutions across industry, including both commercial and in-house EDA tools and flows for automated ESD checks and will discuss directions for future ESD EDA tool development.

DD382: Electronic Design Automation (EDA) Solutions for Latch-up

3:00 p.m. - 4:30 p.m.

Michael Khazhinsky, Silicon Laboratories, Inc.

The verification of latch-up protection networks in modern integrated circuits is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, and the overall computational diffi culties in dealing with large data sets. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verifi cation. These checks are typically focused on layout topology. However, electrical information for latch-up risk areas throughout the chip is not readily available. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. Consequently, a fully automated latch-up rule checking approach analyzing electrical information is highly desired.

In this tutorial we will review a typical latch-up prevention fl ow. Then, the dual DRC and Calibre PERC-based latch-up verification flow will be shown. We will then provide an example of identifying latch-up injectors and describe how this information could be used in both a DRC and Calibre PERC based verification flows. Afterwards, the tutorial will introduce the concept of context based checking as it applies to latch-up spacing checks. An example of validating latch-up prevention techniques for the devices in grounded nwell will be shown along with additional latch-up verification case studies related to guard rings and well ties.

Customized, full color tutorial notes will be provided to each tutorial registrant.

Exhibitor Showcase 10:00 AM-10:10 AM

Session 1A: 10:10 AM-12:15 PM
1A: Advanced CMOS EOS/ESD and Latch-up
Moderator: Souvick Mitra, GlobalFoundries

1A.1 Transient Overshoot of Sub-10 nm Bulk FinFET ESD Diodes with S/D Epitaxy Stressor
Shih-Hung Chen, Dimitri Linten, Geert Hellings, Marko Simicic, Thomas Chiarella, Pierre Eyben, Stefan Kubicek, Erik Rosseel, Andriy Hikavyy, Anda Mocuta, Naoto Horiguchi, imec

New process options in CMOS technology scaling often result in degradation of ESD device performance. TCAD simulations bring an in-depth look at the impact of S/D epitaxy process options with channel strain engineering on CDM-time domain turn-on transient overshoot of ESD diodes in next generation bulk FF and GAA technologies.

1A.2 Low-Capacitance SCR for On-Chip ESD Protection with High CDM Tolerance in 7 nm Bulk FinFET Technology
Po-Lin Peng, Li-Wei Chu, Ming-Fu Tsai, Yu-Ti Su, Jam-Wem Lee, Kuo-Ji Chen, Ming-Hsiang Song, Taiwan Semiconductor Manufacturing Company

A low-capacitance silicon-controlled rectifier for high speed I/O pad protection is implemented with TSMC 7 nm bulk FinFET technology. It can achieve much higher ESD robustness per capacitance with better dynamic on-resistance and faster turn-on speed for CDM protection as compared to the prior art.

1A.3 External Latch-up Risks and Prevention Solutions in Advanced Bulk FinFET Technology
Wei Liang, Robert Gauthier Jr., Souvick Mitra, Hien Lai, GLOBALFOUNDRIES

Internal latch-up (ILU) and external latch-up (ELU) are studied in advanced bulk FinFET technology. ELU risks of thin oxide (SG) and thick oxide (EG) devices are assessed and discussed. In this work we present different design techniques designers are enabled with to eliminate ELU risks in their designs.

Exhibitor Showcase: 10:00 AM-10:10 AM

Session 1B: 10:10 AM-12:15 PM
1B: Manufacturing I
Moderator: Rita Fung, Cisco

1B.1 Design of a Critical Application Air Ionizer for Semiconductor Manufacturing
Larry Levit, LBL Scientific; Gregory Larson, Alan McCall, Julian Montoya, Intel Corporation; Timothy Maroni, NRD LLC; Geoffrey Weil, Anodyne Research; Jeremy Willden, Constellation Labs LLC

A new alpha bar ionizer is described. It utilizes a sinusoidal voltage waveform with air flow to deliver ions up to 1 m. It produces discharge times [1] < 10 seconds with maximum offset voltage of < ± 5 V, typical. The bar uses < 0.9 lpm of air /cm of bar. Without chemical interactions, it is suitable for certification up to Class 1.

1B.2 CPM Test Limitation Study for AC, Pulsed AC, and High Frequency AC Ionizers vs. DC Based Ionizers
Joshua (YongHoon) Yoo, Ethan (YoungChul) Choi, Elly (SoYoung) Koo, Core Insight, Inc.

There are some technical limitations with current charge plate monitor (CPM) equipment for voltage switching type of ionizers such as AC, pulsed AC, and high frequency AC ionizers. Technical limitations are mainly related to the response speed of CPM. ANSI/ESD S20.20-2104 and IEC 61340-5-1 standards require offset value for ionizer balance testing. A CPM manufacturer provides average test data that doesn't match with offset value. Current CPM technology has limitations to indicate risk of various types of ionizers.

1B.3 A Low-Voltage Microwave Plasma Ionizer Without the ESD Risk Due to a High Voltage Source
Byoungjin Bae, Jingook Kim, Ulsan National Institute of Science and Technology

A low-voltage microwave plasma ionizer is proposed. The proposed ionizer eliminates the ESD risk on a target sensitive electronic device due to strong electric field induced by a high voltage source in the ionizer itself and has a good performance to neutralize a charged device.

Session 1A: 10:10 AM-12:15 PM

1A: Advanced CMOS EOS/ESD and Latch-up (Continued)

Moderator: Souvick Mitra, GlobalFoundries

1A.4 ESD Protection Diode with Guard Ring Layout Optimized for Latch-up Immunity Enhancement in FinFET Technology

Kai-Ping Huang, Po-Lin Peng, Li-Wei Chu, Yi-Feng Chang, Tzu-Heng Chang, Jam-Wem Lee, Kuo-Ji Chen, Ming-Hsiang Song, Taiwan Semiconductor Manufacturing Company

A novel ESD dual diode with stronger latch-up robustness has been proposed in FinFET technology. By inserting PW/NW straps, the proposed ESD diode can be built without changing DC-IV and ESD characteristics of conventional ESD diode. The experimental and simulation results demonstrate that the proposed structure has been successfully verified in FinFET CMOS platform.

1A.5 Low-Leakage NMOS Clamps with Gate-Assisted Bipolar Triggering

Michael Stockinger, NXP Semiconductors

NMOS clamps with gate-assisted bipolar triggering are introduced offering low-leakage, area-efficient ESD protection solutions in a 40 nm CMOS technology. Test chip results demonstrate > 6 kV PESD performance with direct pin discharge, as well as excellent HBM and CDM robustness.

Session 1B: 10:10 AM-12:15 PM

1B: Manufacturing I (Continued)

Moderator: Rita Fung, Cisco

1B.4 Characterization of ESD Shielding Bag with Capacitive Probe and IEC 61000-4-2 Generator

Toni Viheriäkoski, Cascade Metrology; Rita Fung, Richard Wong, Cisco Systems; Reinhold Gaertner, Friedrich zur Nieden, Infineon Technologies AG; Pasi Tamminen, EDR&Medeso Oy

ESD sensitive devices inside protective packaging may be exposed to high stress levels outside ESD protected area. ESD shielding bags are therefore tested with realistic stress levels by a system level ESD generator. The aim of this study is to estimate statistical uncertainty of ESD shielding measurements with different ESD generators and a capacitive probe.

1B.5 Evaluation of ESD Garment with Conductive Ribbon

Bernard Chin, Jeremy Ong, UTAC Headquarters Pte Ltd.; L.H. Koh, Everfeed Technology Pte. Ltd.

A new batch of ESD garments (smocks) was found to fail on compliance verification after 10 washes. An experiment was carried out to verify if smocks attached with conductive ribbon will have longer durability. This paper evaluates the durability of two types of smocks up to 110 and 420 washes.

Exhibitor Showcase: 1:25 PM-1:35 PM

Session 2A: 1:35 PM-2:50 PM

2A: EOS/ESD Failiure Analysis, Troubleshooting, and Case Studies I

Moderator: Ann Concannon, Texas Instruments, Inc.

2A.1 HV Latch-up at System Level ESD Current Injection

David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp.

A correlation between JEDEC standard qualification HV latch-up test and a phenomenon of a similar nature induced by injection from system-level ESD pulse current is studied through comparison and additional TLP pseudo latch-up regimes. The initial insight about required layout spacing rules to withstand the ESD pulse injection HV latch-up conditions is presented.

2A.2 Mechanism of Sequential Finger Triggering of Multi-Finger Floating-Base SCRs Due to Inherent Substrate Currents

Hasan Karaca, Clément Fleury, Dionyz Pogany, TU Wien; Steffen Holland, Hans-Martin Ritter, Guido Notermans, Nexperia Germany GmbH

Sequential finger triggering (SFT) associated with successive voltage drops near the holding voltage is observed in multi-finger floating-base SCRs on SOI. The SFT is observed only for long pulse rise times (10 ns). TCAD simulation explains that 3-150 ns time delay between finger triggering is due to lateral carrier diffusion-limited processes.

2A.3 Dual Injection Latch-up Phenomenon in HV Rail Based ESD Protection Networks

Slavica Malobabic, David Marreiro, Vladislav Vashchenko, Maxim Integrated Corp.

A dual injection latch-up phenomenon in rail based ESD protection network was studied using wafer level experiments. When floating the ESD rail, low side injection causes positive feedback with high side diode connected to the power supply. Comparison of dual-injection latch-up vs. conventional HV low side latch-up isolation is presented.

Exhibitor Showcase: 1:25 PM-1:35 PM

Session 2B: 1:35 PM-2:50 PM

2B: Full-Custom and Application Drive ESD Concepts

Moderator: Christian Russ, Infineon Technology

2B.1 Phase Change Disabling Circuit for the Poly Fuse During the ESD Event

Shao-Chang Huang, Li-Fan Chen, Chun-Chih Chen, Ting-You Lin, Kai-Chieh Hsu, Yeh-Ning Jou, Chih-Hsuan Lin, Yung-Chang Chen, Wei-Sung Chen, Jian-Hsing Lee, Vanguard International Semiconductor Corporation

Electrostatic discharge (ESD) can falsely program or erase the poly fuse cell even it has an ESD protection device. In this study, the phase change disabling circuit is successfully proposed and demonstrated that it can prevent the poly fuse from ESD damaging.

2B.2 Concurrent ESD and Surge Protection Clamps in RF Power Amplifier

Myunghwan Park, Jermyn Tseng, Tzung-yin Lee, David Ripley, Skyworks Solutions, Inc.

For cost reduction and device miniaturization efforts, the system-level surge suppressor is often being removed, which motivates developing concurrent HBM and surge protection clamps. Here, we characterize surge and HBM performance of the conventional clamps, and further propose a partial feedback combo clamp and ballasted RC-triggered clamp.

2B.3 A 3-Terminal HV-ESD Protection as Specialized Solution for EDn-MOSTs that Directly Link Two External Pads

Gijs de Raad, Da-Wei Lai, NXP Semiconductors

This paper describes ESD design around EDn-MOST devices that connect directly between two I/O pads. That ESD design involves carefully balancing the EDn-MOST drain voltage against its internal current density during ESD. A novel ESD device, the 3-port PNP, relaxes that balance and so increases design freedom.

Hands-on Session I 1:25 PM-2:50 PM Manufacturing Track

ESD TR53 - Compliance Verification of ESD Protective Equipment and Materials

Dale Parkin, Kevin Duncan, Seagate Technology

TR53 describes the measurement equipment and compliance verification procedures used to verify the performance of ESD protective equipment and materials. It is a main companion document used in conjunction with ANSI/ESD S20.20 to identify periodic performance changes and demonstrate compliance to your Organization's ESD Control Program Plan.

INCLUDED with symposium registration

Exhbitor Showcase 3:20 PM-3:30 PM

Session 3A: 3:30 PM-4:45 PM

3A: EOS/ESD Failiure Analysis, Troubleshooting, and Case Studies II

Moderator: Ann Concannon, Texas Instruments, Inc.

3A.1 3.3V ESD Clamp Structure Susceptibility Towards Pseudo LU in 22FDSOI

Anurag Mittal, Nitin Bansal, Invecas Technologies Pvt., Ltd.

An unexpected failure occurred during latch-up test of a 22FDSOI chip which had 3.3 V general purpose IOs implemented using 1.8v compliant devices. The high supply current flowing was not a real LU failure but due to triggering of RC clamp during negative current injection on nearby IOs. The pseudo latch-up is presented along with methods to ensure robustness of 3.3 V clamp design structures .

3A.2 ESD Design Considerations for Ultra-Low Power Crystal Oscillators in Automotive Products

Stefan Dannenberger, Oddgeir Fikstvedt, Danielle Griffith, Texas Instruments

Ultra-low power crystal oscillators are sensitive to resistive and capacitive loads at the input. That imposes challenges to the design of the oscillator and its electro-static discharge (ESD) protection circuit. In this paper, protection strategies for automotive productions are described while keeping an ultra-low power profile of the oscillator circuit.

3A.3 EOS Protection of the Low Voltage Gate Oxide Devices

Vladislav Vashchenko, Slavica Malobabic, Maxim Integrated Corp.

The problem of the electrical overstress protection of the CMOS devices with gate oxide operation voltage below 2V is solved by a small footprint active miniclamp circuit based on high threshold voltage reference and efficient pull-up driver. The experimental validation is demonstrating the tunable clamping voltage in the range 3.7-4.3V under leakage voltage <0.1nA. A more advanced design with additional CMOS thyristor circuit the clamping voltage <3.3V is presented too and validated by compact model circuit simulation.

Exhbitor Showcase 3:20 PM-3:30 PM

Session 3B: 3:30 PM-4:50 PM

3B: Manufacturing II

Moderator: Michelle Lam, IBM

3B.1 Customer EOS DPM Improvement Through Collaboration

Xi Chen, Intel (China) Ltd.

Through decades we had been working with PC ODMs to understand manufacture EOS issues to caused chip failure, which is always as top buckets of customer required failure analysis units for years. The paper is intent to show manufacture EOS case studies, improvements which people always like to know more.

3B.2 Circular Aperture Effects on Radiated Emissions of Electrostatic Discharge Events

Gregory Larson, Intel Corporation

Aperture effects on the radiated emissions of electrostatic discharge events is introduced with the aid of real time spectrum analysis to understand frequency domain considerations and a comparison of oscilloscope measurements of charge device model (CDM) induced events as measured with and without an aperture impeding free space propagation.

3B.3 Measurement of Electrostatic Discharge Through Human Bodies Contacting Metallic Objects Under HVAC Transmission Lines

Tiebing Lu, North China Electric Power University; Xiuying Li, Norendar International Ltd.

When the human body exposed to the electric field contacts other metallic objects, electrostatic discharge will be generated between fingers and objects. Some feeling experiments are carried out under 500 kV transmission lines. Discharge currents in 3 cases with different electric field are measured to evaluate the transient electric shock.

3B.4 - Poster - Ionized Electric Field due to HVDC Corona Discharge

Tiebing Lu, North China Electric Power University

Corona discharge can be generated along HVDC overhead transmission lines. Ionized electric field is increased due to the corona. Several methods to predict the electric field have been developed, which are demonstrated by experiments. For different complicated cases, some useful results are obtained to protect the environment.

Year-In-Review
Packaging Materials for Shipment of ESD Susceptible Items

David E. Swenson, Affinity Static Control Consulting

Wednesday 8:00 AM - 8:40 AM

The form, fit, and function of packaging materials used for protection of ESD susceptible items during storage and shipment continues to be an area of uncertainty in many ESD control programs. Determining what is needed for packaging is an important responsibility of the ESD Control Program Manager/Coordinator. The involved standards and test methods have either just completed the 5-year review process or will soon. Changes in the documents will be highlighted in this session. Of most interest is the continuing struggle to identify test methods for the low charging property and electric field shielding. The main standard ANSI/ESD S541–2018 was released with the understanding that it would be revised as soon as test methods became available to allow the industry to set specifications for charge generation and electric field shielding. Task teams have been working on the two subjects independently. The progress to date will be reviewed.

Exhbitor Showcase 8:55 AM-9:05 AM

Session 4A: 9:05 AM-11:10 AM
4A: System Level EOS/ESD/EMC I

Moderator: Robert Ashton, Minotaur Labs

4A.1 A Variable V_h Combined Power Clamp for System Level ESD/Surge Immunity Enhancement with Low Leakage

Koki Narita, Mototsugu Okushima, Renesas Electronics Corporation

A combined power clamp using both RC and static trigger circuits for system-level ESD/EFT/surge immunity enhancement is proposed. The proposed clamp can be achieved higher immunity against longer pulses like surge events compared to the conventional combined clamp without increasing its own leakage current using a variable holding voltage technique.

4A.2 Saturation Attenuator for TVS Devices

Eugene R. Worley, Silicon Crossing LLC

One very important issue with TVS clamps is their ability to limit the voltage below the level that can damage a state of the art SOC I/O which can fail at voltages as low as 3.5 V. Since lowering the shut resistance of the TVS to acceptable levels is very difficult another option is to introduce an attenuation resistor between the TVS and I/O. This paper will look at the saturation resistor as a means to protect low level I/Os.

4A.3 Development of EMC Analysis Technology Using Large-Scale Electromagnetic Field Analysis

Ryo Matsubara, Katsuo Inokuchi, Panasonic Corporation

RCJ Invited Paper

Recently, digital devices require LSI operated with higher frequency and lower voltage; therefore, countermeasures for EMC (electromagnetic compatibility) problem are becoming more difficult. Analytical EMC solving techniques, which contribute to design more directly and efficiently than the conventional approach, has been developed for electro magnetic radiation and electrostatic discharge.

Exhbitor Showcase 8:55 AM-9:05 AM

Session 4B: 9:05 AM-11:10 AM
4B: Manufacturing III

Moderator: Dale Parkin, Seagate Technology

4B.1 Capacitive Discharge to Ground of a Flat Metal Disk with a Pin Contact

Icko Eric Timothy Iben, IBM Co.

Capacitance, C, of and voltage, V, on a flat disk is calculated versus separation d from a ground plane. At large d, C and V are constants. At low d, C diverges as 1/d and V goes to 0 with d, eliminating ESD. Adding a contact pin significantly increases ESD risk.

4B.2 Discharge Current Analysis with Charged Connector Pins

Pasi Tamminen, EDR@Medeso; Rita Fung, Rick Wong, Cisco System, Inc.

Electrical connectors can get static charges during handling and discharge on a printed circuit board when assembled. The rise time and shape of the discharge current waveform is studied with simulation and measurement methods. Results show that the ESD current rise time can be less than 10 ps.

4B.3 Are ESD Chairs Good Enough to be Used as Primary Means of Personnel Grounding?

Reinhold Gärtner, Magdalena Hilkersberger, Infineon Technologies AG; Wolfgang Stadler, Josef Niemesheim, Intel Deutschland GmbH; Jürgen Speicher, Wolfgang Warmbier GmbH & Co. KG

Personnel handling ESD sensitive items in seated position are supposed to be grounded via a wrist strap. The paper describes measurement techniques to assess whether grounding personnel via ESD flooring and a chair is feasible. Different techniques to measure the body voltage generation and the influence of chair casters are discussed.

Session 4A: 9:05 AM-11:10 AM
4A: System Level EOS/ESD/EMC I (Continued)
Moderator: Robert Ashton, Minotaur Labs

4A.4 HMM Failure Level Variations Revisited
Marcel Dekker, MASER Engineering; Theo Smedes, NXP Semiconductors; Guido Notermans, Nexperia Germany GmbH; Robert Ashton, Minotaur Labs

EOS/ESD Association, Inc. working group 5.6 tries to establish a standard method, human metal model, to evaluate stand-alone devices with a system level pulse. This paper describes three experiments that address possible causes for variations in test results when comparing different guns or different labs. The most important contributors and possible improvements are identified.

4A.5 ESD_{21}, an Approach to Characterize Behavior of Multiport ICs Under ESD Stress
Omid Hoseini Izadi, David Pommerenke, Missouri University of Science and Technology; Kathy Muhonen, Nate Peachey, Qorvo, Inc.

ESD characterization of an RF switch was investigated. Resulting analysis matched the configuration of the switch. The ESD protection was observed to turn on at the max rating of the IC. This characterization is synonymous to large signal analysis showing the device under test conducting during large voltage transients.

Session 4B: 9:05 AM-11:10 AM
4B: Manufacturing III (Continued)
Moderator: Dale Parkin, Seagate Technology

4B.4 Determining the Proper Methods of Measuring a Conveyor Belt's Resistance to Ground
Donn G. Bellmore, Advanced ESD Services +; Richard Strube, Universal Instruments Corporation

Recently, several discussions have risen regarding what is the proper methods of measuring the resistance of conveyor belts to ground. This study looks at using standard worksurface measurement methods to characterize resistance to ground and the resistance to ground that might be affected by devices or assemblies.

4B.5 Dummy Versus Live ESD Sensitive Devices Charge Analysis for Automated Handling Equipment ESD Qualification
Jeremy Ong, Bernard Chin, UTAC Headquarters Pte Ltd.; L.H. Koh, Everfeed Technology Pte. Ltd.

Dummy units are commonly used for automated handling equipment (AHE) ESD qualification prior to releasing for production, due to resource limitations. Charge analysis for one hour vs. 72 hours baking time for ESD sensitive devices (ESDS) were studied. This paper proposes live ESDS for AHE ESD qualification.

1:40 PM – 1:50 PM Welcome to the IoT Workshop

Harald Gossner, Intel Deutschland GmbH

Today's electronic industry is challenged by the needs of ubiquitous Internet of Things penetrating into all realms of society, business and personal life. The basic functional building blocks of IoT devices are sensing, computing and connecting. There is a plethora of IC solutions for each of these features available and their performance is continuously growing. The driving factors for new applications are flexible integration of multiple functions like sensors, microcontrollers or wireless modem devices and the use of highest performance ICs, but at low cost due to the economical scaling effect of high volume products. To fully exploit this for IoT applications, a single IC solution should be scaled into many applications ranging, for example, from industrial to consumer. However, there is a limitation; IoT modules need to comply with very different reliability and robustness requirements depending on the application and the environment. Since the reusing of IC hardware for diverse applications in the fragmented IoT market is a critical factor for market success, adequate design solutions and development strategies for robustness as well as testing and qualification standards are crucial. This workshop brings together experts and industry leaders with strong engagement in IoT who are concerned about the robustness of IoT devices. As this is the first of a kind workshop the focus is on sharing of requirements of various application fields and discussion of the need of new approaches and standards beyond what is already existing.

Session A 1:50 PM – 4:55 PM

A1: Invited Talk
1:50 PM-2:30 PM

A2: Invited Talk
2:30 PM-3:10 PM

A3: Invited Talk
3:55 PM-4:15 PM

A4: Invited Talk
4:15 PM-4:55 PM

INCLUDED with
symposium registration

Hands-on Session II 1:40 PM-3:40 PM Manufacturing Track

II.A Grounding Measurements
1:40 PM-1:50 PM
John Kinnear, IBM

Establishing the grounding scheme is the foundation for an ESD control program. While several options are available, it is important to know how to make the measurements. How to measure each of the options will be discussed.

II.B Assessing the Risk of Insulators and Isolated Conductors
1:35 PM-1:45 PM
Reinhold Gärtner, Infineon Technologies AG; Wolfgang Stadler, Intel Deutschland GmbH

Charged insulators and isolated conductors are sources of electrostatic fields, resulting in inductive charging of ESD sensitive (ESDS) items, which can lead to failures if the ESDS is contacted by a conductive object. We present and compare different measurement approaches to assess the risk of charged insulators and isolated conductors.

II.A, II.B Demo Session
2:00 PM-2:40 PM

II.C ESD Field Meter Pitfalls and Voltage Suppression Demonstrations
2:40 PM-2:50 PM
Ted Dangelmayer, Dangelmayer Associates

The objective of this demonstration is to clarify confusion related to voltage suppression and the pitfalls related to making valid field meter measurements at workstations. Slides will illustrate the fundamentals and field meter measurements will be display graphically as they occur. This demonstration will be similar to the video on the ESDA website.

II.D Gloves
2:50 PM-3:00 PM
Troy Anthony, ETS
Gloves are routinely used in electronics manufacturing to prevent contamination of printed circuit board and other electronics. However, gloves can also present an ESD risk to product. This hands on session will give participants the opportunity to perform glove/finger cot measurements using established test methods in accordance with ANSI/ESD SP15.1.

II.C, II.D Demo Session
3:00 PM-3:40 PM

INCLUDED with symposium registration

Exhibitor Showcase 1:40 PM-1:50 PM

Session 5A: 1:40 PM-3:05 PM
5A: System Level EOS/ESD/EMC II
Moderator: Ben Orr, Intel

5A.1 Application Example of a Novel Methodology to Generate IC Models for System ESD and Electrical Stress Simulation out of the Design Data
Michael Ammer, Infineon Technologies AG, University of the Federal Armed Forces Munich; Andreas Rupp, Yiqun Cao, Infineon Technologies AG; Martin Sauter, Linus Maurer, University of the Federal Armed Forces Munich

Generating IC models for system ESD simulations out of measurements is quite cumbersome. For products with custom made ESD protection concepts one cannot use a model library for I/O standard cells. This work shows an application example of a novel methodology to generate IC ESD models out of design data.

5A.2 TVS Devices Transient Behavior Modeling Framework and Application to SEED
Li Shen, Shubhankar Marathe, Javad Meiguni, Guangxiao Luo, Jianchi Zhou, David Pommerenke, Missouri University of Science and Technology

The transient behavior for four different types of TVS (non-snapback, snapback, spark gap, varistor) is modeled using the same modeling framework. Using a 10 ns VF-TLP, the quasi-static I-V curve and the transient turn on are captured and modeled in ADS. The models are applied in a SEED simulation to investigate the strengths and weaknesses of the modeling frame.

5A.3 Characterizing and Modeling Common Mode Inductors at High Current Levels for System ESD Simulations
Michael Ammer, Infineon Technologies AG, University of the Federal Armed Forces Munich; Andreas Rupp, Infineon Technologies AG; Martin Sauter, Linus Maurer, University of the Federal Armed Forces Munich

Common mode chokes are frequently used in differential communication buses for noise filtering. It is expected that these inductors can damp incoming ESD pulses significantly and partially protect the communication ICs. In fact they are driven heavily into saturation during ESD events and cannot help to protect the integrated circuit.

Session 6A: 3:30 PM-4:45 PM
6A: Numerical Modeling and Electronic Design Automation I
Moderator: Nitesh Trivedi, Intel

6A.1 Impact of Lowly Doped Regions on Transient Overshoot Voltage During vf-TLP Pulses for Bipolar Devices
Steffen Holland, Guido Notermans, Hans-Martin Ritter, Nexperia Germany GmbH

The effect of the lowly doped region on the transient overshoot voltage of a junction diode, a bipolar transistor, and a SCR is investigated with vf-TLP measurements and calibrated TCAD simulations. The effect of the conductivity modulation is stronger for a BJT and SCR than for a forward biased diode.

6A.2 ESD Protection Impact and Modelling of Bias-Dependent Series Resistance in Diodes
Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar, Analog Devices, Inc.

An investigation of different forward-bias and reverse-bias on-resistance in diodes is presented. The impact of this often neglected effect on ESD protection is demonstrated. A macro-model of diode has been developed to count the bias dependent resistance and been used in circuit level ESD simulation in a SPICE-type simulator.

6A.3 A Comprehensive Physical Model for PNP Based ESD Protection Devices in SOI Technology
Xiaoliang Han, Shuang Zhao, NXP Semiconductors

This paper presents a comprehensive physical model for PNP based ESD protection device. The model includes all major physical effects during ESD device operation, which enables the model to capture the DC, AC and dynamic effects like overshoot, reverse recovery and self-heating. The transition of the device operating regions from high resistance to snapback region, from device turn-on to second breakdown are processed smoothly with the help of numerical functions, therefore eliminating convergence issues during simulation. The simulation results have been verified using DC, TLP, vf-TLP measurements. Due to its highly physical nature, the scalability of the model is also ensured.

Tutorial Session I: 3:55 PM -5:05 PM

Manufacturing Track

I.A Product Qualification

Dale Parkin, Seagate Technology

This tutorial will cover the importance of the product qualification process of products / materials as outlined in S20.20 for use in the protection of ESDS items. This will include an example chart of product, equipment matrix and standard test methods that could be used by the end user.

I.B Product Qualification vs Compliance Verification

Dale Parkin, Seagate Technology

Now you have a product qualified and you have it in use what is next. What is a compliance verification plan? This tutorial will cover the differences between qualification and compliance verification.

INCLUDED with symposium registration

Year-In-Review
Relationships and Interactions Between ESD and EMC

Alan Righter, Analog Devices, Inc.

Thursday 8:00 AM - 8:40 AM

It is known that ESD events generate EMI, which can cause damage in devices beyond the ESD event itself. There is much work in process to better understand the relationship between different ESD tests and EMI/EMC, as well as how EMC-centric tests such as transient and surge extend the realm of understanding effects on ESD devices and systems (boards). One example is the IEC 61000-4-2 test, where evaluation has been going on for some time comparing guns and pulsers and their different results on ICs and systems, and reviewing how the resulting waveform is described and characterized. This Year-in-Review will focus on these main topics through reviews of the recent works in journals and ESD/EMC related conferences, and also including standards updates, and how they are adding to the understanding of the relationship between ESD and EMC.

Session 7A: 8:55 PM-9:55 PM

7A: Modeling II

Moderator: Nitesh Trivedi, Intel

7A.1 Towards a TCAD Model for NMOS Loads in 28FD-SOI Under TLP & (vf)-TLP Transient Condition

Siddhartha Dhar, Johan Bourgeat, Chittoor Parthasarathy, STMicroelectronics

This work analyzes the TLP and (vf)-TLP characteristics of NMOS loads in FDSOI technology. A TCAD model based on electro-thermal simulations is developed, that captures the measured characteristics in single NMOS drivers in ON/OFF state conditions, and validated against stacked configurations. A universal failure criterion based on temperature is demonstrated.

7A.2 Simulation Driven ESD Current Density Check

Ulrich Glaser, Radu Stoica, Radu Ionescu, Marcel Preda, Infineon Technologies

The presented current density check tool identifies the ESD current paths itself and checks the interconnection layers for realistic ESD currents depending on all available ESD paths and the applied ESD stress. It achieves highest flexibility and coverage with practically no false errors and without any need for marking.

Discussion Group Session: 8:55 AM-10:10 AM

Manufacturing Track

DG.A: The ESD Control Program, AH-HA! I Didn't Think About That!

Matt Strickland, L3 Technologies

Proper implementation of the S20.20 is crucial to the effectiveness of the ESD Control Program. This discussion group is intended to bring the seasoned ESD Control Program Manager and those new to the role to discuss the requirements of the S20.20 and how a company implements them.

DG.B: Process Assessment

Wolfgang Stadler, Intel Deutschland GmbH

With decreasing ESD robustness of ESD sensitive items, appropriate ESD control measures are becoming increasingly important. Detailed ESD process assessments is required to identify possible ESD risks in processes and define charging and/or discharging control measures. We will discuss typical problems and risk scenarios and review methodologies and strategies for a successful and efficient process assessment.

DG.C: ESD Packaging / Reuse of the Packaging

Dale Parkin, Seagate Technology; Dave Swenson, Affinity Static Control Consulting

Proper ESD packaging is an essential element of a robust ESD control program. Depending on your application and usage, ESD packaging materials might be reused until they lose their protection properties. However, what is considered appropriate reuse of packaging materials without adding risk to your ESD control program? How do you select your ESD packages to protect your devices and products? Let's bring your questions and experience to share in this discussion group.

INCLUDED with symposium registration

Session 8A: 10:20 AM-12:10 PM

8A: Testing

Moderator: Theo Smedes, NXP

8A.1 Towards Standardization of Low Impedance Contact CDM

Nathan Jack, Brett Carn, Josh Morris, Intel Corporation

The 16.6 ohm implementation of contact CDM (LICCDM) recently published in ANSI/ESD SP5.3.3 is shown to produce waveforms of similar shape, Ifail, and Ipeak vs. Ceff dependency as JS-002. The non-monotonicity of ANSI/ESDA/JEDEC JS-002 at low voltages is overcome using LICCDM. A path to joint standardization with air discharge testing is proposed.

8A.2 Study of CDM Measurement for Bare Die and Wafers

Teruo Suzuki, Kazuya Okubo, Hiroki Taniguchi, Socionext, Inc.; Masanori Sawada, Hiroyuki Okumura, Kazuo Shinke, Hanwa Electronic Ind. Co; Osamu Mihama, Mihama Corp.

ESD failure problems in back-end processing are resolvable, but measuring CDM robustness in the bare-chip/wafer state would provide early information about whether the problem lies with ESD protection circuits or electrostatic control. Our new ANSI/ESDA/JEDEC JS-002-compliant wafer CDM tester correlates with vf-TLP & allows bare-chip/wafer measurement, to achieve the acceptable accuracy.

8A.3 Energy of CDM Failure of ICs on Package-, Wafer-, and Board-Level

Lena Zeitlhoefler, Friedrich zur Nieden, Kai Esmark, Gernot Langguth, Infineon Technologies AG

Energy-based failure is analyzed for CDM-like discharges. The stress of an ESD element can be quantified and simulated if the background capacitance of an IC domain is known. Differences between package, wafer, and board level are evaluated using the capacitively coupled TLP (CCTLP). CCTLP can reproduce a charged board event if the on-board domain capacitance is in the same range as on wafer level.

8A.4 Low-Impedance Contact CDM – Evaluation and Modeling

Marko Simicic, Wei-Min Wu, Shih-Hung Chen, Dimitri Linten, imec; Nathan Jack, Intel Corp.; Shinichi Tamura, Yohei Shimada, Masanori Sawada, Hanwa Electronic Ind. Co., Ltd.

Standard charged device model (CDM) ESD simulators used today cannot be used at wafer level and suffer from high zap-to-zap peak current variability at low voltages. The low-impedance contact CDM provides a solution to these problems. In this paper we evaluate its performance and propose a model for the setup.

Tutorial Session II: 10:35 AM-12:20 PM

Manufacturing Track

II.A ESD TR2020 Handbook

John Kinnear, IBM

ANSI/ESD S20.20 and ESD TR53 are used world wide for establishing an ESD control process. The third document, ESD TR20.20 is a third document that helps select what elements to use. This document provides useful information on options. How to use this document and some examples will be presented.

II.B Measurement Errors and Uncertainties in High Resistance Measurements

Toni Viheriaekoski, Cascade Metrology, Inc.

Compliance verification and qualification measurements of ESD control items are often made with a high resistance meter. A friendly user interface may encourage users to make the challenging low current measurements without the consideration of systematic, random and gross errors. Measurement uncertainties such as a loading effect, electrification, contact resistance and leakage currents can be evaluated in practice. The most common errors and uncertainties will be discussed.

II.C Importance of Equipment Verification

Troy Anthony, ETS

Resistance measurements are routinely made to determine if ESD packaging, workstation protection, or raw material is acceptable. What's the cost of erroneous readings? Bad data can result in work stoppages, material rejection, and safety issues. This session considers the importance of equipment verification and standards that include verification methods.

INCLUDED with symposium registration

Session A: 5:45 PM - 7:00 PM

A.1 Sub-150V CDM Testing

Nathan Jack, Intel Corporation; Alan Righter, Analog Devices, Inc.

What would be sub 150V (or lower target) CDM testing process?

What is the difference/comparison between FiCDM w or w/o nitrogen chamber, CCTLP etc.?

Can one achieve optimum spark gap for low CDM level?

A.2 Machine Learning and More: Advancement in Simulation and EDA Methods for ESD Verification

Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Norman Chang, ANSYS; Robert Gauthier, GlobalFoundries; Michael Khazhinsky, Silicon Labs

There exist multiple commercial EDA tools for ESD design verification. There are relatively few tools to support Design for ESD Reliability, with the exception of simple rule checkers that are used at the early floor-planning stage. The panelists and audience will review the capabilities and limitations of today's EDA tools and build a consensus as to what is still needed, i.e., the ESD community's wish list for EDA researchers and tool vendors. For the balance of the workshop, we will explore how to realize that vision. We will consider whether machine learning methods can help with the modeling of complex systems, i.e., systems with multiple scale lengths and complex electromagnetic and thermal behaviors. We'll debate whether an ESD design methodology can be learned from past designs. And, can "big data" analytics be applied to foundry ESD data to generate layouts that will maximize ESD performance? Come share your experience and ideas, as we work together to advance the state of the art in ESD EDA.

A.3 3rd Party IP and Foundry Deliveries – Problem Solved for Seamless, ESD Safe IC Top Level Integration?

Harald Gossner, Intel Deutschland GmbH

The workshop addresses the results and technical reports created by ESDA WG22 on IP and foundry ESD parameters. Two documents have been released: TR22.0-01-14 describes the essential requirements on ESD-related technology data from foundry vendors needed by design customers. It presents the generic set of ESD parameters with description of test structures and test procedures. TR22.0-02-18 highlights the ESD-related issues relevant to intellectual property (IP) selection, integration, on-chip usage and verification. It also addresses consolidated best practices between IP providers and IP users. Join the workshop to discuss the need of standardization and how the documents can be widely applied or even enforced. We encourage attendees to read both documents which are available at www.esda.org.

A.4 EOS Best Practices

Vladimir Kraz, OnFilter, Inc.

"Electrical overstress is the number one cause of damage to IC components" according to Intel's Manufacturing Enabling Guide, May 2016.

•How does your company deal with EOS?

•Do you have EOS program?

•Do you have any data on EOS exposure in your production?

•How do you track EOS damage in the field?

•What is your overall plan for EOS?

Session B: 5:20 PM - 6:35 PM

B.1 Adapting to the Demands of Automotive – From an ESD Perspective

Ann Concannon, Texas Instruments, Inc.

The semiconductor content in automotive is increasing, expected to double in value over the next 8 years. This will be due to the electric drive drain (high voltage products), sensors (for example LIDAR) for safety and automation, and infotainment to name a few growth vectors. We will explore some of the challenges meeting ESD requirements in these applications – from the challenge of introducing new technologies/products, to new EMC requirements & harsh environments/ESD tradeoff on high voltage products.

B.2 IEC Testing

Nate Peachey, Qorvo Inc.; Andrew Spray, David Klein, Synaptics, Inc.

- Are customers asking for IEC testing of discrete ESD devices, modules or benchmark circuits?
- If customers are asking for this kind of testing, are the required levels consistent between customers?
- Are the requirements and their preferred test procedures based on observations of final system stress and behavior?
- If the customer requires module level testing, how much insight are they giving into how the module will be placed, physically and electrically, in the final system?
- Is customer demand of HMM growing or is it still research level activity?
- Are we doing company specific testing for IEC?
- Do we have a standard for system level ESD characterization?

B.3 ESD Myths and Misconceptions

Dana Beatty, Xfabion; Matt Jane, Tesla; Andy Nold, Eagle Test Systems, a Teradyne Company

This workshop aims to dispel common myths and misconceptions regarding ESD mitigation in the workplace through hands on demonstrations and group discussion. Multiple topics such as ESD “Touch-off pads” and drag chains will be addressed. Each topic will be followed by real world testing using industry standard devices to ultimately debunk each topic.

B.4 IoT devices for consumer, automotive and industrial – where is special need for IP, EDA tools and technology to support ESD and reliability?

Harald Gossner, Intel Deutschland GmbH

While IoT is a widely known buzzword, the challenges for robust design actually apply for most of future semiconductor. In the past, typically the equation worked: ‘higher robustness comes with lower speed’ and ‘high speed devices get accepted with low robustness targets’. This is not applicable to advanced IoT use cases like camera interfaces for autonomous driving or sensor fusing for robotics. The real time transmission and computing of a huge data volume is mandatory for the functionality. At the same time the systems are highly safety critical. Availability and correct functionality must be guaranteed under extreme conditions. The discussion group will address the question what is needed for IP, SOC and module design to achieve this in a dynamic and cost sensitive market environment.

Exhibit Hall

You will find a broad spectrum of products and services for static protection, control, testing, and analysis, as well as prominent trade publications, all in one location for your convenience. Exhibits are open to the public.

Exhibit Hours

Monday, September 16
Welcome Reception
6:00 p.m. - 9:00 p.m.

Tuesday, September 17
9:30 a.m. - 5:30 p.m.

Wednesday, September 18
8:30 a.m. - 1:30 p.m.

Ten minute showcase presentations from exhibitors are scheduled at the beginning of select technical sessions.

A complimentary coffee bar is available in the exhibit hall for all visitors.

Tuesday lunch service will be available in the exhibit hall for anyone wishing to purchase lunch while visiting the exhibits.

Exhibitor	Booth number
ACL Staticide, Inc.	302
Advanced Test Equipment Rentals	416
ANSYS Inc.	106
Barth Electronics, Inc	502
Botron Company, Inc.	109
Clean Control Tech Corp	507
Conductive Containers, Inc.	203
Core Insight, Inc.	112
Dangelmayer Associates, LLC	511
Desco Industries, Inc.	309
Dou Yee Enterprises Pte. Ltd.	114
Electro-Tech Systems, Inc.	313
ESDEMC Technology, LLC	503
Estatec, LLC	314
Estion Technologies GmbH	108
Gibo/Kodama Chairs	403
Grund Technical Solutions, Inc.	513
HANWA Electronic Ind. Co., Ltd.	200
Higain Limited T/A Phasix ESD	301
HPPI GmbH	515
In Compliance Magazine	414
Lubrizol Engineered Polymers	202
Magwel	110
Megalin Source International Co., Ltd.	116
Mentor Graphics Corporation	300
MG Chemicals	400
Modern Dispersions, Inc	317
NOID Corporation	402
NRD, LLC	413
Premix Oy	401
Prostat Corporation	113
Shenzhen Btree Industrial Co., Ltd.	315
Silicon Frontline Technology, Inc.	100
Simco-Ion	213
Statico	215
StaticStop, a division of SelecTech, Inc.	305
Synopsis, Inc.	104
Tech Wear, Inc	103
Thermo Fisher Scientific	209
Transforming Technologies	409
Trek, An Advanced Energy Company, and now home to Monroe Electronics Electrostatic & ESD Product Line	303

EOS/ESD Association, Inc.

Officers

President
Ginger Hansel, *Dangelmayer Associates, LLC, Austin, TX*

Senior Vice President
Alan Righter, *Analog Devices, Inc., San Jose, CA*

Vice President
Harald Gossner, *Intel Deutschland GmbH, Neubiberg, GERMANY*

Treasurer
John Kinnear Jr., *IBM Corporation, Poughkeepsie, NY*

Secretary
Nathaniel Peachey, *Qorvo, Inc., Greensboro, NC*

Past President
Gianluca Boselli, *Texas Instruments, Inc., Dallas, TX*

Headquarters Operations

Lisa Pimpinella, Executive Director
Christina Earl, Standards Senior Program Manager
Nicholas Pimpinella, Administrator, Programs
Brennan Pimpinella, Administrator, Marketing
Tiffany Hutchinson, Administrative Assistant
Elena Quinones, Administrative Assistant

Steering Committee

General Chair
Guido Notermans, Nexperia, Hamburg, GERMANY
Vice General Chair
Lorenzo Cerati, STMicroelectronics, Agrate Brianza, ITALY
Tutorial Program Chair
Wolfgang Stadler, Intel Deutschland GmbH, Neubiberg, GERMANY
Technical Program Chair
Wolfgang Stadler, Intel Deutschland GmbH, Neubiberg, GERMANY
Workshops Chair
Souvick Mitra, GLOBALFOUNDRIES, Inc., Essex Junction, VT
Arrangements Chair
Cheryl Checketts, Mesa, AZ
Registration Chair
Raivo Leeto, Sandia National Laboratories, Albuquerque, NM
Audio/Visual Co-Chair
Ann Concannon, Texas Instruments, Inc., Santa Clara, CA
Audio/Visual Co-Chair
Heinrich Wolf, Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT, Munich, Germany
Tutorial Audio/Visual
Matt Strickland, L3 Technologies, San Diego, CA
Technical Liaison
Michael Khazhinsky, Silicon Laboratories, Inc., Austin,TX
Information
David E. Swenson, Affinity Static Control Consulting, LLC, Austin, TX
Past General Chair
James W. Miller, NXP Semiconductors, Austin, TX
EOS/ESD Association, Inc. Vice President
Harald Gossner, Intel Deutschland GmbH, Neubiberg, GERMANY
Publications & Marketing
HQ Operations, EOS/ESD Association, Inc., Rome, NY

Board of Directors

Gianluca Boselli, *Texas Instruments, Inc., Dallas, TX*
Brett Carn, *Intel, Hillsboro, OR*
Lorenzo Cerati, *STMicroelectronics, Agrate Brianza, ITALY*
Cheryl Checketts, *Estatec, Mesa, AZ*
Ann Concannon, Texas Instruments, Inc., Santa Clara,CA
Charvaka Duvvury, *ESD Consulting, LLC*, Plano ,TX
Reinhold Gaertner, *Infineon Technologies, Neubiberg, GERMANY*
Robert Gauthier, *GLOBALFOUNDRIES, Essex Junction, VT*
Harald Gossner, *Intel Deutschland GmbH, Neubiberg, GERMANY*
Ginger Hansel, *Dangelmayer Associates, LLC, Austin, TX*
Matthew Hogan, *Mentor, A Siemens Business, Wilsonville, OR*
Michael Khazhinsky, *Silicon Laboratories, Inc., Austin, TX*
John Kinnear Jr., *IBM Corporation, Poughkeepsie, NY*
Junjun Li, *IBM Corporation, Poughkeepsie, NY*
Tom Meuse, Thermo Fisher Scientific, Tewksbury, MA
Nathaniel Peachey, *Qorvo, Inc., Greensboro, NC*
Lisa Pimpinella, *EOS/ESD Association, Inc., Rome, NY*
Alan Righter, *Analog Devices, Inc., San Jose, CA*
Mirko Scholz, *imec, Leuven, BELGIUM*
Wolfgang Stadler, *Intel Deutschland GmbH, Neubiberg, GERMANY*
Matt Strickland, L3Technologies, San Diego, CA
David E. Swenson, *Affinity Static Control Consulting, LLC. Austin, TX*
Terry Welsher, Dangelmayer Associates, LLC, Suwanee, GA

Technical Program Committee

Technical Program Chair

Wolfgang Stadler, Intel Deutschland GmbH

Michael Ammer	Infineon
Robert Ashton	Minotaur Labs
Taylor Bahr	ORBIS Corporation
Dana Beatty	Skolnik Technical
Fabrice Blanc	ARM
Mary Kay Botkins	ACL Staticide
Thomas Chang	GLOBALFOUNDRIES
Shih-Hung Chen	imec
Zhong Chen	University of Arkansas
Bernard Chin	Firefly Solutions
Mart Coenen	EMCMCC
Ann Concannon	Texas Instruments
Marcel Dekker	Maser Engineering BV
Leonardo Di Biccari	STMicroelectronics
Jeff Dunnihoo	Pragma Design
Charvaka Duvvury	ESD Consulting, LLC
Farzan Farbiz	
Rita Fung	Cisco
Robert Gauthier	GLOBALFOUNDRIES
Eleonora Gevinti	STMicroelectronics
Marcos Hernandez	Thermo Fisher Scientific
Steffen Holland	Nexperia
Nathan Jack	Intel
Matt Jane	Tesla
Marty Johnson	Texas Instruments
David Johnsson	HPPI
Michael Khazhinsky	Silicon Labs
Michelle Lam	IBM
Gernot Langguth	Infineon
Junjun Li	IBM
Jian Liu	Qorvo
Slavica Malobabic	Maxim Integrated
Tim Maloney	Center for Analytic Insights
Markus Mergens	QPX
Tom Meuse	Thermo Fisher Scientific
Souvick Mitra	GLOBALFOUNDRIES
Andy Nold	Eagle Test Systems/Teradyne
Guido Notermans	Nexperia
Mototsugu Okushima	Renesas
Benjamin Orr	Intel
Greg O'Sullivan	Micron
Dale Parkin	Seagate
Milova Paul	Indian Institute of Science (IISc) Bangalore
Nate Peachey	Qorvo
Paul Phillips	Phasix ESD
David Pommerenke	Missouri Science & Technology
Sithanandam Radhakrishnan	Samsung
Alan Righter	Analog Devices
Christian Russ	Infineon
Javier Salcedo	Analog Devices
Mayank Shrivastava	Indian Institute of Science (IISc) Bangalore
Jay Skolnik	Skolnik Technical
Theo Smedes	NXP Semiconductors
Matt Strickland	L-3 Technologies
Teruo Suzuki	SocioNext
Nitesh Trivedi	Intel
Anthony Troy	Electro-Tech Systems
Toni Viheriäkoski	Cascade Metrology
Pengyu Wei	Apple
Henry Wolf	Fraunhofer
Gene Worley	Qualcomm
Joshua Yoo	Core Insight
Craig Zander	Transforming Technologies
Carol Rouying Zhan	ON Semiconductor
Paul Zhou	Analog Devices

Accomodations

EOS/ESD Symposium and Exhibits, September 15-20, 2019
Riverside Convention Center, Riverside, CA, USA

Room Rates

Marriot Riverside at the Convention Center, Riverside, CA (Room Rate $140/night)
3400 Market Street
Riverside, CA 92501
Reservations Link:
https://www.marriott.com/event-reservations/reservation-link.mi?id=1558470520313&key=GRP&app=resvlink

Call-In: 1-800-228-9290
Rate: $140+tax
Book By: August 9th (Based on Availability)

The Mission Inn Hotel & Spa, Riverside, CA (Room Rate $140/night)
3649 Mission Inn Avenue
Riverside, CA 9250
Reservations Link:
https://reservations.travelclick.com/74028?groupID=1592134&hotelID=74028

Call-In: 1-800-843-7755
Rate: $140+tax (Resort Fee Waived)
Book By: August 9th (Based on Availability)

UNAUTHORIZED HOUSING

Housing block "pirates" now routinely "poach" event attendees and exhibitors!
Pirating companies gather group's contact information from published or online directories. They call attendees leaving the impression that they are an "official" housing representative. They will also frequently cite an imminent sell-out of the block while urging you to secure housing immediately. Another tactic is to offer a room rate that is significantly less than the official rate. Offered rooms may be substandard or at other properties. Please do not respond to these solicitations or book your rooms with any housing organizations that "claim" to represent EOS/ESD Association, Inc. Booking via the hotel link or calling the number we provided are the only safe and reliable methods for booking your hotel reservations.

Reservations When reserving your room, in all instances, identify yourself as a participant of the EOS/ESD Symposium.

Cancellation of reservation must be made at least seven days prior to arrival date or you will be charged one nights room/tax.

Registration - page 1

EOS/ESD Symposium and Exhibits, September 15-20, 2019
Riverside Convention Center, Riverside, CA, USA

Register Online!
http://www.cvent.com/d/86qf9q

Please fill out all sections (1 thru 4) of this form. Sections 3 and 4 are on next page.

1 Please Print or Type (Your name and company will appear on badge and/or certificate exactly as written below.)

Mr./Mrs./Ms.: _____ First Name: _____ Last Name: _____

Company Name: _____

Job Title: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code: _____

Address is (please circle the one that applies) Home or Company

Phone: _____ E-mail: _____

2 Tutorial Registration

Check each session attending, one session per time slot.

SUNDAY, SEPTEMBER 15 & MONDAY, SEPTEMBER 16

☐ FC340: 8:00 a.m. - 5:00 p.m ESD Program Development and Assessment (ANSI/ESD S20.20) (PrM)

SUNDAY, SEPTEMBER 15

☐ FC100: 8:30 a.m. - 5:00 p.m. ESD Basics for the Program Manager (PrM)
☐ FC390: 8:00 a.m. - 5:00 p.m. Basics of ESD Process Assessment
☐ DD200: 8:30 a.m. - 12:00 p.m. Charged Device Model Phenomena, Design, and Modeling (DD)
☐ DD103: 8:30 a.m. - 12:00 p.m. An Overview of Integrated Circuit ESD: The ESD Threat, Testing, Design Concepts and Debugging
☐ DD/FC240: 8:30 a.m. - 12:00 p.m. System Level ESD/EMI: Principles, Design Troubleshooting, & Demonstrations **NEW**
☐ FC140: 8:30 a.m. - 12:00 p.m. System Level for the Program Manager (PrM)
☐ DD201: 1:00 p.m. - 4:30 p.m. ESD Protection and I/O Design
☐ DD204: 1:00 p.m. - 4:30 p.m. ESD Design in HV Technologies
☐ DD/FC130: 1:00 p.m. - 4:30 p.m. System Level ESD/EMI: Testing to IEC and Other Standards (DD)
☐ FC220: 1:00 p.m. - 4:30 p.m. Device Technology and Failure Analysis for the Program Manager(PrM)

MONDAY, SEPTEMBER 16

☐ FC101: 8:30 a.m. - 4:30 p.m. How To's of In-Plant ESD Auditing and Evaluation Measurements (PrM)
☐ DD110: 8:00 a.m. - 12:00 p.m. ESD From Basics to Advanced Protection Design (DD)
☐ DD231: 8:30 a.m. - 12:00 p.m. ESD System Level: Physics, Testing, Debugging of Soft and Hard Failures
☐ DD300: 8:30 a.m. - 12:00 p.m. Circuit-Level Modeling and Simulation of On-Chip Protection (DD)
☐ FC360: 8:30 a.m. - 12:00 p.m. Electrical Overstress in Manufacturing and Test
☐ DD115: 8:30 a.m. - 12:00 p.m. Latch-Up Basics and Testing **REVISED**
☐ DD/FC380: 8:30 a.m. - 12:00 p.m. Electrostatic Calculations for the Program Manager and the ESD Engineer (PrM) **REVISED**
☐ DD117: 1:00 p.m. - 4:30 p.m. TCAD Fundamentals and First Applications to ESD **REVISED**
☐ DD340: 1:00 p.m. - 4:30 p.m. Integrated ESD Device and Board Level Design
☐ DD302: 1:00 p.m. - 4:30 p.m. Troubleshooting On-Chip ESD Failures
☐ FC200: 1:00 a.m. - 4:30 p.m. Packaging Principles for the Program Manager (PrM) **NEW**
☐ DD/FC165: 1:00 p.m. - 4:30 p.m. ESD Control Concepts for Design, Validation, and Test Engineers

THURSDAY, SEPTEMBER 17

☐ DD319: 8:30 a.m. - 12:00 p.m. Physical Process, Device and Circuit Simulation (TCAD) Methodologies in Application to Industrial ESD Research and Design
☐ DD260: 8:30 a.m. - 12:00 p.m. Design for EOS Reliability
☐ DD150: 8:30 a.m. - 12:00 p.m. Introduction to RF ESD Design **NEW**
☐ DD/FC250: 8:30 a.m. - 12:00 p.m. What Information Needs to be Exchanged for Potential EOS Problem
☐ FC120: 8:30 a.m. - 12:00 p.m. Ionization Issues and Answers for the Program Manager
☐ FC210: 8:30 a.m. - 12:00 p.m. ESD Standards Overview for the Program Manager (PrM) **NEW**
☐ FC166: 1:00 p.m. - 4:30 p.m. ESD QMS Best Practices Strategy Including Class 0 and Costly Controversial ESD Myths **NEW**
☐ FC365 1:00 p.m. - 4:30 p.m. Practical Applications of Ionization
☐ FC150: 1:00 p.m. - 4:30 p.m. Hands-on ESD Measurments & Instruments - Uses and Pitfalls
☐ DD220: 1:00 p.m. - 4:30 p.m. Transmission Line Pulse (TLP) Basics and Applications (DD)
☐ DD381: 1:00 p.m. - 2:30 p.m. Electronic Design Automation (EDA) Solutions for ESD
☐ DD382: 3:00 p.m. - 4:30 p.m. Electronic Design Automation (EDA) Solutions for Latch-up

Please continue and fill out all sections (3 and 4) of this form on next page

Registration - page 2

Register Online!
http://www.cvent.com/d/86qf9q

EOS/ESD Symposium and Exhibits, September 15-20, 2019
Riverside Convention Center, Riverside, CA, USA

Remember to fill out sections 1 and 2 on page 1 of this form.

Please Print or Type

First Name: _____ Last Name: _____

Company Name: _____

Phone: _____ E-mail: _____

How did you learn about this event? _____

☐ Under the Americans With Disabilities Act, I require auxiliary aids or services.
☐ I am taking the ESD Certified Professional-Program Manager exam: 9-20-19.
☐ I am taking the ESD Certified Professional-Device Design exam: 9-20-19.

3 Fees: Please check appropiate boxes.

Save by registering in advance! This will facilitate your registration upon your arrival at the Symposium. Early registration and member discounts* are valid only if received no later than July 15, 2019.

☐ **Symposium $800**
(Includes technical sessions, workshops, and exhibits)
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $600/Non-Members $700

☐ **First Time Attending**

☐ **Tutorials $710**
(Sunday, Monday, OR Thursday (Full Day))
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $510/Non-Members $610

*Membership discounts apply to those who participate as members all year long and are current at the opening of symposium registration. Memberships processed after this date will not apply. You will receive a complimentary 2020 membership with your Symposium registration which will allow you to enjoy the full benefits of membership in 2020.

☐ **Bundled Fees $2,465**
(Symposium plus Sun., Mon., and Thurs. full tutorial days)
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $1,765/Non-Members $2,165

Student Fees
The EOS/ESD Association, Inc. offers a fifty percent discount for full-time students. Proof of enrollment required. Student fees apply only to symposium or tutorial registration and do not apply to bundled fees, ANSI/ESD S20.20 seminar, or Emerging Topics.

☐ **ESD Program Development and Assessment (ANSI/ESD S20.20) $1,710**
(Attendance limited to first 30 registrants)
This seminar is not included in the bundled fee.
Early Registration Fees valid until July 15, 2019
EOS/ESD Association, Inc. Members* $1,510/Non-Members $1,610

Register 5 or more people from one company at the same time and save $100 per person. Please contact EOS/ESD Association, Inc. prior to registering.

4 Payment: Company purchase orders not accepted.

☐ **Check** (Make payable to EOS/ESD Association, Inc.)

TOTAL ENCLOSED $ _____

Type: __Visa® __Master Card ® __AMEX® __Discover®

Credit Card # _____ **Expiration Date:** _____ **Code:** _____

Print Name on Card: _____

Billing Address: _____ **City** _____ **State** _____ **Zip** _____

Include payment with this form. Mail form and payment to: EOS/ESD Association, Inc., 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069, USA, Tel: +1-315-339-6937. Students must include proof of full-time enrollment to obtain student fees. Only U.S. currency, checks drawn on a U.S. bank that is a member of the U.S. Federal Reserve, travelers checks payable in U.S. dollars, and credit cards (Visa®, Master Card®, AMEX®, and Discover®) will be accepted. Pick up registration materials at the Registration Desk when you arrive. Cancellation & refund requests will be honored if received in writing no later than July 15, 2019, and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

IEW 2020

14th Annual International Electrostatic Discharge Workshop

Now in its 14th year, the IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities. The workshop will include a tutorial, invited seminar speakers, discussion groups, invited talk speakers, technical presentation sessions, and special interest groups. The IEW is the perfect opportunity to submit late-breaking and exciting new research to stimulate discussion and interaction around new ideas, encouraging new research topics. To maintain the unique IEW experience and provide ample opportunity for discussion, there will be an increased focus on discussion groups and invited speakers in 2020. The IEW workshop presentation format for technical sessions will begin with each author presenting a brief summary to highlight key findings, followed by an interactive poster-based discussion session among authors and attendees. The IEW is closely aligned with the EOS/ESD Symposium for collaborative conference activities.

Save the date

May 4-8, 2020
2020 International ESD Workshop (IEW)
Tagungshotel Jesteburg
Hamburg, Germany

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069, USA

PH +1-315-339-6937 • Email: info@esda.org • www.esda.org

EOS/ESD Symposium and Exhibits
September 7-18, 2020
Peppermill Resort and Casino, Reno, NV USA

Mark Your Calendar!

Setting the Global Standards for Static Control!

EOS/ESD Association, Inc. 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069, USA
PH +1-315-339-6937 • Email: info@esda.org • www.esda.org