International Electrostatic Discharge Workshop (IEW) May 8 – May 11, 2023

Setting the Global Standards for Static Control!

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The IEW Experience

Dear Colleagues and ESD Enthusiasts, greetings on behalf of the 16th annual International ESD Workshop (IEW) Management Team! This in-person event presents a unique opportunity for attendees to participate in in-depth discussions and learning on EOS, ESD and Latch-up topics in a highly interactive environment. This year, the IEW will be held at the Evangelische Akademie, Tutzing, located on the shores of the Lake Starnberg, 30 kilometers southwest of Munich. This 18th century mansion encourages thoughtful discussions and immersive interaction.

The IEW is structured around a high quality and well balanced program presented by highly skilled and recognized professionals in the field of EOS/ESD and beyond, from both industry and academia. The schedule of the IEW includes 1 Tutorial, 1 Keynote Speech, 1 Industry Council Report, 3 Seminars, 3 Invited Talks, 3 Discussion Groups and 3 Technical Poster sessions.

Come and follow an instructive tutorial on signal integrity and ESD, an interesting keynote speech on programmable matters related to analog and digital computing in the magnetic domain, and the Industry Council report presented by a prominent ESDA member.

Come and listen to stimulating state of the art seminars and invited talks addressing a large variety of EOS/ESD topics. Seminars will be given on Electrical overstress problems and solutions, Transient absolute maximum rating (tAMR), and Exploring ESD events by virtual testing. Invited talks are also scheduled on Electromagnetic field coupling to transmission lines, ESD along the “Chain”, and Foundry ESD deliverables and parameters.

Come and engage round-table live discussions on subjects that matter to ESD Engineers, by participating to Discussion group parallel sessions where exiting topics like ESD challenges for advanced CMOS, Future challenges for Latch-up in testing, Third party interface IP, Reliability of GaN power HEMT’s, Heterogeneous integration and ESD, and ESD challenges for the automobile will be discussed.

Come and discover the core of the IEW technical program, with the poster sessions on ESD Modeling and testing, ESD protection circuit and design, and ESD device and technology. They provide an ideal forum for exchanging ideas between the participants.

Come and experience the IEW.

We sincerely hope that you will join us at the 2023 IEW in Germany.

***Dr. Ir. Dolphin Abessolo-Bidzo**,*
NXP Semiconductors,
Management Committee Chair

Tutorial
Monday, May 8, 13:00 – 16:30

Signal integrity and ESD – Simulations for optimal ESD protection

Dr. Andreas Hardock, Sergej Bub, Nexperia Germany GmbH; Dr.-Ing. Jens Werner, Jade Hochschule Wilhelmshaven/Oldenburg/Elsfleth

This tutorial briefly introduces the basics of electrostatic discharge and demonstrates practical protection concepts using the examples of modern high-speed interfaces in automotive and mobile applications e.g. 1000BASE-T1 and USB4. It is discussed how modern ESD protections behave in the time and frequency domain using common solvers e.g. CST and ADS and how their system impact can be analyzed with the help of simulations. Furthermore, the advantages of SEED simulation are demonstrated on several examples for transient ESD events on device and system level using dedicated behavioral dynamic SEED models incl. their implementation based on TLP data.

Andreas Hardock studied nanostructure technology at the Julius-Maximilian-University of Würzburg and received his doctorate in the field of functional vias at the TU Hamburg-Harburg under Prof. Schuster. He started his professional career in the automotive sector as an EMC engineer at Behr-Hella Thermocontrol. From 2016 to 2020 he was at Continental Automotive GmbH in Babenhausen, where he was responsible for SI/PI EMC and ESD topics in the role of hardware architect in product development. Since 2020, he has been responsible for ESD/EMC topics at Nexperia as Application Marketing Manager.

Sergej Bub received the M.Sc. degree in electrical engineering specialized in nanoelectronics and microsystem technic from Technical University Hamburg Germany in 2017. He is currently a System Level ESD Expert at Nexperia working in the development department with the focus on modelling and simulation of high-speed systems for mobile, computing and automotive applications as well as on development and optimization of discrete ESD protection components used for system-level ESD protection.

Seminar I
Monday, May 8, 17:00 – 18:00

Electrical Overstress: Past & Present, Problems and Solutions
Karim Kashani, Robert Bosch GmbH

For more than 50 years electrical overstress (EOS) is one of the major reasons for failures of semiconductor devices. In this seminar, the past and present understanding of EOS as well as strategies used to deal with EOS and EOS failures are introduced, analyzed and discussed. Typical problems, pitfalls and fallacies related to this matter are presented and recommendations to solve and overcome these issues are given. Special attention is paid to the concept of absolute maximum ratings and its implications for semiconductor devices. Finally, strategies and tools to effectively deal with potential EOS failures are introduced.

Karim T. Kaschani received his Ph.D. degree for his research in the field of semiconductor power devices in electrical engineering from the Technical University in Brunswick in 1996. He worked for almost 8 years for Siemens Semiconductors and Infineon Technologies as a development engineer and project leader in the field of advanced ICs for switch-mode power supplies, on concept engineering of high voltage SOI technologies and on the development of high voltage ICs. Afterwards he joined Atmel Automotive and worked for almost 7 years as head of the ESD test and consulting group and as product quality engineering manager. Thereafter, he joined Texas Instruments and worked for more than 9 years as senior ESD engineer responsible for the regional ESD and EOS support in Europe. He then worked for 2.5 years as leader of the ESD team for Elmos Semiconductors S.E. and is currently working as senior ESD engineer for Robert Bosch GmbH in Germany. He holds several patents and is author or co-author of several papers, conference presentations and tutorials in the fields of semiconductor power devices, ICs, semiconductor technologies, ESD and EOS.

Welcome Entertainment
Monday, May 8, 19:00 – 20:00

Science or Fiction: "Is AI Ready for Museums – are Museums Ready for AI?"
Prof. Dr. Andreas Gundelwein, Baden-Württemberg State Museum on Technology and Work

New technologies often induces hopes – as well as fears, in many cases unrealistic hopes – as well as baseless fears. Examples are the railway in 19th century, biogenetics in the 20th century – as well as Quantum computing and Artificial Intelligence (AI) in the 21st century. Without understanding the basic principles, opportunities, limits and risks of new technologies society will not accept them and will not develop the necessary consensus. Additionally, a lack of acceptance, knowledge, and motivation will result in a future lack of experts and staff. To build up knowledge, competence and acceptance in the field of new technologies museums are playing a key-role. Museums are highly credible center of competence, are reaching many different groups of age and education and are offering low-threshold approaches to science and technology. But to exhibit and communicate abstract topics like AI, new concepts, methods and formats including artwork are needed. Also, a strong cooperation with research institutions and industry is indispensable. The talk presents a couple of interesting and state-of-the-art approaches to this challenging task.

Andreas Gundelwein was **b**orn 1965 in Hamburg and studied archaeology and geosciences in Hamburg and Freiburg, Germany. Since 1993 he is active in the field of museum management, science communication and MINT-education. From 2014 to 2022 he was responsible for the conception and realization of the new branch of Deutsches Museum in Nuernberg, the “Museum of the Future” (https://www.deutsches-museum.de/nuernberg), presenting a broad range of new technologies and their possible impacts on society. During this time he successfully established the project “Intelligent Museum” in cooperation with ZKM (Center for Art and Media, Karlsruhe ; https://zkm.de/de/projekt/intelligentmuseum), as well as the “Quanta”-project on Quantum technologies, both funded by the federal government of Germany. Beside this, he is a member of the scientific advisory board of “Buendnis fuer Bildung” (https://www.bfb.org/) and was a boardmember of MINTaktiv (https://www.mintaktiv.de/) from 2014-2022. Since January 2023 he is Managing Director of TECHNOSEUM, the Baden-Württemberg State Museum on Technology and Work and Germanys third largest Museum on Science and Technology (https://www.technoseum.de/). The next challenge is the projected expansion of TECHNOSEUM, doubling the exhibition space and aiming to future technology and communication.

Keynote
Tuesday, May 9, 9:30 – 10:00

Programmable Matter(s): Analog and Digital Computing in the Magnetic Domain

Dr.-Ing. habil. Markus Becherer, Technical University of Munich

Digital computation with ferromagnetic multilayer islands is a promising technology in Beyond CMOS device research. In the physical implementation of the so-called perpendicular nanomagnet logic (pNML), it offers intrinsically non-volatile computational states, atto-joule dissipation per bit operation, and CMOS-competitive data throughput. Another route to computing in the magnetic domain is through spin-wave devices fabricated by direct patterning with a focused ion beam. Inspired by optical designs such as lenses, gratings, and Fourier domain primitives, complex structures for neuromorphic and edge AI implementations are developed, generally: programmable matter for unconventional computing.

Dr.-Ing. habil. Markus Becherer is currently the group leader for nanomagnetic device research at the Chair for Nano and Quantum Sensors at the Technical University of Munich (TUM) and, at the same time, technical director of ZEITlab, the central electronics and information technology labs of the TUM School of Computation, Information, and Technology. He received his diploma in electrical engineering from TUM in 2005. In 2011, he received his Dr.-Ing. degree from TUM and was awarded the Kurt-Fischer-Prize for an outstanding thesis. After graduation, he was head of the nanomagnetic logic research group at the Chair for Technical Electronics. Since 2017, he has been an adjunct teaching professor at TUM in the field of micro and nanoelectronics. From 2017 to 2020, he was provisional head of the Chair for Nanoelectronics at TUM. His research interests are fabrication technologies for nanostructures, prototyping platforms for device technologies, and magnetic devices and systems for sensing and computing.

Invited Talk 1
Tuesday, May 9, 11:00 – 12:00

Why the Wire is on Fire - Electromagnetic Field Coupling to Transmission Lines

Dr.-Ing. Mathias Magdowski, Otto von Guericke University

Cables and transmission lines attached to devices and complex systems may act as parasitic receiving antennas and can guide unwanted radiated electromagnetic disturbances into connected sensitive electronics like sensors or measurement units. In this talk, the basic field-to-wire coupling phenomena will be described. Analytical and numerical calculations will be explained and compared with experimental results.

Mathias Magdowski was born in Wolmirstedt, Germany in 1984. He received his Dipl.-Ing. and Dr.-Ing. degree in electrical engineering from the Otto-von-Guericke University, Magdeburg, Germany in 2008 and 2012, respectively, where he is currently working as a scientific co-worker at the Institute for Medical Engineering. His current research interests include analytical and statistical methods for modeling EMC problems, especially the field-to-wire coupling of statistic fields in mode-stirred chambers. He is a member of the corporate research group 767.3-767.4 within the German Commission for Electrical, Electronic & Information Technologies and serves as the co-convenor of the Joint Working Group on Reverberation Chambers within the International Electrotechnical Commission and the International Special Committee on Radio Interference. Mathias Magdowski also volunteers as a marketing & member services coordinator within the Institute of Electrical and Electronics Engineers (IEEE) German EMC Chapter and in the IEEE Student Branch in Magdeburg.

Seminar 2
Tuesday, May 9, 13:00 – 14:00

Industry Council's White Paper on Transient AMR
Harald Gossner, Intel Deutschland GmbH

Industry Council on ESD Target Levels is currently releasing a new White Paper of tAMR. It builds the base for an understanding of a wide range of transient pulse parameters that affect reliability shared between semiconductor suppliers and system integration customers. The seminar will explain how the paper clarifies the terminology of transient absolute maximum ratings (tAMR) and related parameters. Field relevant examples of the use of transient AMR information for a robust system design in various application fields will be demonstrated. Depending on the application fields recommendations are provided how to establish an efficient and meaningful data preparation and information flow between supplier and customer. This addresses both standardized, application specific test methods and generic characterization methods (like Wunsch-Bell). The report recommends a novel extraction of tAMR limits covering the regimes of reliability degradation effects and of damage due to excessive transient stress conditions. The phenomena and the gaps of understanding in the region of combined effects of transient stress and reliability degradation are highlighted.

Harald Gossner is senior principal engineer at Intel. He received his diploma degree in physics from Ludwig-Maximilians-University, Munich, in 1990 and his PhD in electrical engineering from Universität der Bundeswehr, Munich, in 1995. For 15 years, he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2011 he joined Intel leading the system ESD activities for Intel products. Harald Gossner has authored and co-authored 150 technical papers and two books in the field of ESD and device physics. He holds 110 patents. He received several best paper awards at the EOS/ESD Symposium and the outstanding achievement award of EOS/ESD Association, Inc. Harald served as Technical Program Chair and General Chair of the EOS/ESD Symposium. In 2006 he became co-founder and co-chair of the Industry Council on ESD Target Levels. Currently, he represents EOS/ESD Association as president and contributes as an editor to IEEE EDL.

Technical Session A: ESD Modeling and Testing
Tuesday, May 9, 14:30 – 15:30

A.1 Where is the charge deposited in the IC when a CDM discharge occurs?
Theresa Lutz, Kai Esmark, Infineon Technologies AG

This presentation uses 3D finite element simulations in order to evaluate the capacitance of simple cylindrical test objects and of a complex Si die in a wire bond package: The simulated charge distributions provide insights into the initial charge conditions of a CDM discharge event.

A.2 Oscillation of a Power Clamp during JESD78 Latchup Stress
Wolfgang Hartung, Irene Geijselaers, Adrien Ille, Reinhold Gaertner

In JESD78E and earlier versions, the definition of a Latch was mainly focused on the triggering of a parasitic SCR structure. However, many other structures are possible as root cause for a parasitic low impedance path between a given supply and GND rail. In this contribution a case study shall be given for a power clamp triggered upon signal stress in the JESD78 stress, emphasizing the importance of the changes done for the F Version of the JESD78 standard.

A.3 Software development: towards enabling full 300mm automated measurements for ESD research
Dieter Claes, IMEC

This work focuses on the structured automation of ESD data-acquisition and processing. This not only has the advantage of faster, less error-prone, measurements but also the benefit of easy upscaling from a single device to automated data acquisition from a range of devices, dies or even wafers.

A.4 Simulation of ESD in 2.5D/3D Bonding Technologies
Shane Lin, Piet Wambacq, VUB; Marko Simicic, Nicolas Pantano, Shih-Hung Chen, imec

This presentation evaluates the CDM risk of D2W and W2W bonding by commercial electrostatic simulators and analytical calculation. The results show the voltage difference between the wafer and die is reduced as they come closer together. The impact of the wafer warpage on CDM risk has also been checked. The results show the wafer warpage has almost negligible impact on CDM risk.

A.5 DC SMUs of an HBM/LU tester: Limitations & Exploiting the Possibilities

Sheela Verwoerd, Jian Gao, Marcin Grad, Michael Stockinger, NXP Semiconductor

DC SMUs in MK2 tester is useful to determine fail or pass condition of IC by performing parametric tests. This poster shows effect of current range/limits on measurement accuracy and how we correctly exploit usage of DC SMUs. DC SMUs can be used to compensate for tester artifacts, too.

A.6 Future Challenges in LU Testing

Wolfgang Hartung, Irene Geijselaers, Magdalena Hilkersberger, Reinhold Gaertner, Infineon Technologies

The latest JESD78F update brought changes in LU Testing, yet there are still problems for products regarding test execution and still many consider the JESD78 Test to be incomplete in its coverage. In this poster we give insights and initiate discussion on the future challenges of the Test. This includes HV technologies, TLU and SLS, and misconceptions of the standard.

A.7 Miscorrelation Between VF-TLP and CDM in T-Coil for High-Speed IF

Hideki Kano, Teruo Suzuki, Socionext Inc.

Simulations were performed for the T-coil using different current waveforms for VF-TLP and CDM. Mutual induced voltage of T-coil was more pronounced in VF-TLP than in CDM. Since VF-TLP (TLP) is a tool for ESD design, ESD designers need to consider this difference during ESD design, especially in leading-edge CMOS technology processes.

Invited Talk 2
Tuesday, May 9, 17:00 – 18:00

ESD along the "Chain"
Rita Fung, Cisco

Different people have different thoughts about ESD. I/O designer wants to know the ESD spec current. Manufacturer wants to know the ESD passing voltage. Foundry wants to know if you are going to waive the ESD design rule at your liability. Contract manufacturer wants to know if the failed component is an outlier. In this talk we will look into different problems from different perspective, how each problem can be addressed gradually with collective effort.

Rita Fung is currently a Technical Leader in Technology & Quality at Cisco Systems (HK) Ltd. She received her MSc in IC Design Engineering from the HKUST and MEng/BEng in Electronic & Information Engineering from the HKPolyU. She worked as ESD design & Layout Engineer in Solomon Systech and TSMC prior to joining Cisco. She has been actively engaged in semiconductor quality and reliability, her focus and specialty in ESD leads her to be regional expert in supporting ESD issues in design & manufacturing. She has published and co-authored a few technical papers in ESD area.

Discussion Group Session A (Parallel Sessions) Tuesday, May 9, 19:00 – 20:30

A.1 - ESD Challenges for Advanced CMOS: Moving towards Nanosheet and Backside Technology Options

Moderator: Shih-Hung Chen, IMEC

Next to bulk FinFET technologies, a gate-all-around (GAA) architecture has been proposed as a promising candidate because of improved channel electrostatic and leakage control. Vertically stacked horizontal nanosheets (NS) with the GAA architecture can further maximize the driving current per layout footprint. Besides of the novel transistor architecture, more design-technology co-optimization (DTCO) scaling options, such as buried power rail (BPR) and back-side power delivery network (BS-PDN), have been also proposed as scaling boosters in future logic CMOS technologies. However, only very few prior works discussed ESD reliability in these promising future technologies. In addition, the challenges might not only from technology options but also from more realistic aspects, such as design verification and product qualification. This discussion group aims to look at the ESD challenges in advanced CMOS technologies with varied perspectives. With your ideas and sharing experience, this discussion group will be able to bring some clarity to those emerging ESD challenges.

A.2 - Future Challenges for Latchup in Testing

Moderator: Wolfgang Hartung, Infineon

The future brings new challenges for the JESD78 test: The spectrum of IC products has extended to FinFET and HV technologies, pin voltages have developed to decreasing (< 2V) whereas increasing (> 100V) classes. This arises a number of questions how the JESD78 Test is to be done in the future: White Paper 5 of the Industry Council for ESD Targets showed that the JESD78 is still regarded as useful, yet the perception was revealed that the test coverage is far away from being complete. Transient Latchup and ESD System Level Stress are supposed to close this gap for customers. It is believed that the common JESD78 Targets seem to provide a basic level of robustness, yet references for real life events in the field are missing. LV pins seem to see no current injection at all, while for HV products no commercial test solutions are available at the moment. Soft fails or other functional failures are no regarded at all. With this discussion we want to get a better feeling for future requirements of Latchup Testing.

Technical Session B: ESD Protection Circuit and Design
Wednesday, May 10, 9:10 – 10:00

B.1 Influence of Bus Inductance on Product CDM Robustness
Patrick Huff, Kai Esmark, Christian Russ, Infineon Technologies

CDM discharge currents flowing across product inherent inductive paths like extended bus systems might limit the overall CDM robustness of the product. A significant increase of the CDM withstand current can be achieved through a simple layout change to the bus architecture which is demonstrated on theoretical and experimental level.

B.2 ESD Protection Design for Overvoltage Supply Pins
Steffen Schumann, Mirko Scholz, Infineon Technologies

In analog mixed-signal ICs often some pins are powered above the nominal supply voltages of the IC. With simulation and measurement data we will show the implementation of over-voltage ESD supply protection clamps. Our design ensures a fast turn-on during CDM stress and an equal stress of the gate oxides during DC operation.

B.3 ESD Protection of Differential High-Speed Inputs in a SiGe-HBT BiCMOS Process
Dolphin Abessolo-Bidzo, Siamak Delshadpour, NXP Semiconductors

Differential multi-GHz high-speed and RF inputs pairs are very challenging to protect against ESD stress without degrading their high-speed and RF performance. In this poster, a novel ESD solution of high-performance combo re-driver in the 10.3 GHz range is presented and successfully implemented in a 0.25µm SiGe-HBT BiCMOS Process technology.

B.4 Design of Ultra-Low-Leakage (ULL) Clamps in a 22nm CMOS Technology
Nandha Kumar Subramani, Alain Loiseau, Xuejiao Yang, Souvick Mitra, GLOBALFOUNDRIES

A 3.3 V ULL RC clamp was designed using a SCR as the discharge device to achieve ultra-low leakage current (< 1 nA). To avoid mis-triggering the SCR device (potential latch-up issues), a large trigger current was implemented. The designed clamp demonstrated well behaved TLP/HBM performance and straightforward tuning of both trigger voltage and current.

B.5 WITHDRAWN

B.6 Tool Independent Method for Removing Common IO Resistance in Layout Driven ESD Network Analysis

Jordan Davis, Woojin Seo, Chanhee Jeon, Samsung Foundry; Ahmed Saleh, Siemens

One factor determining the effectiveness of on-chip ESD protection is the parasitic resistance from IO to protection that is not common to any other device. A simple method for accurately calculating this using existing EDA tools has been developed, allowing for point-to-point resistance to be used as a sign-off tool.

Discussion Group Session B (Parallel Sessions) Wednesday, May 10, 19:00 – 20:30

B.1 - Third Party Interface IP: Evaluation of ESD Design and Qualification
Moderator: Peter de Jong, Synopsys

The use of 3rd party IP to substitute or complement own developments is common practice in many companies but may lead to new questions. There are two aspects related to 3rd party IP that we want to address in this Discussion Group:

1. Foundry providing the IP design 'tools' (ESD guidelines, ESD data, ESD design flow, ESD check runsets, etc.) How to ensure that the foundry ESD guidelines and runset checks provide sufficient coverage? Does the foundry 'guarantee' good ESD if checks pass? If not, what type of assessment is needed to evaluate the IP? Add-ons needed?
2. IP provider developing the IP and performing the silicon qualification. Is fulfillment of foundry ESD guidelines/rules a requirement? Is it sufficient? Is it feasible? What about the applicability of foundry guidelines for 'special' IP (RF, OVT, high-speed)? What is the relevance of pre-silicon check results when the IP is qualified? What is the recommended IP CDM qualification procedure? Differences between CDM waveforms on test chips and on product: How does this work out in practice? New approaches required for D2D interface IP?

B.2 - Reliability and Other Factors Hindering GaN Power HEMT's Market Acceptance – Are we doing enough?
Moderator: Prof. Mayank Shrivastava of the Indian Institute of Science, Bangalore

In 2014 several market reports projected GaN power HEMTs to reach $600 million by 2020 and $6 billion by 2025. Eight years down the line we are still far from the projections and commercial GaN HEMTs are still far from the fundamental limits. There are several reasons for it, however, the biggest showstopper is the reliability gap. System level/transient reliability and lack of guidelines/standards to qualify/ understand it is a growing concern, which is increasing the reliability gap. The threat increases further while pushing for high switching frequencies, high power density, and higher peak power. The question is are we doing enough to address it and understand it? Can conventional approaches, often followed in Silicon power technologies, work for GaN power technologies? If not, then what should be the approach to address it? To what extent system designers are required to work with device and reliability engineers? Do we have the right tools to address it? Are there fundamental limiting factors? There are several other open questions that are required to be discussed and debated. This discussion offers an open platform to share the experiences of stakeholders from the device and power electronics/ automotive industry; listen to suggestions; and brainstorm ways forward to address this pressing concern, which is hindering GaN power HEMT's performance and market acceptance.

Seminar 3
Thursday, May 11, 09:30 – 10:30

Exploring ESD Events by Virtual Testing Using Physics-Based Computer Simulation

Gerhard K.M. Wachutka, Technical University of Munich (retired)

Abstract

Prof. Gerhard K.M. Wachutka's research interests cover the basic physical principles of microstructured components and systems, in particular in the area of electronic components and microsensors and microactuators. He uses physics-based modeling and predictive computer simulation for "virtual prototyping". The aspects investigated include the robustness and reliability of components and appropriate design optimization. Prof. Wachutka studied physics at Munich's Ludwig Maximilian University and did his doctorate in theoretical solid-state physics there in 1985. After that, he joined Siemens' Research & Development division, where he worked on the computer-aided development of modern high-performance components. From 1990 to 1994, he worked at the Swiss Federal Institute of Technology's physical electronics laboratory in Zurich. There, he led the modeling and simulation group for micro-mechatronic components and systems. Since 1994, he has held the Chair of Physics of Electrotechnology at TUM.

Invited Talk 3
Thursday, May 11, 11:00 – 12:00

Foundry ESD Deliverables and Parameters, Including an Update of ESDA Working Group 22 ESD TR22.0-01

Dr. Efraim Aharoni, Tower Semiconductor

An effective ESD protection, planned at IC design level, requires information and data exchange between the foundry supplier, IP vendor, IC designer, and EDA tools vendors. The trade-off between the ESD capability and the signal integrity is reflected in key ESD parameters extracted from dedicated measurements. Foundries manufacturing integrated circuits (IC's) should supply a variety of ESD-related deliverables in a process design kit (PDK). This talk highlights the recommended guidance given to the ESD engineer in the foundry, in the process of creation and supplying the ESD portion of the PDK and other deliverables. In particular, providing of a variety of special parameters required for design of an optimized ESD protection in the IC. An extensive effort has been invested by WG22 to update the first published technical report, ESD TR22.0-01. A significant portion of the update includes recommended ESD characterization and extracted parameters related to emerging technologies/applications like RF, SOI, BCD, advanced CMOS, and more. The report includes an overview of benchmark key ESD parameters, test structures, measurements, extraction methods, and useful presentation of the information. The designer and the EDA tool vendor are equipped with the know-how of using the parameters in optimizing the ESD window as well as developing effective methods of proper ESD protection, ESD checkers and simulations.

Efraim Aharoni received his MSc and PhD in physics in 1989 and 1994 from the Technion, Israel Institute of Technology where he focused on high temperature superconducting devices. He joined Tower Semiconductor in 1993 and has worked in a variety of fields – engineering, management, development, and production. Amongst his engineering roles: process, device, yield, director R&D CMOS and reliability. He has led the ESD and latch-up activities as a senior principal engineer including the development of new ESD devices and protection concepts, creating libraries of ESD devices in PDK, development of a unique concept of empirical ESD modeling (for simulation of circuits containing snap-back based devices), PERC, and customer support. He works closely with the design center, device engineers, PDK group, customers, and production lines, at sites worldwide. Efraim has been a TPC member for IEW and EOS/ESD symposia, is co-chair of WG22, and a member in the Industry Council. In addition, he is the head of the Electrical Engineering department in the Kinneret College on the sea of Galilee and lectures on a variety of courses.

Discussion Group C (Parallel Sessions)
Thursday, May 11, 13:00 – 14:30

C.1 - Heterogeneous Integration and ESD
Moderators: Marko Simicic, imec; Heinrich Wolf, Fraunhofer EMFT

An increasing number of products is using 2.5D bonding technologies. Some products with 3D bonding have also appeared on the market in the past years. This brings forward challenges for ESD protection designs, ESD testing and ESD control requirements. ESD circuit designers face limited silicon area and increasing interconnect frequency bandwidths. ESD control engineers face extremely low CDM target levels and an unclear assessment process. ESD test engineers face testing bare dies/wafers with tens of thousands of µ-bumps. To tackle these challenges, the Industry Council on ESD target levels published the White Paper 2 in 2021 and is expected to publish an update in 2023. The suggested CDM levels for heterogeneous integration are 30 V and below, down to 5 V. This discussion group will try to answer questions like: How low does CDM protection need to go? What CDM levels can ESD control achieve in 2.5D and 3D bonding processes? How do we test CDM with these constraints?

C.2 - ESD Challenges for the Automobile in the Near Future
Moderator: Steffen Holland, Nexperia

In the automobile the data rates on bus systems constantly increase. This is caused by the ongoing trend of adding more electronic components to the car. Existing high speed ICs operating at low voltages were/are primarily developed for consumer electronics. Currently, existing automobile system protection schemes are designed for higher voltages. The addition of sensors, permanent internet connection and driving assistance systems, possibly with the aim of a self-driving car, will probably cause architectural changes of the bus system(s). The topic of the discussion is to pick some examples and discuss about the consequences of these changes for ESD protection on system but also on the component level.

Technical Session C: ESD Device and Technology Thursday, May 11, 15:00 – 15:50

C.1 HEMT Based Active Clamps Realized in an HV GaN Technology
Gernot Langguth, Janina Roemer, Infineon Technologies AG

Active clamps based on normally-off HEMT devices are realized in a 600 V GaN technology. DC measurements demonstrate low-leakage behavior within the voltage range of operation. TLP measurements show that very low clamping voltages below 50 V are achieved. Clamping voltage can be tuned by varying the HEMT device width.

C.2 ESD Robustness of Bulk FinFET GGNMOS Impacted by the DTCO/STCO Scaling Options
W-C. Chen, G. Groeseneken, KU Leuven; S-H. Chen, D. Linten, imec

This work focuses on the impact of process option in bulk FinFET GGNMOS. The impact of source and drain epitaxy influenced by the gate pitch and the gate length are studied. Moreover, the ESD performance of GGNMOS in extremely thin Si thickness for STCO scaling are evaluated.

C.3 IV hysteresis in SCR due to interaction of bulk and surface current paths
Rudolf Krainer, Hossam Jomar, Hasan Karaca, Dionyz Pogany, TU Wien; Steffen Holland, Hans-Martin Ritter, Vasantha Kumar, Nexperia

IV hysteresis is observed in discrete technology SCRs with p- and n- buried layers (BLs) and analyzed by 2D TCAD and compact modeling. The hysteresis is due to switching between the bottom current path via BLs and top SCR path, and is not attributed to 3D effects as current filamentation.

C.4 Improving Robustness of GaN HEMT Devices
Abhinay Sandupatla, imec

GaN HEMTs exhibit 3 types of HBM failures, reverse electric field (REF), constant power (CP) and current crowding (CC) failure. Robustness was improved by increasing the gate-ohmic spacing, Field plate length, multi-finger gates and back barrier by 78.6% , and REF by 51.7%, CP by 57.9%, CC by 637% respectively.

C.5 Evaluating Impact of DTCO/STCO Scaling Options on Guard Ring Efficiency

Kateryna Serbulova, Guido Groeseneken, Jo De Boeck, KULeuven ESAT; Shih Hung Chen, IMEC

Design-technology co-optimization and system-technology co-optimization, such as buried power rail and backside power delivery network, have been proposed as scaling boosters in logic CMOS technologies. Also, latch-up risk is still considered as a reliability concern. In this work, the impact of different scaling options on guard ring efficiency is evaluated.

C.6 Compact Modeling of Sequential Finger Triggering in Multi-finger SCRs Using RC Coupling

H. Jomar, H. Karaca, R. Krainer, D. Pogany, TU Wien

Sequential finger triggering phenomenon in multi-finger SCRs is modeled by circuit simulation employing RC elements for inter-finger coupling. Delay between triggering of neighboring fingers up to 250ns is simulated by adjusting parameters of SCR and coupling elements. The results qualitatively reproduce previously reported experimental and TCAD analysis.

Schedule

Start	End	Monday, May 8, 2023
12:00	13:00	Lunch
13:00	14:30	**Tutorial - Signal Integrity and ESD – Simulations for Optimal ESD protection** Dr. Andreas Hardock, Sergej Bub, Nexperia Germany GmbH
14:30	15:00	Break
15:00	16:30	**Tutorial - Signal integrity and ESD – Simulations for optimal ESD protection**
16:30	17:00	Break
17:00	18:00	**Seminar 1: Electrical Overstress: Past & Present, Problems and Solutions** Karim Kashani, Robert Bosch GmbH
18:00	19:00	Dinner
19:00	20:00	**Welcome entertainment – Bavarian Evening & Science or Fiction: "Is AI Ready for Museums – are Museums Ready for AI?"** Andreas Gundelwein, Baden-Württemberg State Museum on Technology and Work
20:00	21:30	Networking/ Social Gathering
		Tuesday, May 9, 2023
7:30	9:00	Breakfast
9:00	9:30	Welcome
9:30	10:30	**Keynote: Programmable Matter(s): Analog and Digital Computing in the Magnetic Domain** Dr.-Ing. habil. Markus Becherer, Technical University of Munich
10:30	11:00	Break
11:00	12:00	**Invited talk 1: Why the Wire is on Fire - Electromagnetic Field Coupling to Transmission Lines** Dr.-Ing. Mathias Magdowski, Otto von Guericke University
12:00	13:00	Lunch
13:00	14:00	**Seminar 2: Transient Absolute Maximum Rating (tAMR)** Harald Gossner, Intel Deutschland GmbH
14:00	14:30	Break
14:30	15:30	**Technical Session A: ESD Modeling and Testing**
15:30	16:30	Poster Discussion Session A
16:30	17:00	Break
17:00	18:00	**Invited talk 2: ESD along the "Chain"** Rita Fung, Cisco
18:00	19:00	Dinner
19:00	20:30	**Discussion Group Session A (Parallel sessions)** A1: ESD Challenges for Advanced CMOS: Moving towards Nanosheet and Backside Technology Options A2: Future Challenges for Latchup in Testing
20:30	21:30	Networking/ Social Gathering

Start	End	**Wednesday, May 10, 2023**
7:30	9:00	Breakfast
9:00	9:10	Announcements
9:10	10:00	**Technical Session B: ESD Protection Circuit and Design**
10:00	11:00	Poster Discussion Session B
11:00	11:30	Break
11:30	12:00	Report on DG Session A
12:00	13:00	Lunch
13:00	18:00	Open time - Prearranged Activities or Welcome to Explore on Your Own
18:00	19:00	Dinner
19:00	20:30	**Discussion Group Session B (Parallel Sessions)** B1: Third Party Interface IP: Evaluation of ESD Design and Qualification B2: Reliability and Other Factors Hindering GaN Power HEMT's Market Acceptance – Are we doing enough?
20:30	21:30	Networking/ Social Gathering
		Thursday, May 11, 2023
7:30	9:00	Breakfast
9:00	9:10	Announcements
9:10	9:30	Industry Council Report
9:30	10:30	**Seminar 3: Exploring ESD Events by Virtual Testing Using Physics-Based Computer Simulation** Prof. Gerhard Wachutka, Technical University of Munich, (retired)
10:30	11:00	Break
11:00	12:00	**Invited Talk 3: Foundry ESD Deliverables and Parameters, Including an Update of ESDA Working Group 22 ESD TR22.0-01** Efraim Aharoni, Tower Semiconductor
12:00	13:00	Lunch
13:00	14:30	**Discussion Group Session C** C1: Heterogeneous Integration and ESD C2: ESD Challenges for the Automobile in the Near Future
14:30	15:00	Break
15:00	15:50	Technical Session C: ESD Device and Technology
15:50	16:50	Poster Discussion Session C
16:50	17:05	Break
17:05	17:50	Report on DG Sessions B & C
17:50	18:00	Closing
18:00	19:00	Dinner
19:00	20:00	Networking/ Social Gathering
		Friday, May 12, 2023
7:30	9:00	Breakfast
9:00	11:00	Check Out

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