2025 International ESD Workshop in US (IEW-US)

Annual International Electrostatic Discharge Workshop
Co-located with 2025 International Reliability Physics Symposium (IRPS)

April 1-3, 2025   Hyatt Regency, Monterey, CA, USA

CALL FOR POSTERS

Now in its 18th year, the IEW continues to provide a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities. In 2025 IEW-US will again co-locate with the International Reliability Physics Symposium (IRPS). In addition to everything IEW-US provides, IEW-US registrants can attend the full IRPS technical program (any technical session, invited talks, and keynote speakers), including the joint evening poster reception. IRPS registrants will have access to IEW keynote and invited talks (but not the other unique elements of IEW-US). IEW-US will retain the defining elements that make it a unique experience: invited speakers, seminars, poster sessions, discussion groups, and some downtime to network and explore the area.

The Technical Program Committee solicits workshop contributions, including data and analysis that advance the state-of-the-art knowledge, enhance or review general knowledge, or discuss new developments with special attention will be dedicated this year to the following focus topics:

3DIC ESD Challenges

2.5D/3D hetero-integrations system-technology co-optimizations (STCO) with 2.5D/3D hetero-integrations and chiplet design concepts have been considered a major future innovation booster in the semiconductor and electronics industry. Discuss ongoing research and development work to better understand the required ESD target levels on ESD testing of die-to-die interfaces and for IP development in 2.5D and 3D ICs.

New Developments in Latch-up Design, Testing, and Standards

Emerging product trends such as technology scaling (e.g., FinFET versus planar CMOS), increasing product complexity, and more demanding operation environments (e.g., automotive, high junction temperature, radiation-induced latchup) lead to the stark reality that latch-up will be a major reliability threat for the foreseeable future.

ESD Threats and Opportunity in Emerging Technologies

Backside power delivery, new materials, Wide-bandgap (WBG) semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), are driving radical transformation in computing, power electronics, LEDs, and communications. These emerging application areas are disrupting many applications that require innovative approaches to meet ESD requirements.

Circuit/Chip/3DIC Electronic Design Automation (EDA)

EOS, ESD, and latch-up EDA are rapidly developing fields. Conventional EDA tools are IC-focused, and each die technology tool needs a complex setup unless a foundry-provided rule deck is used. 3DIC flows present new verification challenges when dealing with complex IC dice, packages, and modules involving multiple technologies and EDA tools. Research into EDA tools is used to design packages, dice, interposers, and modules with compute resources to manage the scaling necessary for these increasingly complex assemblies.

ESD at Foundries – How to meet Customers' Demands?

ESD foundry support challenges, ESD library requirements, ESD documentation content, customer-friendly ESD solutions, EDA tool implementations and pre-sets by foundries, continuous improvements for diverse customer needs, IP verification methodology, and making the ESD solution ecosystem beneficial for both customers and foundries.

Other topics and areas to consider for abstract submissions include but are not limited to:

Anomalous/Unresolved ESD Issues
Random and unrepeatable ESD failures, case histories, ESD tester correlation issues, and unique failure window effects in the stress voltage range.

Automotive Applications ESD/EMC
Contributions addressing ESD and EMC challenges in automotive systems design include compliance with standards such as bulk current injection (BCI), direct power injection (DPI), IEC-61000-4-2, ISO-10605, and ISO-7637.

EDA Tools
EDA verification and simulation tools; techniques, design flows, best practices, experiences with foundry rule decks, commercial tools, and custom tooling. SPICE compact models. TCAD simulations.

ESD and Latch-up Data Analysis
Tools that enable processing large ESD and latch-up tester datasets, viewing CDM waveform parameter statistics, and mapping design data onto ESD and latch-up test programs. Application of AI and Machine Learning to EOS, ESD, and latch-up analyses.

Failure Analysis (FA) Techniques
Locating failure sites, particularly for CDM, imaging techniques, correlating FA-identified damage sites with ESD stress, distinguishing EOS-like failures from ESD failures, and unusual failure modes.

Novel On-Chip Protection Clamps and Circuit Configurations
New clamp devices and clamp configurations, methods to increase the failure threshold of protected devices, high voltage clamps for automotive and power amplifiers, new chip protection concepts, and low-capacitance clamps for RF and high-speed interfaces.

System-Level ESD Issues
On- and off-chip IEC protection clamps, component/ system ESD co-design case studies, cable discharge clamps, transient latch-up, design of system-level clamp circuits, system-level ESD test issues and scan techniques, and ESD-induced soft errors. Cable Discharge Event (CDE) - test methods, applicability, design impact, potential standardization. System ESD design - co-design between the system board and the component (SEED). System ESD simulation methods and component modeling, new stress models. On-chip design methods for improving system ESD. System ESD-related failure modes and case studies. Test methods for validating ESD on the board level. Test standardization of component robustness under system ESD.

Test Characterization, Methods, and Issues
TLP & VF-TLP debug and device characterization methods, correlation of TLP & VF-TLP tests with standard qualification tests, HBM and CDM tester artifacts, unresolved test results and failures, issues relating test qualification levels to real-world exposure, test chip methodology, cable discharge test methods, and test standards issues.

IMPORTANT DATES

Abstract Poster Submission Deadline
February 15, 2025

Notification of Acceptance
February 22, 2025

Final Poster and Teaser Presentation Due
March 15, 2025

Submission Guidelines

Thanks to the co-location with IRPS, submissions will occur through the IRPS Ex-Ordo website (https://www.irps.org/abstract-submission). The poster (in presentation PDF format) should clearly demonstrate specific results and explain the importance of the work in the context of prior work. Use the IEW presentation template available at https://www.esda.org/events/2024-us-esd-workshop-us-iew/. Registration for the conference is required for the author presenting the poster. Accepted posters will be included in poster and five-minute teaser presentation sessions. IEW-US does not publish proceedings but will share presentation slides with the authors' permission. Walk-in posters are also permitted at IEW-US with no prior review. Only the works submitted for review and acceptance will be included in the five-minute teaser presentation sessions.