White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements

Executive Summary

Industry Council on ESD Target Levels

September 2011

Revision 3.0

工业协会关于 ESD 目标级别

This page is intentionally left blank

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements on IC products for safe handling and mounting in ESD protected areas while addressing the constraints from silicon technology scaling and IC design. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), ESD tester manufacturers, ESD consultants and ESD IP companies. In terms of product shipped, the member IC manufacturing companies represent 7 of the top 10 companies, and 12 of the top 20 companies, and over 70% of the total volume of product shipped by the top 20 companies, as reported in the EE Times issue of August 6, 2007. Membership on the Industry Council is continuously growing and interested parties should contact the Chairmen.

Core Contributing Members

Colin Bolger, VIA Technologies
Brett Carn, Intel
***Charvaka Duvvury, Chairman**
Texas Instruments
Yasuhiro Fukuda, OKI Engineering
Reinhold Gaertner, Infineon
Robert Gauthier, IBM
Ron Gibson, Celestica
***Harald Gossner, Chairman**
Infineon
Hiroyasu Ishizuka, Renesas
Satoshi Isofuku, Tokyo Electronics Trading
Larry Johnson, LSI
John Kinnear, IBM
Tim Maloney, Intel
Jim Miller, Freescale
Homi Nariman, AMD
Alan Righter, Analog Devices
Theo Smedes, NXP Semiconductors
Arnie Steinman, MKS Ion Systems
Teruo Suzuki, Fujitsu
Benjamin Van Camp, Sarnoff Europe

Supporting Members (August 2007)

Jon Barth, Barth Electronics
Stephen Beebe, AMD
Leo G. Henry, ESD/TLP Consulting
ChanSu Kim, Samsung
Alan Liang, TSMC
David Mendez, Solectron
Tom Meuse, Thermo Fisher Scientific
Koen Verhaege, Sarnoff Europe
Nobuyuki Wakai, Toshiba
Tetsuaki Wada, Matsushita Electric Industrial

Translation to Mandarin

Zhixin Wang, Synaptics Inc
Yihong Yang, Synaptics Inc

Mission Statement

The mission of the Industry Council on ESD Target Levels is to review the ESD robustness requirements of modern IC products for allowing safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council will provide a consolidated recommendation for the future ESD target levels. The Council Members and Associates will promote these recommended targets to be adopted as company goals. Being an independent institution, the Council will present the results and supportive data to all interested standardization bodies.

Disclaimers

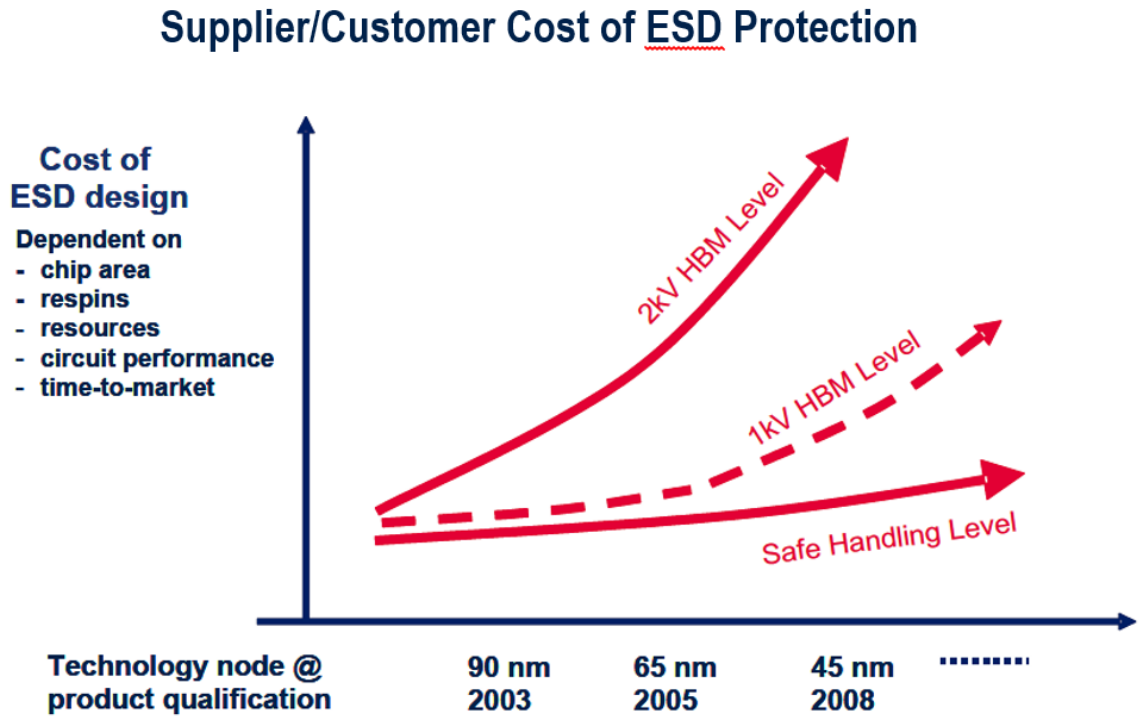
The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.
This document was compiled by independent ESD experts from different semiconductor supplier companies as well as contract manufacturers. The data represents information collected for numerous different products selected for the specific analysis presented here; no specific components are identified. The readers should not construe this information as evidence for unrelated field failures resulting from electrical overstress events or system level ESD incidents. The document only refers to component level ESD recommendations which should have no impact on system level ESD requirements.
The Industry Council while providing these recommendations does not assume any liability or obligations for parties adopting these recommendations.

Executive Summary

In this summary we would like to offer an overview of the White Paper to present the most important issues and conclusions. Further details can be found in the various chapters of the document.

The ESD Challenge

Problem:
The current industry ESD qualification target levels for HBM and MM are unsupportable both in terms of what protection level is needed in a modern manufacturing environment, and what protection level can be practically achieved in an advanced technology IC, especially with high performance circuits. Across the industry we are today failing too many ESD qualification tests based on failures to target levels which have no bearing on real-world stress levels. These issues are having a severe and unnecessary impact on time to market and customer confidence.



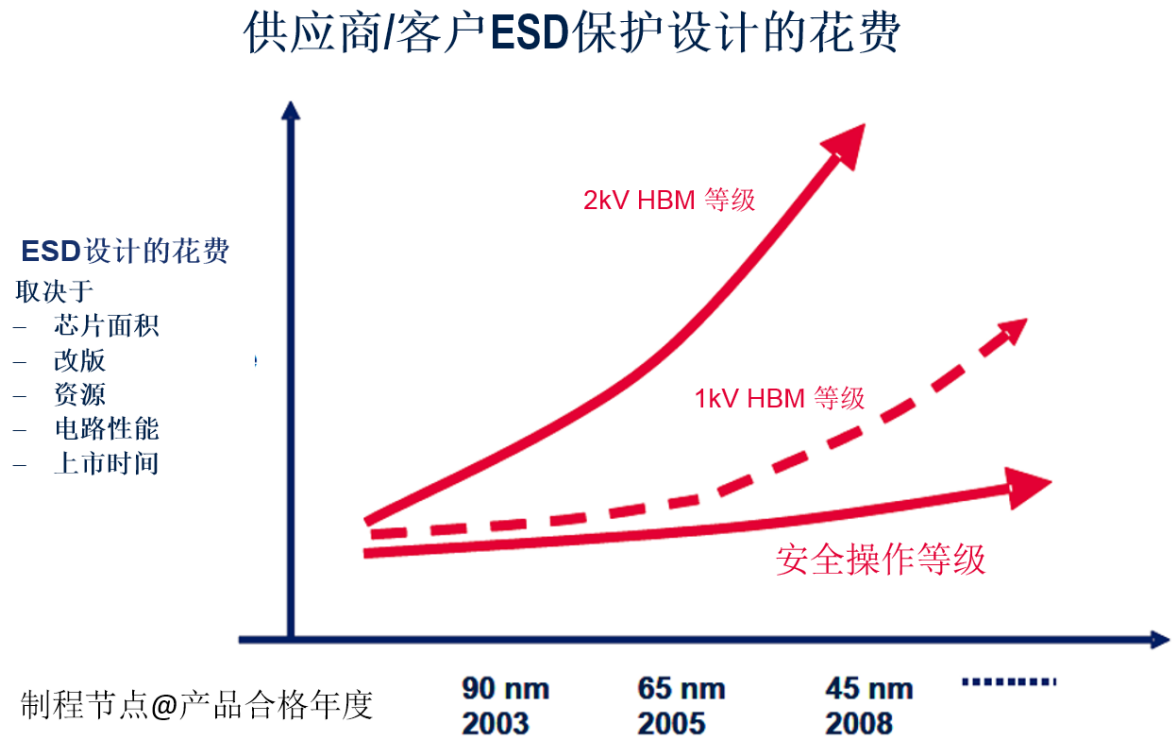
Data:
While the commonly accepted 2 kV HBM requirement was set more than 20 years ago, we have ample evidence showing that this is an over-specified level both in terms of the existing ESD control methods which are effective to control at <500 V (**Chapter 2**), and the lack of any significant ESD field returns from products shipped with ≤2 kV performance (**Chapter 4**).

执行摘要

在本摘要中，我们希望透过白皮书的概述来介绍最重要的问题与结论。更多细节请参照文档中各章节的内容。

ESD的挑战

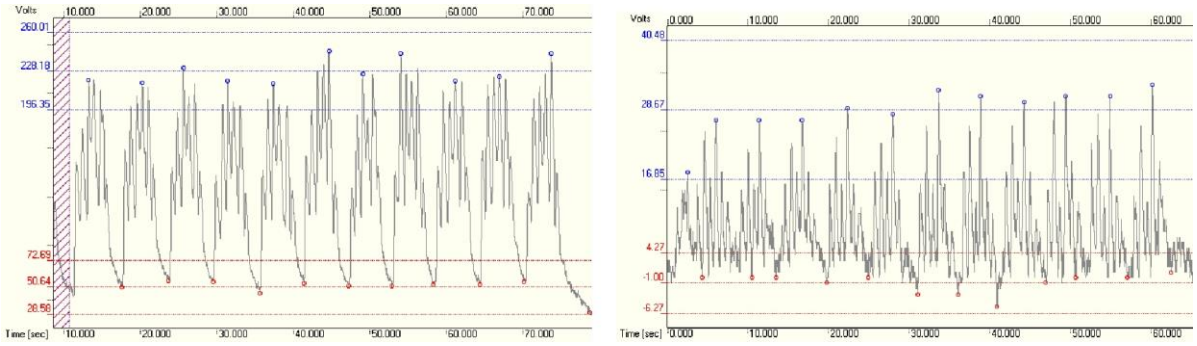
问题：
根据在现代生产环境中哪一种防护级别是必须的，还是在先进制程的IC中，尤其是高性能电路中，哪一个防护级别是可以实现的，目前工业界ESD的HBM与MM模型的合格标准并不能同时支持。纵观整个工业界，由于选用的ESD测试机标准并不能代表实际产品ESD应力水平，导致现在产品在ESD合格测试中不良率极高。这个问题正在对产品上市时间以及客户对产品的信心产生严重的和不必要的影响。



数据：
在20年前订立的2kV HBM标准至今被广泛应用。然而，现有的ESD控制方法能够有效地抑制低于500V的HBM（第二章），并且不高于2kV性能的产品退货率低，我们有充足的证据证明2kV HBM标准过高（第四章）。

Executive Summary (cont.)

The voltage on a person's body as they walk in a controlled manufacturing environment



(a) (b)

(a) ESD levels with basic but less than ideal control methods: Generated Levels @ <500 V
(b) ESD levels with proper basic control methods: Generated Levels @ <100 V

The Proposal:

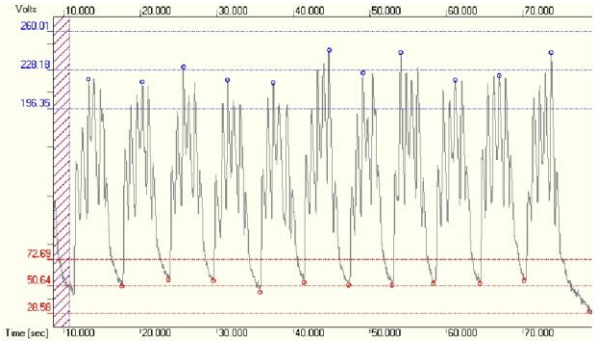
We propose a reduction in HBM and MM ESD target levels to specify realistic ESD level requirements that accommodate both circuit design and safe handling and mounting in ESD protected areas.

HBM Level of IC	Impact on Manufacturing Environment
2 kV 1 kV 500 V	Basic ESD Control methods allow safe manufacturing with proven margin
100 V to <500 V	Detailed ESD Control methods are required

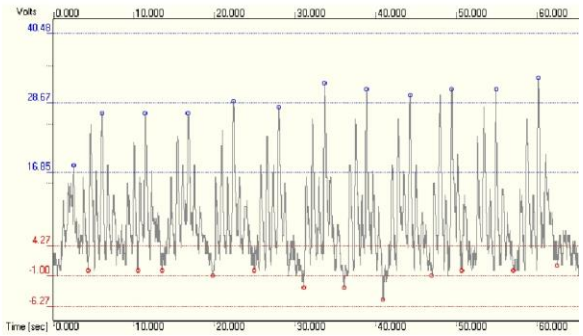
Important note: These proposed HBM levels fully ensure that more than sufficient MM robustness (> 30 V) is also maintained with basic ESD control methods.

执行摘要（续）

当人体在受控的生产环境中行走时产生的电压



(a)



(b)

（a）拥有基本但低于理想的控制方法时ESD的级别：产生的电压电压级别<500V

（b）拥有合适的基本控制方法时ESD的级别：产生的电压级别<100V

提议：

我们提议通过降低HBM与MM的ESD防护级别来设定实际的ESD防护标准，从而兼顾电路设计并且满足在ESD保护区域的安全操作与放置。

芯片的HBM级别	对生产环境的影响
2 kV 1 kV 500 V	基本的ESD控制方法可以保证安全生产，并具有经过验证的良性误差
100 V 至 <500 V	要求详细的ESD控制方法

重要注解：这些被提议的具有基本ESD控制方法的HBM防护标准能够充分地保证高于30V的MM防护能力