White Paper 3
System Level ESD
Part I: Common Misconceptions and Recommended Basic Approaches

Executive Summary

Industry Council on ESD Target Levels

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工业协会关于 ESD 目标级别

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About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies. *In terms of product shipped, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies, and over 70% of the total volume of product shipped by the top 20 companies, as reported in the EE Times issue of August 6, 2007.*

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Terry Welsher, Dangelmayer Associates	

Translation to Mandarin

Zhixin Wang, Synaptics Inc
Yihong Yang, Synaptics Inc

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Editors:
Robert Ashton, ON Semiconductor
Brett Carn, Intel Corporation

Authors:
Robert Ashton, ON Semiconductor
Jon Barth, Barth Electronics
Patrice Besse, Freescale Semiconductor
Jonathan Brodsky, Texas Instruments
Stephanie Dournelle, ST Microelectronics
Charvaka Duvvury, Texas Instruments
Reinhold Gaertner, Infineon Technologies
Robert Gauthier, IBM
Harald Gossner, Infineon Technologies
Leo G. Henry, ESD/TLP Consulting
Mike Hopkins, EM Test USA
John Kinnear, IBM
David Klein, IDT
Tom Meuse, Thermo Fischer Scientific
James W. Miller, Freescale Semiconductor
Tim Maloney, Intel Corporation
Guido Notermans, ST-Ericsson
Nate Peachey, RFMD
Wolfgang Reinprecht, Austria Microsystems
Alan Righter, Analog Devices
Theo Smedes, NXP Semiconductors
Pasi Tamminen, Nokia
Benjamin Van Camp, Sofics
Terry Welsher, Dangelmayer Associates

Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system level ESD issues, the Council has now expanded its mission to directly address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system level ESD design. To ensure a broad range of perspectives the Council has expanded its roster of Members and Associates to include OEMs as well as experts in system level ESD design and test.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing this information, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Executive Summary

Our intention in this document is to work with the OEMs, and with their participation and feedback, eliminate misconceptions about system level ESD while jointly addressing the design of robust ESD systems. **Our aim is to bring suppliers and customers together for a common purpose towards the development of ESD robust systems.**
There is a growing awareness in the electronics OEM community that system level ESD robustness is an important requirement for reliable products. System level ESD testing is today applied to a wider range of products than ever before. Designing ESD robust systems can be very challenging, especially for systems which integrate advanced technology integrated circuit (IC) components. For most system designers, ESD protection strategy and design efficiency are only dealt with in an ad hoc manner. Many of the most severe system level ESD design problems can be traced to misconceptions between system designers (OEMs) and their IC providers. Adopting a consolidated approach to system level ESD design, which addresses these misconceptions, will be key to future success in building ESD robust systems.

This White Paper serves three important purposes. First it provides an overview of system level ESD test and design challenges in the industry today. Second, it identifies and characterizes the primary misconceptions mentioned above. Third, it introduces a new co-design approach called "System-Efficient ESD Design" (SEED) that promotes a common OEM/IC provider understanding of the correct system level ESD needs.

This white paper is the first part of a two part document. Part I will primarily address hard failures characterized by physical damage to a system. "Soft failures", in which the system's operation is upset but without physical damage, is also critical and predominant in many cases. The same soft failures can also refer to system upsets involving recoverable damage to system malfunction. However, these issues are out of the scope of the current document and will be dealt with in detail in Part II of this white paper. Although EOS failures can result from a system failure our focus here is not intended to cover other types of EOS failures that can come from mishandling, etc.

Background and Purpose (Chapter 1**)**

There is a critical need in the IC industry to directly address the growing division in the understanding of system level ESD between system/board designers and their IC providers. The true nature of system ESD reliability, especially in light of the rapid advances in the IC industry, requires a comprehensive examination. There are three aspects to this study.

1. Understanding of the nature of system failures which can be either "hard" or "soft." Hard failures are typically related to physical damage which is not recoverable, while soft failures describe a system upset or malfunction including recoverable damage.

2. Clarification of misconceptions that often lead to an inefficient approach to system level ESD design. For example, the commonly held belief that IC level ESD specifications (such as the HBM) can ensure robust system ESD design.

执行摘要

本文档的目的是与OEM厂商合作，获得它们对系统级ESD的期望与反馈，消除对系统级ESD的误解，共同解决强健的ESD系统设计问题。**我们的目的是集合供应商与客户，以开发具有强健ESD性能的系统作为共同的目标。**

系统级ESD的鲁棒性对于可靠的产品来说是一项很重要的要求，这一点已经逐渐成为电子OEM界的共识。相比较以前，现在更多的产品已经采用系统级ESD测试。设计具有强健ESD性能的系统是可以具有挑战性的，尤其是对于那些集成了先进制程集成电路（IC）元件的系统而言。对于大部分设计师而言，他们仅仅会以一种特殊的方式来处理ESD保护策略与设计效能。许多的很严重系统级ESD设计问题都可以追溯到系统设计师（OEMs）与他们的IC供应商之间的误解。采用统一的方法来进行系统级ESD的设计，解决两者之间的误解，将成为未来构建具有强健ESD性能的系统的关键。

本白皮书具有三个重要的目的。第一，它总结了目前工业界系统级ESD测试与设计的挑战性。第二，它识别与描述了上述的主要误解。第三，它提出了一个崭新的合作设计方法，名字为“高效系统级ESD设计（SEED）”。这个方法推动一个OEM与IC供应商之间关于正确系统级ESD需求的共识。

完整的文档具有两部分，而本白皮书是第一部分。第一部分主要阐述通过系统物理破坏表征而来的硬失效问题。“软失效”会扰乱系统正常运作，但不会造成系统的物理破坏，并且在很多例子中都是关键的和主要的。同样的软失效还可以指系统的扰乱，包括在系统故障时可以恢复的破坏。然而，这些问题已经超出本文档的范畴，而它们将在白皮书的第二部分进行详细的探讨。尽管EOS失效可以来源于系统失效，但我们在这里的重心并不涉及可能来源于误操作等其它类型的EOS失效。

背景与目的（第一章）

IC工业界迫切需要解决系统/板级设计师与他们的IC供应商之间对于系统级ESD的理解的分歧。系统级ESD可靠性的真正本质，尤其是在快速发展的IC工业，需要一个全面的考查。这项研究具有三个方面：

1. 理解系统失效中的本质，其可以是“硬失效”或者“软失效”。“硬失效”一般指不可恢复的物理硬件破损，而“软失效”是指系统干扰或者包含可以恢复的故障。
2. 澄清经常导致低效的系统级ESD设计的误解。比如，大家普遍认为的IC级ESD技术参数（比如HBM）可以保证强健的系统级ESD设计。

3. Definition of the whole system in the context of which portions of the IC components on a PCB are involved in the protection strategy. For instance, identifying the external (interface) pins that would be in the critical path of an ESD event and require careful design strategy, versus internal (non-interface) pins which are not as affected and may not require special attention during system design. However, while differentiating internal versus external pins, it must be noted that issues associated with inter- chip pins are also important. Part I will address only direct stress issues while the indirect effects coming in from coupling will be dealt with in more detail in Part II of the white paper. OEM concerns about failures of products in manufacturing and in the field have often led system manufacturers to take their own initiatives, whether effective or not, or to make various demands from the IC suppliers, whether justified or not in each and every case.

Test Methods and Their Field of Application (Chapter 2)

The existing system level ESD test methods and their field of application are discussed in great detail. First, it is noted that IEC 61000-4 is a set of EMC test standards which includes the system level ESD test method, IEC 61000-4-2. It specifies calibration waveforms, procedures and stress points for executing ESD tests on systems. The standard clearly excludes several locations and situations. The standard also explicitly encourages committees, manufacturers and users to derive standards from IEC 61000-4-2 for specific applications. We discuss the IEC 61000-4-2 ESD procedure and present several examples of application specific interpretations. We also discuss examples where people have derived practices to stress locations or situations that were excluded in the IEC 61000-4-2. The most extreme example is the application of system level ESD stress directly to ICs. Several approaches for this application are discussed.

Proven System Level Fails (Chapter 3)

Here we address proven system level failures from actual case studies, examples of both field returns and failures generated during qualification testing. Field failures generated during a system operation are not easy to resolve as to whether they come from ESD or EOS types of events. If a failure is detected, a thorough root cause analysis would be necessary to establish the cause. The examples given try to ascertain whether the failures are related to the device HBM or CDM robustness as well as the type of external protection device implemented and their effectiveness in protecting against an IEC ESD event. By classifying the failure types and establishing the failure statistics a better insight into the system failure phenomena will be obtained. In this document we highlight how system problems are typically solved.

OEM System Level ESD Needs and Expectations (Chapter 4)

Next, we discuss the needs and expectations that OEMs have from their IC suppliers such that the OEM can design products that will not be physically damaged or have their operation upset by ESD stress. Three hypothetical design paths for ESD robust systems are outlined:

1. Design with ESD robust ICs in which ESD is not a concern.
2. Design with a combination of ESD robust and non-robust products, but with clear guidelines, procedures and tools available (i.e., the SEED approach).
3. Design with a combination of ESD robust and non-robust ICs, but without clear ESD

guidelines, procedures and tools available to the system designer.

3. 根据在PCB上哪一个部分的IC元件须要归入保护策略来定义完整的系统。比如，区分将会在ESD放电时成为关键放电路径并须要仔细的设计策略的外部（界面）管脚，与不会受到影响并在系统设计时可能不需要特别注意的内部（非界面）管脚。然而，在区分内部与外部管脚时，必须强调的是，关于芯片与芯片之间的管脚也是很重要的。第一部分将会阐述直接放电的问题，而关于来源于耦合的非直接放电效应将在在白皮书的第二部分进行探讨。OEM厂商担心产品在生产与现场的失效问题，这也经常导致系统生厂商采取主动措施，不管其是否有效，又或者向IC供应商提出各种要求，不管这些要求是否通过每一个例子的验证。

测试方法与它们的现场应用（第二章）

本文档将着重讨论现有的系统级ESD测试方法，以及它们的现场应用。第一，须要强调的是IEC 61000-4-2是EMC测试方法的一部分，它包括了IEC 61000-4-2系统级测试方法。它详细说明了在系统上执行ESD测试时的校验波形，步骤与放电地点。这个标准明确地排除了若干地点与情况。同时，这个标准也明确地建议委员会，生厂商，与用户根据特殊的应用要求，从IEC 61000-4-2 来获取标准。我们会讨论IEC 61000-4-2的测试步骤，以及通过若干特殊应用的例子来解释。我们还会讨论若干例子，包括人们自行推导出但被IEC 61000-4-2标准排除的放电地点与情形。其中最极端的例子是使用系统级ESD对IC进行直接放电。我们将会讨论关于这个应用的若干方法。

经过证明的系统级失效（第三章）

在这里我们会阐述通过实际例子来证明的系统级失效，包括现场返回以及在校验测试时产生的失效。就失效是来源于 ESD 还是 EOS 类型的放电而言，在系统运作时产生的现场失效都是不容易解决的。如果检测到失效，则需要彻底的分析来寻找失效的根本原因。这里给出的例子尝试去查明失效是否与以下因素有关联：器件的 HBM 或 CDM 鲁棒性，外部保护器件的类型以及它们保护 IEC ESD 放电的效能。通过分类失效类型与建立失效的统计数据，我们可以更好地洞悉系统失效的现象。在本文档，我们会突出系统问题是如何解决的。

OEM对系统级ESD的需要与期望（第四章）

下一步，我们会讨论OEM厂商对于它们的IC供应商的需要与期望，从而OEM厂商能够设计不会被ESD放电导致物理破坏或者运作干扰的产品。这里概述三个有助于系统级ESD鲁棒性的假想设计路径：

1. 设计具有强健ESD性能的IC，使其不再被ESD问题困扰。
2. 设计具有强健与一般ESD性能组合的产品，但需要有清晰的指引，步骤与工具（比如，SEED方法）。
3. 设计具有强健与一般ESD性能组合的产品，但不需要清晰的ESD指引，步骤与工具。

As desirable as path 1 may be, it is typically unrealistic. Instead we describe the information and tools needed to move from path 3 (which often describes ESD system design today) to path 2, which is a realistic goal for the future.

Lack of Correlation between HBM/CDM and IEC 61000-4-2 (Chapter 5)

There is a common assumption in the system design community that the IC level HBM has relevance to ESD performance at the system level. This assumption persists because of a lack of understanding of the differences between the models and a lack of actual data to make valid comparisons. Figure 1 contains data where some IC and system level information is available for a rough comparison. Details of the tests which were done to generate this data are not available as is often the case. However, this limited data serves to suggest that correlation is not likely (though not disproven by such a small data set). In this section, this lack of correlation and why this is expected is discussed. The relationship between IC ESD models (HBM and CDM) and the IEC 61000-4-2 is further explored. By comparing required waveform characteristics, equivalent circuit models and practical realization issues, it is demonstrated that these IC models cannot be expected to correlate to system level ESD. Actual test comparisons that have been reported in the literature are reviewed. While emphasis is placed on common HBM and CDM tests, comparisons to other emerging models are discussed. These include cable discharge events (CDE), human metal model (HMM), transient-induced latch-up, extended pulse length transmission line pulse (TLP) and charge-board events (CBE).

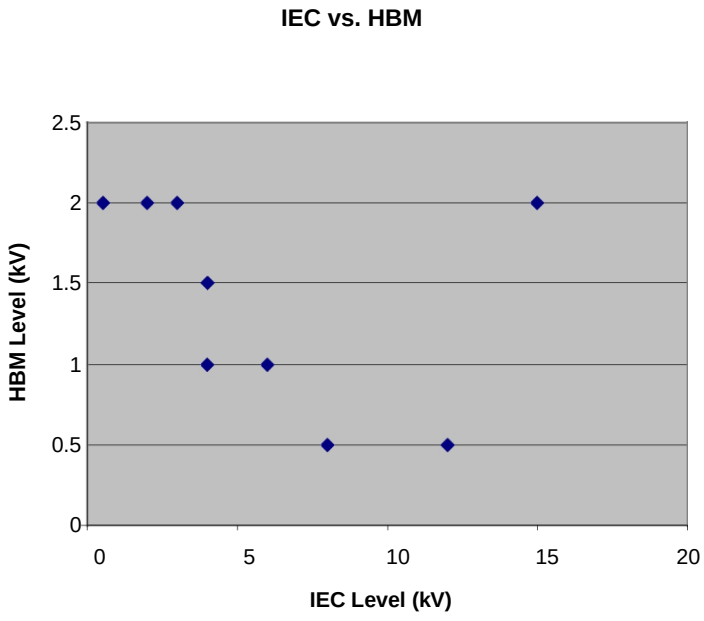

Figure 1: Comparison of IC ESD and System ESD

路径一可能是大家最希望的，但是它一般是不实际的。相反，我们会描述从路径3（目前常称作ESD系统设计）提升到路径2所需要的信息与工具，这也是将来切实可行的目标。

缺乏HBM/CDM与IEC 61000-4-2之间的关联（第五章）

在系统设计领域，大家都普遍假设IC级HBM性能会与系统级ESD性能有所关联。这个假设一直存在是因为缺乏对于模型之间差异的理解，以及缺乏可用作有效比较的真实数据。图1包含了一些IC与系统级信息的数据，它们可用作粗略的比较。用于产生这些数据的测试细节经常是缺乏的。然而，这些有限的数据建议这种关联是不可能的（尽管这一小组数据也没有反驳）。在这一节，我们将讨论为什么会缺少这种关联，同时为什么这个在预期之内的。我们将进一步探讨IC的ESD模型（HBM与CDM）与IEC 61000-4-2之间的关系。通过比较所需的波形特征，等效电路模型与实际的实现问题，将证明这些IC模型是不能够与系统级ESD有所关联的。我们会回顾文献中的真实测试比较。虽然重点是放在一般的普遍的HBM与CDM测试，但是也会讨论与其它新兴的模型的比较。这包括电缆放电模型（CDE），人体金属模型（HMM），瞬变导致的闩锁效应，延展波宽的传输线脉冲（TLP），和充电板模型（CBE）。

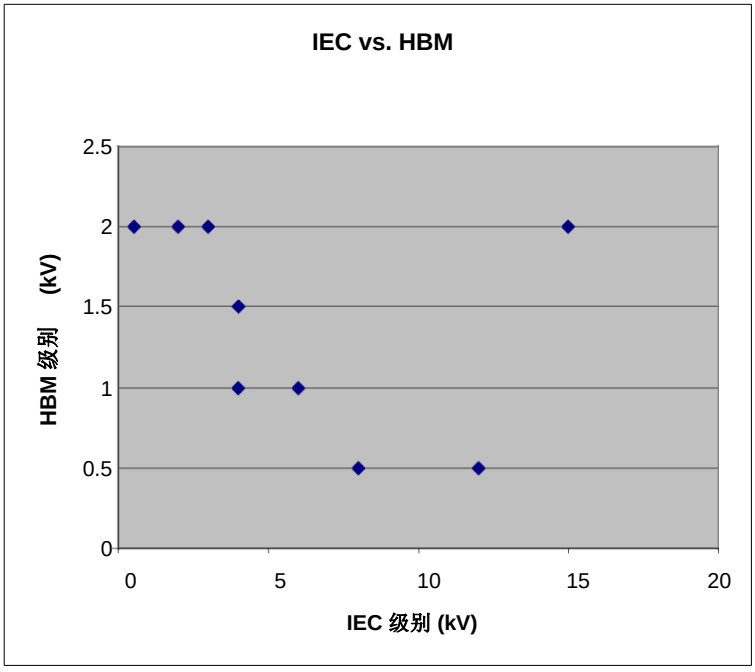

图1：IC的ESD与系统ESD的比较

Relationship between IC Protection Design and System Robustness (Chapter 6)

Finally, we discuss the relation between IC protection design and system design robustness to avoid physical damage. Requirements and constraints of IC level ESD protection design are presented. Starting by highlighting misconceptions in equating IC ESD robustness, like HBM according to JEDEC with system level ESD robustness, a detailed discussion of various system level ESD protection concepts (both on-chip and on-board) is performed. On-board and on-chip protection circuits interact and can even compete. This requires a careful evaluation of the relevant parameters. Using analysis methods like transmission line pulsing, which reflect essential characteristics of IC pins and board protection elements, a systematic design of system level ESD protection can be developed. Essentially the comprehensive on-chip/ on-board protection co-design methodology, referred to as System- Efficient ESD Design (SEED), enables an optimum protection design from building blocks that provide a clear advantage to today's trial and error approach. The generic SEED concept is illustrated in Figure 2. The benefits are discussed for some examples like USB, CAN bus and antenna interfaces.

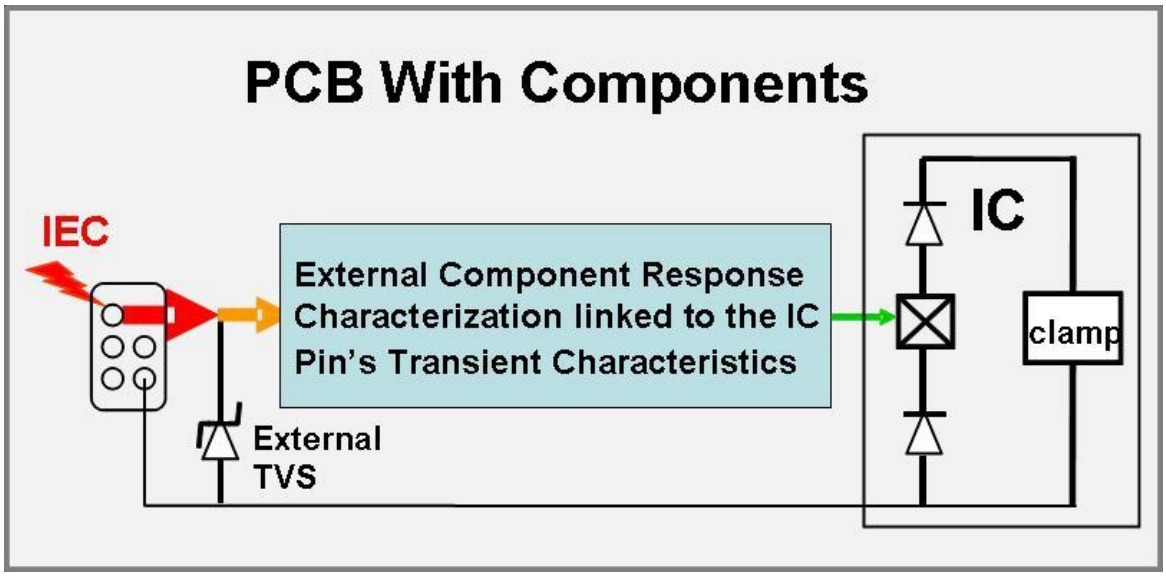

Figure 2: System-Efficient ESD Design concept requires careful consideration of interaction between the PCB protection and the IC pin transient characteristics.

Cost of System Protection

Assessing the cost of design, it becomes clear that a co-design approach is superior to design concepts relying on excessive ESD robustness requirements at the IC level. We show a path that illustrates how IC suppliers and system manufacturers can cooperate in the future, with both parties benefiting from this approach to achieving required system robustness without overly specified IC level ESD targets and performance restrictions.

IC保护设计与系统鲁棒性之间的关系（第六章）

最后，我们将讨论IC保护设计与系统设计鲁棒性之间的关系来避免物理破坏。IC级ESD保护设计的要求与限制将会被展现。首先从展现把IC的ESD鲁棒性，比如JEDEC的HBM，等效到系统级ESD的鲁棒性这一误解开始，然后详细讨论不同的系统级ESD保护概念（片上与板上）。板上与片上的保护电路的交互甚至可以互相竞争。这要求对相关联的参数作仔细的评估。使用分析方法，比如可以反映IC管脚与板级保护元件的传输线脉冲，可以开发出系统级ESD保护的系统设计。本质上，全面的片上/板上共同保护设计，称作高效系统级ESD设计（SEED），能够通过构建比目前尝试与失败的办法更有利的模块来实现优化保护设计的方法。图2显示了一般的SEED概念。它的好处将通过一些例子，比如USB，CAN总线和天线界面来讨论。

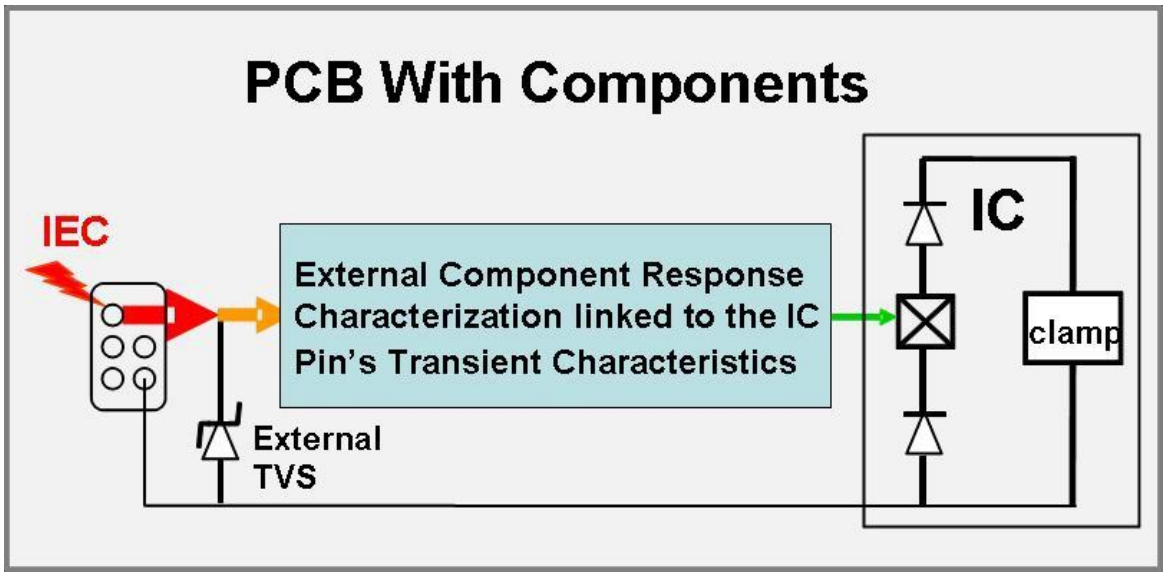

图2：高效系统级ESD设计概念需要对PCB保护与IC管脚瞬变特性的交互作用作仔细的考量

系统保护的成本

关于设计的成本，很明显共同设计的方法是优于过分要求IC级ESD鲁棒性的方法。我们会展现IC供应商与系统生厂商将来如何合作，同时双方均可从中获利，在不过分要求IC级ESD目标与性能限制的情况下达到所要求的系统级鲁棒性。