White Paper 3
System Level ESD

Part II: Implementation of Effective ESD Robust Designs

Executive Summary

Industry Council on ESD Target Levels

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工业协会关于 ESD 目标级别

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Abstract

This document (White Paper 3 Part II) is the second of two Electrostatic Discharge (ESD) Industry Council white papers dealing with System Level ESD.

In Part I, the misconceptions common in the understanding of system level ESD between supplier and original equipment manufacturer (OEM) were identified, and a novel ESD component / system co-design approach called system efficient ESD design (SEED) was described. The SEED approach is a comprehensive ESD design strategy for system interfaces to prevent hard (permanent) failures. In Part II we expand this comprehensive analysis of system ESD understanding to categorize all known system ESD failure types, and describe new detection techniques, models, and improvements in design for system robustness. Part II also expands this SEED co-design approach to include additional hard / soft failure cases internal to the system.

Part II begins with an overview of system ESD stress application methods and introduces new system diagnosis methods to detect weak ESD failure areas leading to hard or soft failures, and provides a "cost vs. performance vs. robustness" analysis of present-day state-of-the-art EMC/EMI design prevention methods that have been developed to prevent system level ESD failure. It follows with an expansion of SEED failure classifications to cover a combination of hard (permanent) and/or soft (resettable) system failures and stresses which could cause these errors, and describes cases where the SEED co-design approach can be expanded to provide additional benefits to system ESD design. System design simulation tools are described in the context of their potential improvements to simulating system level ESD stress and failure modes. Application-specific industry system ESD test methods are then described in the context of their ability to reveal hard and soft failure modes from actual system deployment. Finally, a technology roadmap of the system design components is described, including IC technology and related circuit speeds, automotive electronics, packaging technology, system / board interconnect technology and ESD protection materials, illustrating continuing challenges for system ESD design improvement.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies. In terms of semiconductor market leaders, the member IC manufacturing companies represent 8 of the top 10 companies, and 12 of the top 20 companies as reported in the EE Times issue of November 9, 2010.

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ChangSu Kim, Samsung	Michael Wu, TSMC
Han-Gu Kim, Samsung	MyoungJu.Yu, Amkor
Marcus Koh, Everfeed	

This document is assembled from reference material available through various public domains as listed below:

The Industry Council on ESD
http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association
http://www.esda.org/

JEDEC – Under Publication JEP162
http://www.jedec.org/

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Editors:
Brett Carn, Intel Corporation
Terry Welsher, Dangelmayer Associates

Authors:
Robert Ashton, ON Semiconductor
Jon Barth, Barth Electronics
Patrice Besse, Freescale Semiconductor
Jeff Dunnihoo, Pragma Designs, Inc
Charvaka Duvvury, Texas Instruments
David Eppes, AMD
Harald Gossner, Intel Corporation
Leo G. Henry, ESD/TLP Consulting
Masamitsu Honda, Impulse Physics Laboratory
Mike Hopkins, Amber Precision Instruments
Marty Johnson, Texas Instruments
David Johnsson, Intel Corporation
David Klein, Freescale Semiconductor
Tom Meuse, Thermo Fischer Scientific
Tim Maloney, Intel Corporation
Guido Notermans, ST-Ericsson
Ghery Pettit, Intel Corporation
David Pommerenke, Missouri University of Science & Technology
Alan Righter, Analog Devices
Wolfgang Reinprecht, Austria Microsystems
Pasi Tamminen, Nokia
Matti Uusimaki, Nokia
Benjamin Van Camp, SOFICS
Vesselin Vassilev, Novorell
Joost Willemen, Infineon Technologies

Translation to Mandarin
Zhixin Wang, Synaptics Inc
Yihong Yang, Synaptics Inc

Executive Summary

Overview

White Paper 3 Part II, while establishing the complex nature of system level ESD, proposes that an **efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level**. This objective requires an appropriate characterization of the components and a methodology to assess the entire system using simulation data. This is applicable to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)). This type of systematic approach is long overdue and represents an advanced design approach which replaces the misconception, as discussed in detail in White Paper 3 Part I, that a system will be sufficiently robust if all components exceed a certain ESD level.

In the first step, a method for categorizing the failure types has been introduced. An advanced characterization and simulation approach is discussed through examples. However, a full design flow cannot be established without **a common effort across the electronic industry involving IC suppliers, suppliers of discrete protection components and original equipment manufacturers (OEMs) as well as tool vendors**. This paper identifies existing tools with both simulations and scanning techniques that are applicable for this purpose and calls out fields for further development.

Equally important is the notion that **efficient system ESD design can ideally be achieved by improved communication between the IC supplier, the OEM and the system builder**. As technologies advance even further, and as systems become more complex under various applications, this shared responsibility is expected to gradually shift more towards system design expertise.

Understanding Component to System ESD

Towards achieving the goals mentioned above, it is first important to decouple the component ESD requirements from system level ESD design. White Papers 1 and 2 established that component electrostatic discharge (ESD) levels can be safely reduced to practical levels with basic ESD control methods that are mandatory in every production area. We have also established that these ESD target levels enable fabrication of integrated circuits (ICs) with on-time delivery (in billions of units) for electronic systems in consumer applications with high circuit performance. The general perception has been that component ESD (for example, human body model (HBM)) is a prerequisite for good system level ESD robustness. But this misconception once again needs to be clarified, as shown below in Figure 1, **system level ESD and component ESD are not correlated with each other.**

执行摘要

综述

白皮书 3 第二部分建议在建立复杂的系统级 ESD 时，要在系统级分析不同元件在 ESD 情况下的交互作用，才能得到有效的 ESD 设计。这个目标要求有各个元件的合适的特性描述，以及使用仿真数据来分析整个系统的研究方法。这适用于不同种类的系统失效（比如，硬失效，软失效，以及电磁干扰（EMI））。这种系统级方法是早应该被采用的，同时它也代表着一种先进的设计方法，可以消除如果所有元件都超过一定的 ESD 等级则系统就具有足够强健的误解，这个误解在白皮书 3 第一部分有详细讨论。

首先，会介绍一种失效类型的分类方法。然后透过例子来讨论一种先进的特性描述与仿真方法。然而，建立完整的设计流程需要**电子工业之间的交叉合作，包括IC供应商，分立保护元件供应商，原始设备制造商（OEMs），以及工具供应商。**本文将对已有的、可用于仿真和扫描技术的工具进行鉴定，并唤起现场的进一步开发。

通过加强 IC 供应商，原始设备制造商，以及系统构建者之间的沟通可以快速实现有效的系统级 ESD 设计这一概念也是同等重要的。随着制程的进一步推进，以及系统在不同应用下变得更加复杂，预计这个分担的责任将逐步转移至系统设计的专业知识。

理解元件到系统级ESD

在实现上述目标的过程中，首先最重要的是把元件级ESD要求从系统级ESD设计中分离出来。白皮书1和2指明，在每一个生产区域，若基本的ESD控制方法是强制要求的话，元件级静电放电（ESD）等级可以安全地降低至实用的水平。同时，我们指明，这些ESD目标等级允许为消费电子系统生产与及时交付（十亿级单位量）具有高电路性能的集成电路（ICs）。一般的看法认为，各个元件级ESD（比如，人体放电模型（HBM））是良好的系统级ESD鲁棒性的先决条件。但是这里必须再次澄清这个误解，如图1所示，**系统级ESD与元件级ESD之间并没有关联**。

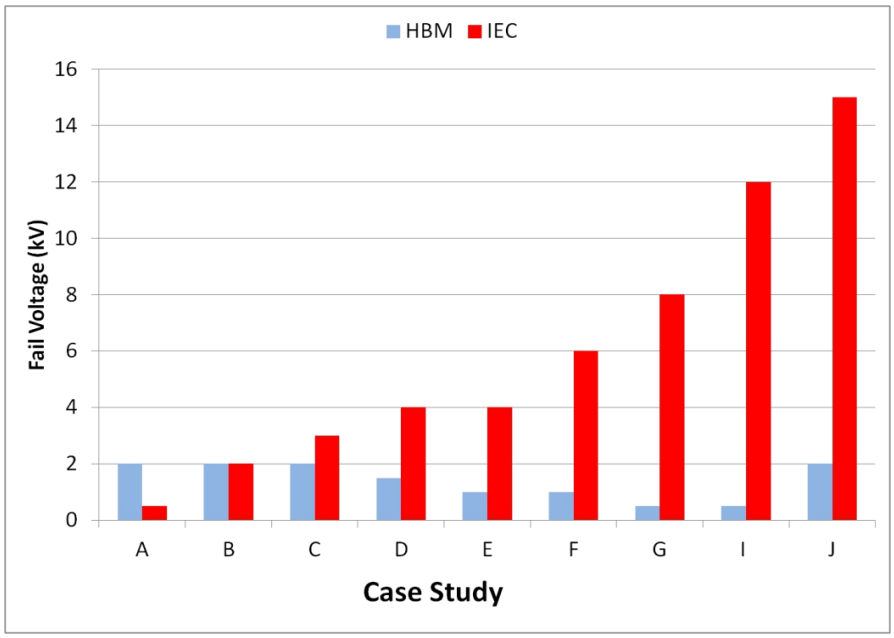

Figure 1: Comparison of IC level and system level ESD failure threshold of various systems (A-J) showing that HBM protection is not related to System level ESD robustness

In fact, at the system level, ESD robustness is a much more complex issue requiring a deeper understanding to address the ESD protection requirements for electronic systems such as laptops, cell phones, printers and home computers. These system complexities come about as a result of protecting the external interfaces, such as the universal serial bus (USB), to the outside world. Such systems, after encountering the more severe ESD pulses defined by the IEC standard, can lead to hard or soft failures. As introduced in White Paper 3 Part I, the basic version of system-efficient ESD design (SEED) addresses **hard failures** related to IC pins with a direct external interface, **soft failures,** which are more frequently reported, are challenging to understand and overcome. In this latter case, addressing soft failures requires an extension of the SEED approach to other failure mechanisms that include latch-up and EMI effects. In this document, the steps to categorize the different failure mechanisms, and the appropriate characterization and simulation methodologies, are identified through various forms of **Advanced SEED**.

Communication and Strategy

This white paper documents a rigorous approach to describing **the challenges related to all categories of system level ESD failures** that can arise from energy injection due to the IEC contact pulse stress, as well as from electromagnetic compatibility (EMC) and EMI effects. To classify these fails and to provide a common terminology, three categories of fails have been introduced:

- SEED Category 1 (physical damage due to pulse energy)
- SEED Category 2 (damage or interference of function due to transient latch-up)
- SEED Category 3 (interference of function by noise or bursts on supply net and signal lines)

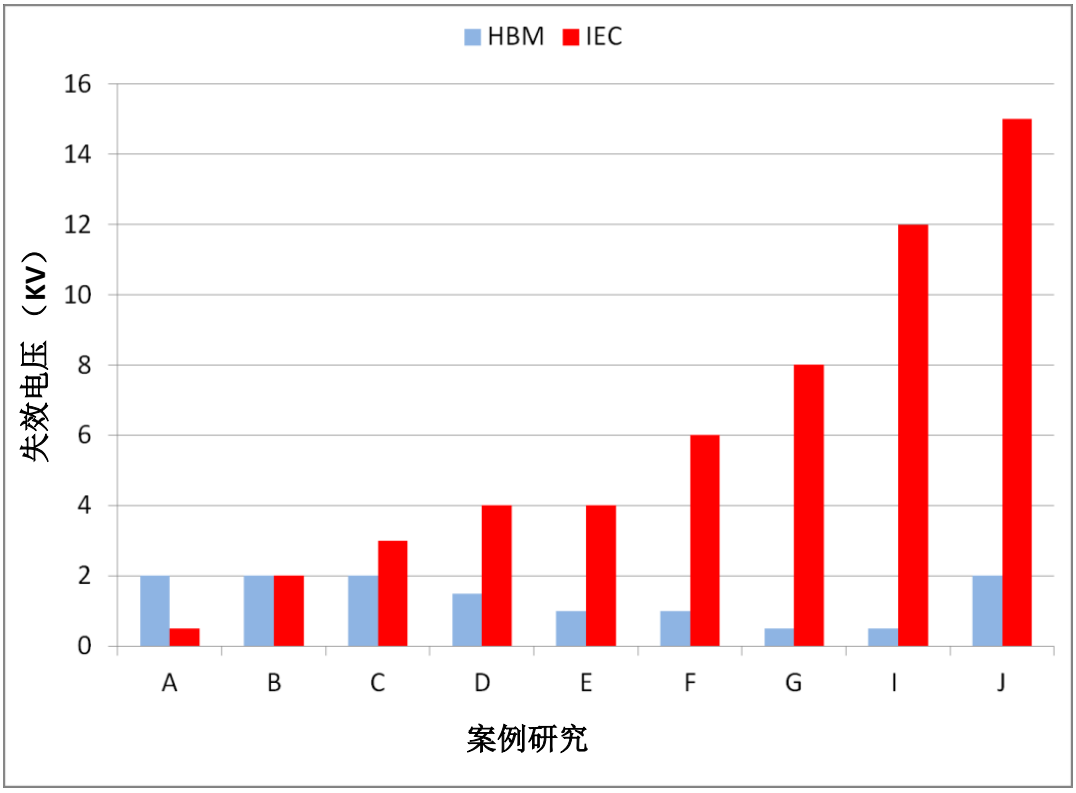

图1：不同系统（A-J）的IC级与系统级ESD失效阈值之间的比较，表明HBM保护与系统级ESD鲁棒性之间并无关联

事实上，在系统级，ESD鲁棒性是一个更加复杂的问题，其要求更加深入的理解来达到电子系统ESD保护的要求，比如笔记本电脑，手机，打印机，以及家用电脑。这些系统复杂性来源于对外围界面的保护，比如通用串行总线（USB）到外部世界。在遇到IEC标准定义的更加严重的ESD波形后，这些系统可能导致硬失效或软失效。正如白皮书3第一部分介绍，基本版本的高效系统级ESD设计（SEED）解决带有直接外部界面的IC管脚的**硬失效**，而对于更多反馈的**软失效**，理解和克服则是具有挑战性的。对于后者而言，解决软失效问题需要SEED方法的延伸至其它失效机理，包括闩锁效应和电磁干扰效应。本文档将通过不同类型的**先进的SEED**来阐明不同失效机理的分类，以及适当的测试与仿真方法。

交流与策略

这份白皮书记录了一个严格的方法来描述**与所有类型的系统级ESD失效都相关的挑战性**，这些失效来源于IEC接触波形放电，以及电磁兼容（EMC）与电磁干扰效应所形成的能量注入。要区分这些失效并提供通用的术语，这里介绍三种失效的分类：

- SEED 分类 1（波形能量产生物理破坏）
- SEED 分类 2（瞬变闩锁效应产生的功能性破坏或干扰）
- SEED 分类 3（噪声产生的功能性干扰，或者电源和信号线的瞬爆）

Understanding these different categories of failures is an important part of addressing the appropriate solutions. Thus, one main objective is to close the existing communication gap between OEMs and IC providers by involving the expertise of both OEMs and system design experts. As a result, the completion of this second phase of White Paper 3 required the participation and contributions from world class experts on the art of system level ESD phenomena and protection techniques.

One of the challenges which remains elusive is the trade-off between cost, performance, robustness, and time-to-market. This white paper also addresses these issues, bringing forth a dialogue between the IC supplier, customer, and the system designer.

Implementation of Advanced Tools

White Paper 3 Part II specifically covers in detail **an overview of system ESD stress application methods, system diagnostic techniques to detect hard or soft failures, and the application of tools for susceptibility scanning.** For example, as illustrated in Figure 2, these types of advanced tools can be used to differentiate the characteristics of products and enable proper system protection methodology.

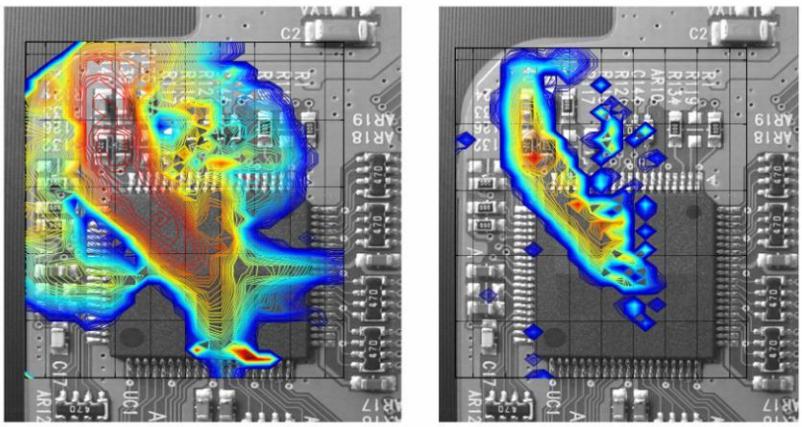

Figure 2: Susceptibility scanning using pulse techniques on Product A (left) and Product B (right) (Courtesy of Amber Precision Instruments)

Along the lines of communication and interaction, IC suppliers and system designers can share their knowledge of tools and their applications. For example, suppliers would provide a single definition, high quality model of their input/output (IO). Then OEMs would use analytical tools to integrate the IC's IO models into their system models for system level stress analysis. These tools will not reach their full potential unless the data they collect can be used within the standard design flow for an electronic system. For these to be effective, model files such as input/output buffer information specification (IBIS) and simulation programs with integrated circuit emphasis (SPICE), which describe the electrical properties of components, need to be enhanced to describe component behavior in the ESD range. Suppliers of components, ranging from integrated circuits to ESD protection components also need to characterize their products in the appropriate ESD range.

理解这些不同类型的失效是提出合适的解决方案的重要部分。因此，其中一个重要的目标，是通过引入 OEM 与系统设计专家的专业知识来消除 OEMs 与 IC 供应商之间的分歧。因此， 要完成白皮书 3 第二阶段，需要关于系统级 ESD 的现象与保护技术的世界级专家参与与贡献。

其中一个仍然难懂的挑战是成本，性能，鲁棒性，以及上市时间之间的权衡。本白皮书会提出这些问题，同时带来IC供应商，客户，以及系统设计师之间的对话。

先进工具的使用

白皮书3第二部分特别细节地涵盖了**综述，包括系统级ESD放电的应用方法，检测硬失效或软失效的系统诊断技术，以及易感性扫描工具的应用**。比如，如图2所示，这些先进工具可用于区分产品的特征，以及使合适的系统级保护方案成为可能。

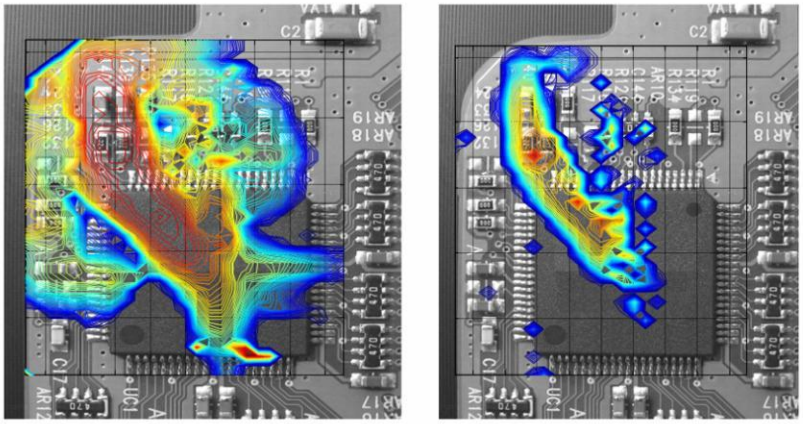

图2：在产品A（左）和产品B（右）上使用脉冲技术的易感性扫描（经由Amber Precision Instruments提供）

在沟通与交互的过程中，IC供应商与系统设计师可以分享他们关于工具的知识，以及它们的应用。比如，供应商可以提供统一的定义，输入/输出口（IO）缓冲器的高质量模型。OEMs可以使用分析工具把IC的IO模型集成到系统模型中进行系统级放电分析。当所收集的数据可以用于电子系统设计流程中的时候，这些工具才会发挥它们的最大潜能。为了使这些都有效果，需要增强模型文件对元件在ESD范围的行为描述，比如输入/输出缓冲器信息技术特征（IBIS），和描述元件电气特性的面向集成电路的仿真程序（SPICE）。元件的供应商，从集成电路到ESD保护元件，同样需要在适当的ESD范围内测试他们产品的特性。

Impact from the Technology Roadmap

Finally, we bring into focus that IC technology and related circuit speeds will increasingly have an impact on system designs. This roadmap will cover market segments ranging from information technology (IT), communications, automotive electronics, IC package technology development to advances in board and assembly technologies. **The cost of ESD must be considered along with all development and innovation; the industry must decide who should bear the cost of ESD design and its pressure on production schedules and time to market**

System level ESD will continue to be a challenge in the future. The dilemma of meeting technology demands for speed and performance will inevitably require either the development of more effective shielding or innovation of novel on-board protection solutions.

Conclusions

In summary, this white paper has pointed out the necessary framework required for comprehensive improvement in the first time success rate of ESD robust system designs. A number of helpful tools and techniques already exist. However, standardization between IC suppliers, PCB protection device suppliers and system designers requires common models, common methods and compatible simulation tools in order to meet the goal of better ESD design capability. **None of this will occur without a great deal of communication between EDA tool vendors, component suppliers and system designers.**

Finally, this document has provided a major step forward in identifying and understanding the technical issues. An important message to remember is that **the current focus on component ESD performance must shift towards improving system level ESD performance. That is, while minimum component ESD levels provide for safe component handling, the bulk of future research and development efforts should be directed towards system level ESD to reach a day when a high first pass success rate in system level ESD design is straightforward.**

技术路线图的影响

最后，我们会强调IC技术和相关的电路速度将会对系统设计产生越来越大的影响。这个路线图包括从信息技术（IT），通讯，汽车电子，IC封装技术开发，到先进电路板和组装技术的市场。**在所有开发与创新中，ESD的成本是必须考虑的；工业界必须决定由谁来承担ESD设计的成本，以及对产品计划和上市时间造成的压力。**

系统级ESD在将来仍然是一个挑战。满足技术对速度和性能的要求这一困境将不可避免地要求开发更有效的屏蔽，或者全新的板上保护方案的创新。

结论

总之，本白皮书指出了必要的框架来全面提升强健的ESD系统设计的首次成功几率。若干有用的工具和技术已经存在。然而， IC供应商，PCB保护器件供应商和系统设计师之间的标准化需要通用的模型，通用的方法，和兼容的仿真工具来实现更优的ESD设计能力这一目标。**只有通过EDA工具供应商，元件供应商，和系统设计师之间的大量沟通，这一目标才可实现。**

最后，本文档踏出了判别和理解这些技术问题的重要一步。有一条重要的信息要谨记，**就是目前对元件级 ESD 性能的关注必须向提升系统级 ESD 性能进行转移。也就是说，最低的元件级 ESD 等级提供安全的元件操作，未来研究与开发的努力主体应该转向系统级 ESD，直至有一天，系统级 ESD 设计能够直接简单地拥有很高的首次成功率。**