White Paper 4
Understanding Electrical Overstress - EOS

Executive Summary

Industry Council on ESD Target Levels

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Abstract

Damage signatures from Electrical Overstress (EOS) are the leading reported cause of returns in integrated circuits and systems that have failed during operation. Solutions to this problem are hindered by a prevailing misconception in the electronics industry that insufficient robustness to electrostatic discharge (ESD) is a primary cause of EOS. This document, White Paper 4, (WP) has been carefully compiled by the Industry Council on ESD Target Levels to foster a unified global understanding of what constitutes EOS and how EOS damage signatures can result from a wide variety of root causes.

The paper begins by outlining a brief history of EOS. It then presents the results of an industry-wide EOS survey. This survey gathered information on the types of EOS problems experienced by over 80 different companies, the relative importance of EOS to their overall business, and the methods assigned by these companies to address EOS issues. The survey provides a combined picture from which a more comprehensive definition of EOS can be made. The numerous categories and sub-categories of EOS root causes are explored in an attempt to understand how to create better specifications which will reduce their occurrence. In addition to the survey results, this paper studies many field returns with EOS damage signatures to establish the underlying root causes of damage and offers the respective identified solutions.

The survey and the case studies both show that successful failure analysis (FA) depends on careful communication between customer and supplier from the time a failure occurs until its cause has been discovered. Detailed investigation into manufacturing and handling processes is often necessary to accurately identify the root cause. This paper outlines a basic summery of the typical process flow for component electrical failure analysis.

The key point is that EOS issues can be mitigated when the proper understanding of IC design, factory and field environments, and system implementation is combined with effective communication across all these areas.

Purpose

This purpose of this white paper will be introduce a new perspective about EOS to the electronics industry. As failures exhibiting EOS damage are commonly experienced in the industry, and these severe overstress events are a factor in the damage of many products, the intent of the white paper is to clarify what EOS really is and how it can be mitigated once it is properly comprehended. It is very clear that EOS is predominantly a matter of what customers do with devices, and in which applications the semiconductor specifications are exceeded causing destruction of the device. This white paper will describe those phenomena and explain the most important facts so that the involved partners in the industry have the opportunity to understand and recognize helpful steps for analysis and avoidance of EOS events.

In view of the above, we define EOS in terms of its impact inside applications. We focus on exceedance of specifications but not on how an exact specification was originally created. We focus instead on when and how the specifications are exceeded to cause EOS damage.

It is intended that this document be disseminated throughout the semiconductor industry for the benefit of those persons whose positions are concerned with the real nature of EOS. It is intended to serve as a foundational reference document for existing and future technologies.

Additional Motivation

A key finding from the Council's investigation is that component level ESD specifications and robustness have at most a minimal role in leading to an EOS condition or causing returns that exhibit EOS damage. While relating ESD scenarios to EOS, the document explicitly emphasizes the non-correlation between EOS return rates and Component ESD Target Levels. This is fully in line with what has been established in the Industry Council's white papers published as JEDEC documents JEP155 and JEP157.

About the Industry Council on ESD Target Levels

The Council was formed in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, original equipment manufacturers (OEMs), ESD tester manufacturers, ESD consultants and ESD intellectual property (IP) companies.

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Mission Statement

The Industry Council on ESD Target Levels was founded to review the ESD robustness requirements of modern IC products in order to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by advanced process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels as well as guidelines for various EOS and ESD topics. The Council Members and Associates promote these recommended targets and guidelines for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group associated with JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, as well as the member organizations, while providing this information, do not assume any liability or obligations.

This document is assembled from reference material available through various public domains as listed below:

The Industry Council on ESD
http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association
http://www.esda.org/

JEDEC – Under Publication JEP174
http://www.jedec.org/

Executive Summary

In this summary the Industry Council will address the most important electrical overstress (EOS) issues and conclusions of White Paper 4. Further details can be found in the various chapters of the document.

Traditional Perceptions of EOS

Through the years, a high incidence of failures exhibiting EOS damage has been reported in most market segments of electronics and related industries, such as the automotive industry. This damage has often been mislabeled as "EOS Failure", implying that these malfunctions are solely a result of a phenomenon or stress called EOS. Understanding EOS as a "stress" has led many customers to incorrectly assume a device experiencing EOS is "weak". This misperception has led to requests to "improve" a device in regards to EOS.

Another incorrect assumption has been that EOS can be avoided by making devices more ESD robust to both the human body model (HBM) and the charged device model (CDM). This misconception has been addressed in JEDEC publications JEP155 [1] and JEP157 [2] where it is convincingly shown that the incidence of EOS is independent of the level of HBM and CDM robustness.

Industry Council Worldwide Survey

In preparation for this white paper, the Industry Council conducted a worldwide survey of the electronics industry concerning EOS. Results confirmed the long held view that EOS is consistently one of the "high bars" on product failure Pareto charts. Looking at the EOS survey, respondents reported greater than 20% of total failures being EOS-related or 30% of total electrical failures being EOS-related, making EOS the largest bar on the Pareto chart of that responder's known causes of returns. One glaring revelation was the critical need for a better industry-wide understanding of EOS to address its issues.

Looking at the EOS survey further, misapplication (powered handling) stands out as the highest cause of EOS damage, with over 40% of respondents indicating EOS damage which occurred in the field as the most common location. Damage signatures associated with EOS often can involve package and silicon damage and are more extensive in a product than failure signatures resulting from events in the measurable ESD regimes. The main findings of the EOS Survey were:

1. **Powered Handling**: This stands out as the most widely reported root cause, involving a significant (over 20%) percentage of reported returns exhibiting EOS damage. Powered handling can include overvoltage, improper insertion, power supply sequencing, and incorrect biasing during use.

2. **Absolute Maximum Rating (AMR):** A number of returns exhibiting EOS damage were attributed to applied voltages exceeding the specified AMR voltage, indicating that incomplete or unclear maximum ratings may be an issue and that AMR characterization and improved AMR information on the datasheets is important to minimize the risk of EOS.

执行摘要

在本摘要中，工业协会将概述白皮书4中的电气过应力（EOS）最重要问题及结论。更多细节请参照文档中各章节的内容。

EOS 的传统认知

多年来，EOS 损坏的高失效率在电子领域的大多数市场分区，以及相关工业比如汽车工业，均有所报告。此类损坏通常被误标为“EOS 失效”，暗指此类机能失常单单是 EOS 的现象或应力的所导致的结果。EOS 被理解为“应力”使得很多客户误认为经历 EOS 的器件设备是性能比较“弱”。此误解导致了对“改善”器件 EOS 性能的需求。

另一个错误假设认为可以通过加强器件 ESD 性能的人体模型（HBM）及器件充电模型（CDM）来避免 EOS。JEDEC 公开发行的 JEP155 [1] 和 JEP157 [2]中指明了这种误解，并且令人信服地表明了 EOS 失效与 HBM 和 CDM 的强度并无关联。

工业协会的全球调查

为准备此白皮书，工业协会在电子工业界展开了关于EOS的全球调查。结果证实了长期以来EOS一贯占据产品失效帕累托（Pareto）图“高数据条”之一的观点。参看EOS调查结果，收到反馈的报告中，与EOS相关的占据了所有失效的20%以上，或者占据所有电子失效的30%。这使得EOS在帕累托图中占据了退还品已知失效原因最大的数据条。这明确地揭示了工业界对EOS更好理解的必要性，以解决其相关问题。

继续细看EOS调查结果，误应用（带电操作）是EOS损伤的最主要原因，超过40%的反馈显示最普遍的EOS损伤发生地在现场。相较于可测量ESD范畴的损伤现象，与EOS相关的损伤现象包括封装，硅晶片，及产品的更多方面。EOS调查的主要发现包括：

1. **带电操作**：带电操作作为 EOS 损坏的根本原因被广泛报告，在 EOS 损伤返品中占据了显著比例（20%以上）。带电操作可能导致过电压，装插不良，供电顺序，及使用中的错误偏压。

2. **绝对最大定额**：一部分返品显示的 EOS 损伤是由于提供了超出规定的绝对最大定额（AMR）的电压值，表明了不完全或不清晰的最大定额规定可能会是个问题，并且表明在产品规格书中对 AMR 进行特性描述和改进 AMR 的信息对于减小 EOS 风险是很重要的。

3. **ESD Related**: System level events, discharges from charged devices, and ESD controls in manufacturing which are not compliant with handling ESDS devices are additional root causes for EOS damage. Charged board events (CBE) and cable discharge events (CDE) also contribute.

4. **Miscellaneous Causes**: There were other miscellaneous causes reported that ranged from weak printed circuit board (PCB) designs to mishandling.

New Definition of EOS Incorporating AMR and EIPD

It became clear to the Council during analysis of the survey, as well as gathering data on customer–supplier experiences with resolving EOS-related returns that a new way of visualizing the relationship of AMR to EOS is sorely needed in the industry. The Council proposes that the relationship between EOS and AMR may be illustrated in the manner indicated in Figure 1. Definition of AMR and its relationship to device stress, reliability impact and long and short term damage potential allows semiconductor manufacturers to clearly provide the maximum voltage / current / power limits. This enables system manufacturers to incorporate devices into their systems safely and ensure an operational environment that does not exceed those maximum limits. This is based on the following EOS definition:

An electrical device suffers an electrical overstress event when a maximum limit for either the voltage across, the current through, or power dissipated in the device is exceeded and causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

Critical to this definition is a clear understanding of what is meant by maximum limit. Chapter 3 further expands this definition by providing a practical interpretation of EOS in terms of AMR. Insight into the electrical aspects of AMR can be gained by examining the voltage ranges illustrated in Figure 1.

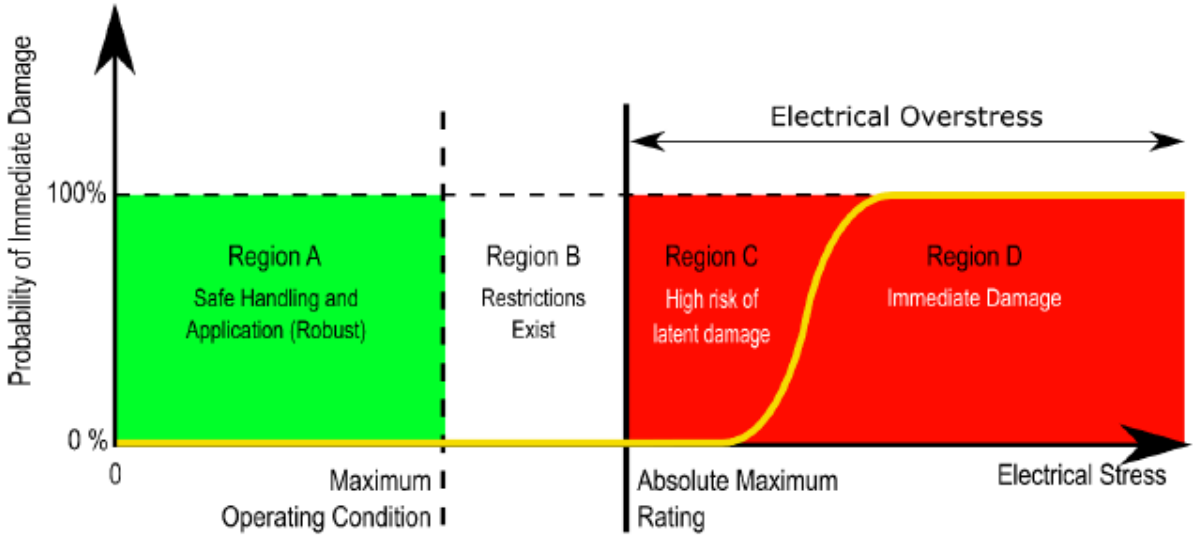

Figure 1: A graphical depiction of how Absolute Maximum Ratings should be interpreted. The yellow line is the number of components suffering immediate, catastrophic EOS damage

3. **ESD相关**：系统级别的事件，来自充电器件的放电，及制造过程中没有依照ESD标准的ESD控制等，是EOS损伤的另外几种原因。另外充电板事件（CBE）及导线放电事件（CDE）也会导致EOS损伤。

4. **其它原因**：还有一些报告提到其它原因，范围包括印刷电路板（PCB）的薄弱设计及误操作。

包含AMR和EIPD的EOS新定义

通过对调查的分析以及收集用户--供货商间解决EOS相关返品的经验数据，工业协会逐渐明确EOS和AMR关系直观化新方法对于业界的必要性。协会建议EOS和AMR的关系可以如图1的方法所描述。AMR的定义和它与器件压力之间的关系，可靠性影响，及长短期潜在EOS损伤使得半导体制造厂家可以明确地提供最大电压/电流/功率限制。这样系统生产厂商就可以安全地将器件引入他们的系统并确保工作环境不超过最大限制。这个基于以下EOS定义：

电子器件在施加的电压，或通过的电流，或消耗的功率，超出允许最大限额时会遭受电子过应力，导致直接损伤或功能失常，或潜在损伤所导致的不可预期的生命周期短缩。

这个定义最重要处是对“最大限额”的明确理解。第3章通过从AMR角度提供实用的EOS解释来更详细地延伸了这个定义。通过检查图1描述的电压范围可以洞察到AMR的各方面电气特性。

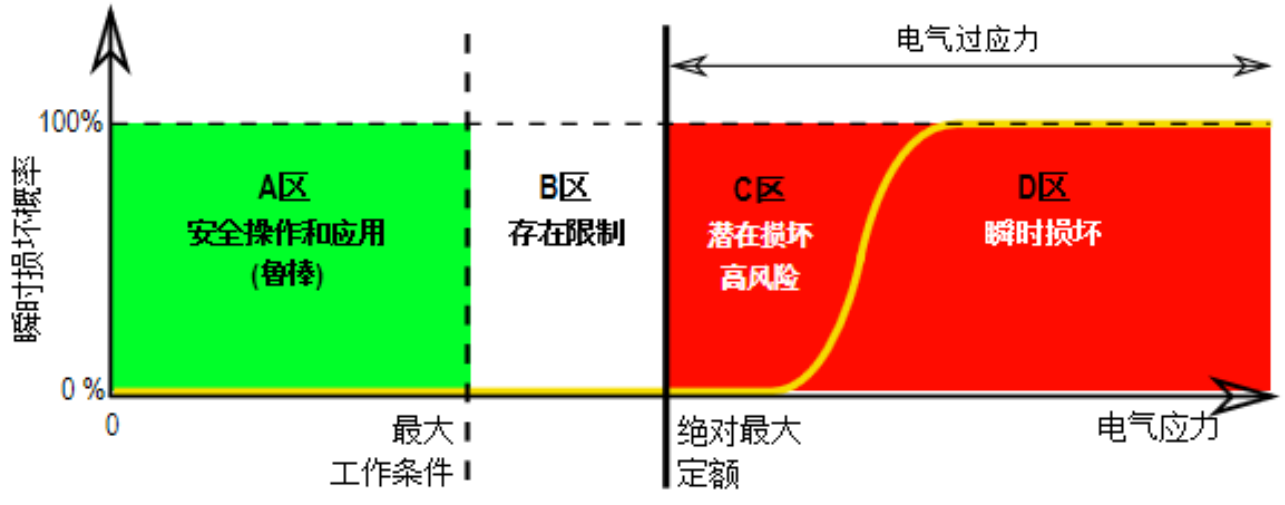

图1：图解应如何诠释绝对最大定额。黄色线显示遭受瞬时及致命的EOS损伤的元件数。

First, there is the safe operating area, a region of robust operation (region A). This is the region in which the manufacturer designed the device to operate. This is followed by a region in which operating restrictions exist (region B). In region B, the device is not guaranteed to function as specified, however the device is not expected to be physically damaged. Operating the device in region B for extended periods of time may also result in reliability issues. The upper limit of region B is the AMR. At and beyond the AMR the user should expect problems. Beyond the AMR are two regions of *electrical overstress* with either latent (region C) or immediate (region D) damage as a result of exceeding AMR. Note that the transition between latent damage and immediate damage is subject to normal process variations as illustrated by the yellow S curve. In order to properly evaluate the product reliability and robustness, it is important to understand that some qualification stresses, such as device level ESD and latch-up, are *expected* to run evaluations that will exceed AMR. For example, in the case of latch-up, this may be necessary in order to get significant current injection to assess latch-up robustness

There are different methods a device manufacturer may use to determine AMR values. The manufacturer may pick very conservative AMR values not based on physical properties of the product. This results in a wide region C before the onset of immediate damage. Alternatively, the manufacturer may define the AMR values based on detailed circuit and technology understanding resulting in a more accurate prediction of the damage threshold. This can result in the near elimination of region C. Regardless of the method chosen, the manufacturer is solely responsible for defining the AMR. Further, an AMR is a function of stress duration and any single documented value will have a fixed time association. Consequently, a clear understanding of the AMR by a system manufacturer is necessary to ensure that the operating environment of the system is within the specified conditions and that the limits defined in the AMR are never exceeded. This is particularly important when the system is using the semiconductor device in new or unique configurations. In these special cases, communication between the supplier and system manufacturer *is absolutely necessary*, particularly if the AMR does not appear to cover a mode of operation the system manufacturer expects their system to experience.

Beyond this discussion of regions of operation where the AMR describes maximum electrical and environmental values of operation, there is controversy about whether it should also refer to ESD limits. As noted above, while recognizing that this definition of EOS focuses attention on the AMR, placing greater significance and expectations on its limits than may have been given in the past, each supplier has their own approach to setting the AMR values. With respect to ESD, several different approaches have been observed:

- Some suppliers do not include ESD limits as part of their AMR because testing to establish the ESD limits often does not have similar statistical data collected as is required for setting more traditional items such as voltage.
- Some suppliers do place ESD limits in their AMR definition as it is felt that this is part of the overall agreement that must be met between supplier and customer.
- Other suppliers have placed ESD limits in an AMR section did so for no other reason than it was the only place that it made sense to them.

Regardless of the approach taken, the supplier is *solely* responsible for deciding what parameters and limits are included in their product's AMR. Since this discussion on AMR could be a new interpretation of existing documentation, system manufacturers should be communicating with their suppliers to verify that AMR information for any datasheet published prior to release of this white paper has appropriate meaning and that system manufacturers do not misinterpret the information as having a different meaning than the supplier originally intended.

首先，有一个安全工作范围，即稳定工作区间（区间A）。这是厂家设计的器件工作的区间。紧接着的区间里会有工作限制（区间B）。在区间B里器件不保证会按规格工作，但是器件也不至于会有物理损伤。器件长期在区间B里工作也会导致可靠性问题。区间B的上限就是AMR。在AMR以及超出AMR，用户应该要预期器件会有问题发生。超出AMR后有两个电气过应力区间，分别代表在超出AMR后所产生的潜在（区间C）和瞬时（区间D）的损坏。请留意潜在损伤和瞬时损伤间的渐变会受到正常的制程差异的影响，即图解中的黄色S曲线。为了正确地评估产品的可靠性和稳健性，一定的质检应力，类似器件级别ESD和闩锁的评估测试，会*有意*超出AMR，对于这个的理解比较重要。比如，在闩锁效应测试时，为了注入超大电流来评估闩锁的稳健性，超出AMR可能很有必要。

器件厂家有不同的方法来确定AMR值。厂家可能会选择比较保守的AMR值而不是基于产品的物理特性。这导致在瞬时损伤发生前会有比较宽的区间C。或者，厂家可能会基于对具体电路及技术的理解来定义AMR值。这样能对损伤阈值有更精确的预估，也可以近乎消除区间C。无论选择哪种方法，厂家全权负责定义AMR。而且，AMR与应力持续时间有关，任何书面记载的数值都会与固定的时间关联。因此，系统厂家对AMR的明确理解，对于保证系统在规格的条件范围内工作，且绝不超过AMR所定限制，是很有必要的。这对于半导体器件在全新或独特系统配置中的应用尤为重要。在这些特殊情况下，供应商和系统厂家间的交流*绝对必要，*尤其是如果AMR没有涵括系统厂家预期他们系统将运行的工作环境。

在此AMR描述最大工作电气和环境值的工作区间讨论之外，还有关于是否也该参照ESD限值的争论。如上所述，此EOS定义聚焦于AMR，比以往任何时候对它的限值赋予更重要意义且期待时，各供应商会有自己的设置AMR值的观点。至于ESD，目前有如下几种不同的方案：

- 有些供应商的 AMR 里不包含 ESD 限值，因为制定 ESD 限值的测试通常没有收集像传统项目所需的类似电压等的统计数据。
- 有些供应商确实在AMR定义里包含ESD限值，感觉是为达成供应商和客户间总体协议的一部分。
- 有些供应商把ESD限值放进AMR的一部分，唯一原因是他们没有其他地方比放在这里更适合。

无论采用哪种方案，供应商*全权*负责决定他们产品的AMR里包括哪些参数和限值。由于此对于AMR的讨论可能会对现存文档有新的诠释，系统厂商需要和他们的供应商交流，以确认在此白皮书发布前公开的规格书里的AMR信息的正确性，以及系统厂商不会对相关信息有不同于供应商原意的误解。

This white paper also points out that failure analysis engineers are likely to assign, albeit some would say prematurely, the term EOS to any visible damage signature that appears to have been the result of excessive voltage or current. These assignments are often based on experience and may often be correct. However, after initial failure analysis, often times it is unclear as to whether a device has experienced EOS per this white paper's definition until further communication between supplier and customer has been carried out. The damage could be a violation of an AMR caused by incorrect biasing in the application, over voltage, induced latch-up conditions, extreme uncontrolled ESD, misorientation, or something else entirely. The damage may also have been due to a defect in an individual weak device, an improperly set AMR or an intrinsic weakness in the technology. To that extent, this white paper introduces the term "electrically induced physical damage" (EIPD) to represent the term that should be used by FA engineers when no clear communication has been completed with the customer as to possible root causes of the damage. The definition of EIPD is the following:

Damage to an integrated circuit due to electrical/thermal stress beyond the level which the materials could sustain. This would include melting of silicon, fusing of metal interconnects, thermal damage to package material, fusing of bond wires and other damage caused by excess current or voltage.

The term EIPD is used when it has not yet been determined if a unit experienced an EOS event by the definition of EOS above and elaborated on in Chapter 3. That conclusion can only be determined after the supplier and customer have worked together to arrive at potential root causes.

EOS Root Causes

As shown in the fishbone diagram of Figure 2, there are many categories and sub-categories for EOS root causes. The three main categories where EOS damage can occur are:

1) **powered handling**
2) **unpowered handling**
3) **switching / alternating current (AC) applications**

Each category can be traced to a specific sub-category shown as branches in the fishbone diagram of Figure 2. The sub-categories of Figure 2 are not meant to be an exhaustive list of root causes but an overview of some of the more common root causes.

此白皮书还指出失效分析工程师们倾向于将 EOS 这个术语用于任何由过电压或过电流导致的可视损伤现象，尽管部分结论偏早。此类用法通常基于经验而且正确。但是除非供应商和客户间的进一步交流，通常初步失效分析并不清楚器件是否真的经历了此白皮书定义的 EOS。损伤可能因为违反了 AMR，包括非正确的应用偏置，过电压，引发闩锁的条件，极端不受控制的 ESD，定向误差，或完全不同的其他因素。损伤也有可能因相对弱的单一器件的某种缺陷，或没有正确设置的 AMR，或所用技术本身的弱点。基于上述，此白皮书介绍“电诱导物理损伤”（EIPD）术语，用于失效工程师们所描述这类没有和客户完成明确交流以找出可能根源的损伤。EIPD 的定义如下：

由于电气/热应力超出材料能承受水平而导致的集成电路损伤。这可以包括硅熔化，金属链接熔断，封装材料热损伤，接合线熔断，及其他过电流或过电压导致的损伤。

EIPD术语用于还不能确定某元件是否经历了上述定义及第三章里阐述的EOS事件。只有在供应商和客户合作找到潜在的根源后才可以明确那个结论。

EOS根源

如图2的鱼骨图所示，EOS根源包含很多分类及子分类。可能发生EOS损伤最主要的3类根源如下：

1）带电操作
2）非上电操作
3）切换/交流（AC）应用

如图2鱼骨图的各分支所示，每个分类可以追迹到某特定的小分类。图2的小分类并不是一个完全的根源清单，而是一些更共通根源的概览。

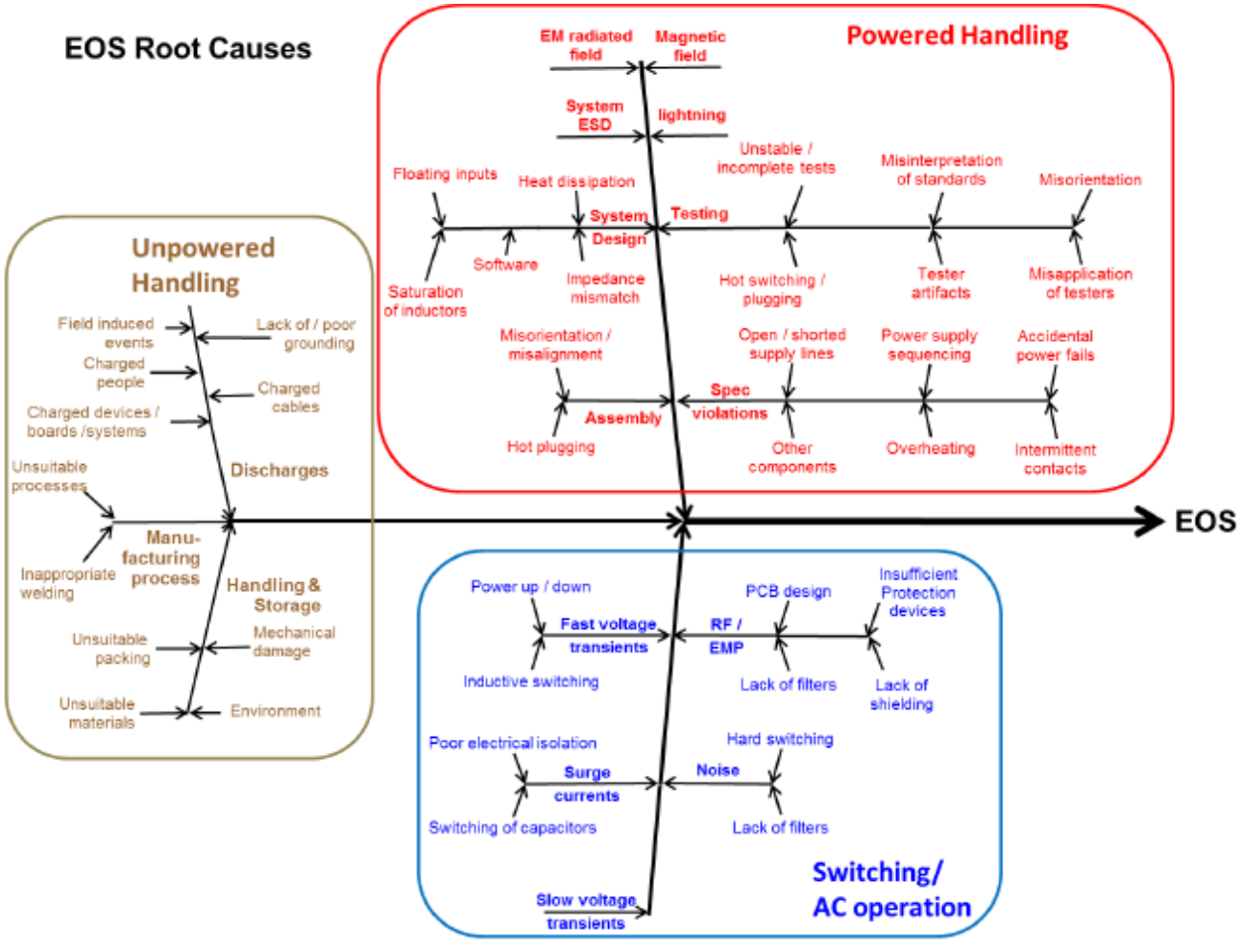

Figure 2: Fishbone Diagram Representing Different Root Causes Leading to EOS

Based on the EOS survey, the most common cause of EOS events is powered handling. Events may be related, for example, to overstress-induced phenomena when power is turned on, incorrect power supply sequencing, electromagnetic interference (EMI), or hot plugging. In addition, there are many system ESD events, especially during specification testing, which may result in unintended EOS damage. For responders showing a higher confidence level of finding a root cause of EOS damage (70 % to 100 %), a majority of those responders most often reported root causes which included hot plugging, overshoot / overvoltage, power surge, and misorientation being in their top 3, see Table 1 in Chapter 2. Clearly powered handling is an area where more focus is needed to address EOS damage.

In the unpowered branch, possible root causes include: an external charged source discharging into or through the device; the charged device/system being discharged; or the device/system being in an electrostatic field when the discharge has occurred. It should be noted that the root causes in unpowered handling are ESD-like in nature but may not be specifically related to the HBM or CDM testing performed as part of a product qualification. In fact, as the survey responses suggest, ESD represents a very small percentage of what constitutes EOS damage. Many manufacturers spend significant time auditing factories for ESD, thinking this will resolve all EOS events, when in actuality, it will only address a small percentage of EOS related damage. Auditing a factory for EOS involves a much more in-depth look at power delivery systems and connection issues with significant focus on the powered handling root causes shown in Figure 2.

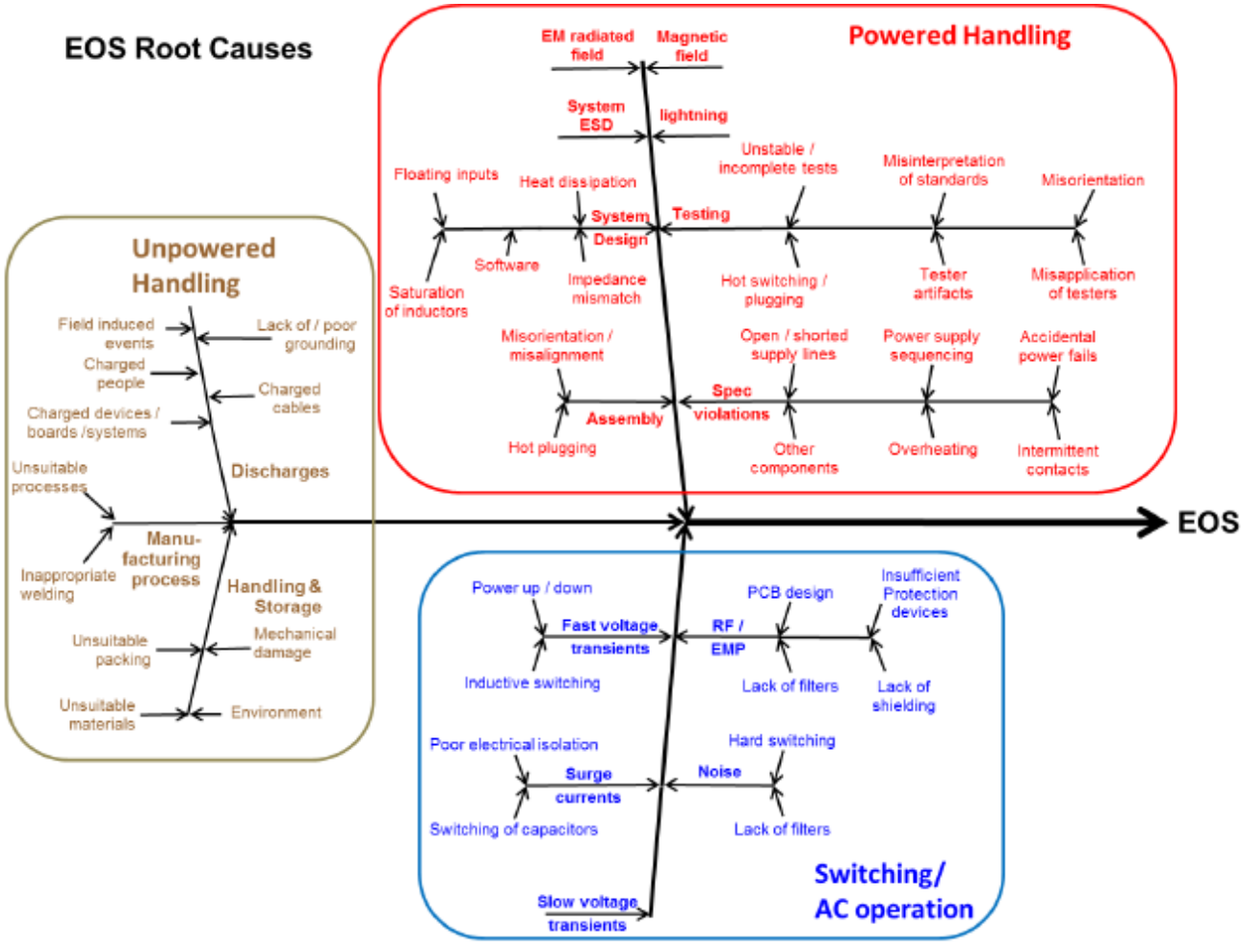

图2：EOS不同根源的鱼骨图

基于EOS调查，EOS事件最普遍的根源是带电操作。EOS事件可能关联到，比如：当电源开启时上电过应力导致的现象，错误的供电顺序，电磁干扰（EMI），或热插拔。除此以外，有很多系统级ESD事件，尤其在规格测试期间，可能会导致无意的EOS损坏。在拥有较高信心(70 %至100 %)的能查到EOS损坏根源的调查回复中，大多数报告的根源前3位都包括热插拔，过冲 / 过压，电源浪涌，及取向错误，参考第2章表1。很明显，解决EOS损伤问题需要更多关注带电操作这个根源领域。

非上电分支的可能根源包括：外部带电源经由该器件放电或放电进入该器件；充电了的器件/系统被放电；或放电发生时该器件/系统处于静电场中。需注意非上电操作时EOS损伤的根源在性质上与ESD类似，但并不一定与产品合格测试的HBM或CDM部分相关。实际上，从调查反馈结果看，ESD只占EOS损伤的一小部分。很多制造商花费可观的时间用于审计工厂的ESD，认为可以解决所有EOS事件。而在现实中这只能解决一小部分EOS相关损伤。从EOS角度审计工厂包括对供电系统和连接问题的更深层检查，及对图2所示各带电操作根源的显著关注。

Typical root cause examples in the category of switching / AC operation are radio frequency (RF) coupling, spurious electromagnetic pulses (EMP) or poor PCB design, all of which may result in EOS damage. This category had the lowest reported incidence as root causes of EOS damage but this could be a result of the difficulty in properly assessing the environment for this category.

EOS Root Cause Diagnostics

When failed products are returned, proper failure analysis (FA) methods become crucial, but the success in determining *root cause* depends on the process flow used in this work. *Communication and cooperation* between customer and supplier *must* happen if the root cause is to be found. One challenge involves determining what can be classified as EOS and what should not be considered as EOS. The analysis itself can be lengthy as failure analysis times can range from days to months. Chapter 6 discusses the factors that play a critical role in the analysis time. The analysis can also be complex, involving tools from optical microscopy to acoustic microscopy to assess the component and many other advanced techniques including analysis of the system board characteristics. But this may only identify a *cause*. Coupling the device failure analysis with the product return signature and the use environment is critical to finding the *root cause*. While proper training and the tools available to FA engineers described in this paper are necessary, an FA engineer can only find the *cause* of the device damage (such as the identification of the damage signature and probable polarity / path of transients resulting in the damage), not the root cause of what created the EOS event as shown in Figure 2. Therefore, there must be a cooperative effort between supplier and customer to find the *root cause*. It should be noted that in some cases, such as in a singular damaged unit or if the use environment in which the damage occurred is unknown, it may not be possible to determine root cause.

EOS Case Studies and IC Designs

There are many EOS damage scenarios that can be avoided if the product field return causes are understood. White Paper 4 discusses these in detail and establishes some important conclusions on A) **Product EOS Returns**, B) **IC Technology / Design Issues**, and C) **Field and Factory Events**.

A) Case studies of product returns with EOS damage signatures were analyzed to determine a root cause. This allowed a reduction of EOS occurrences and demonstrated how appropriate solutions can be identified to meet customer needs. Some important conclusions are:
    1. Failure analysis only provides a damage signature and probable path and does not reveal the true root cause.
    2. Incorrect testing limits during qualification can lead to failures being falsely identified as EOS.
    3. An EOS damage signature could be due to a broad list of root causes including, but not limited to; hot-plugging, ground bounces, supply switching, EMI transient surges, and process / product / system assembly issues.

切换/交流（AC）操作类的典型根源例子包括射频（RF）耦合，伪电磁脉冲或不良PCB设计，这些都会导致EOS损坏。此类占所汇报EOS损伤根源的最小范围，但也许是因为为这一类作正确环境评估的难度引起。

EOS根源诊断

当有失效产品退返，正确的失效分析（FA）方法变得至关重要，但成功确定*根源*取决于分析工作的流程。为找到根源客户和供应商间的*交流与合作必不可少*。其中一个挑战在于决定什么可以归纳为EOS及什么不应该被认为是EOS。分析本身可能很漫长，因为失效分析时间可以是几天至几个月。第6章讨论了影响分析时间的决定性因素。分析也可能很复杂，包括检查器件所用到的光学显微镜至声学显微镜等工具，和其它很多先进技术，包括系统板特性的分析。但这可能只识别一个*原因*。把器件失效分析结合到产品退返特征以及使用环境是找到*根源*的关键。一方面适当的培训及提供此白皮书里所描述的工具给FA工程师是很有必要，同时FA工程师仍只能找到导致器件损伤的*原因*（比如鉴定损伤现象，及可能导致损伤的极性 / 变化路径），而不是图2所示导致EOS事件的根源。因此必须有供应商和客户间的共同努力以找到*根源*。需注意某些情况下，比如只有一个单独损坏品或损坏时的使用环境未知等，也许不可能确定根源。

EOS实例分析及IC设计

如果理解了某产品市场返品的原因，那么很多EOS损坏情况是可以避免的。白皮书4对此有详细讨论，并在如下方面建立了一些重要结论：A）**产品EOS退返**，B）**IC技术/设计问题**，和C）**现场及工厂事件**。

A） 针对 EOS 损坏退返品的实例分析来确定根源。这有助于减少 EOS 的发生，并证明了怎样找到合适解决方案来满足客户需求。部分重要结论包括：

1. 失效分析只提供损坏现象及可能的损坏途径，但不能揭示真正的根源。
2. 合格测试过程中的不正确测试限度会导致失效被误判断为EOS。
3. EOS损坏现象可能会由很广泛的根源引起，包括且不限于下述：热插拔，接地反弹，电源切换，EMI瞬时冲击，以及制程/产品/系统集成问题。

B) Technology scaling and IC protection designs can also have some impact on EOS returns. A summary of these investigations reveal:
   1. Today's advanced process technologies have not shown any obvious increase in return rates for products exhibiting EOS damage when compared to older, more robust technologies [1, 2]. It should be cautioned that further technology advances, with thinner gate dielectrics and novel transistor process technologies, will reduce breakdown voltages and continue to shrink design windows. This reduction in breakdown voltage will reduce AMRs and may subsequently begin to influence returns which exhibit EOS damage. In all cases, it will become even more critical to adhere to the AMR boundaries and maintain clear communication between supplier and customer.
   2. As previously established, lowering ESD target levels for compatibility with technology scaling and circuit performance have no impact on EOS return rates.
   3. However, IC ESD protection design styles and implementations can have an impact on EOS if careful adherence to AMR values is not addressed. A summary of the design styles and their impacts are summarized in Chapter 7.

C) Factory and field return analysis can provide lessons learned as listed below:
   1. EOS damage can occur due to poor grounding methods and can easily be mitigated with established guidelines. A risk analysis often can avoid such problems.
   2. Learning from field events is important. Many of the problems could be avoided if the supplier and the board designer communicate early in the product application development cycle having knowledge of possible root causes.
   3. Automotive applications pose some of the most common risks. For example, hot plugging is a persistent problem in automotive electronics interconnection that can be mitigated by practicing the principle of first-mate-last-break.
   4. EOS caused by ESD can be reduced by avoiding charging/discharging in manufacturing lines and implementing a balanced ESD protection approach.

EOS Mitigation and Communication

An important focus of this white paper is to convey the proper understanding of EOS, fostering communication between supplier and customer and reducing the number of returns exhibiting EOS damage in the industry. Useful customer communication methods are identified based on observed case studies and the expected influences from IC designs, production issues, field events, and application issues. Points to consider include:

1) Proper understanding of AMR
2) Realistic specifications of AMR and customer realization of its limits
3) Accurate determination of the location and possible causes of the damage and finding the true root cause event which created the damage
4) Understanding the use application and impacts to the IC's ESD protection design
5) Lessons learned from product returns from both manufacturing and the field

These are summarized to help the industry deal with returns exhibiting EOS damage.

B） 技术缩小及IC保护设计也会影响EOS返品。此类研究的总结表明：

1. 和以前更强健的技术相比，当前的先进制程技术并没有显示EOS损坏产品返品率的明显增加 [1, 2]。需引起注意的是，随着技术继续发展，更薄的栅极电介质和新颖的晶体管制程技术会降低击穿电压，并继续压缩设计窗口。降低击穿电压会减小AMR且由此开始影响有EOS损伤现象的返品。在所有情况下，遵循AMR边界及保持供应商和客户间的明确交流变得更加重要。
2. 如前所述，降低ESD目标水平以保持技术定标与电路性能的兼容性并不影响EOS返品率。
3. 然而，如果没有谨慎遵循AMR值，那么IC ESD保护设计风格和实施可以影响EOS。第7章里总结了各设计风格及它们的影响。

C） 对工厂及现场返品的分析可提供下述经验教训：

1. EOS损坏会由不良接地方法引起，并能通过建立准则而很容易得到缓和。风险分析通常可以避免此类问题发生。
2. 从现场事件中学习非常重要。如果供应商和电路板设计方能在产品应用研发阶段尽早沟通并拥有可能的根源的相关知识，那么很多问题可以避免。
3. 车载应用提出了一些最共通的风险。比如：长久以来车载电器连接的热插拔问题，可以通过实施first-mate-last-break（FMLB：一种热插拔继电器）的原则而缓和。
4. 因ESD引起的EOS可以通过避免产线上冲/放电及导入平衡的ESD保护方案来减少。

EOS缓和与交流

此白皮书一个很重要的焦点是传达对EOS的正确理解，鼓励供应商和客户间的交流，以并减少业界由于EOS损坏的不良返品。基于对IC设计，生产问题，现场事件，及应用问题的实例分析观察和期待的影响，可以确定有用的客户交流方法。需要考虑的因素包括如下方面：

1) 对AMR的正确理解
2）可行的AMR规格及客户对其限值的认知
3）精确判断损伤的位置及损伤的可能原因，以及找到导致损伤的真实根源
4）对实际应用及对IC ESD保护设计的影响的理解
5）从产线及现场返品中汲取的经验教训

这些就是用于帮助业界处理有 EOS 损坏的返品的总结。

Summary

This is the first known comprehensive document on EOS in electronics manufacturing and operations written to foster understanding of EOS, root cause determination for resolving EOS issues, and implementation of methods for EOS mitigation. A common language on EOS as documented here is the first significant step to help solve and mitigate EOS issues. IC suppliers, customers, applications engineers, and system builders alike should take part in understanding and solving EOS. Finally, customers and suppliers should treat all conditions for applications as a contract and agree that all unspecified conditions are not allowed. Education of these important aspects is the responsibility of all parties involved.

Outlook

For over four decades, EOS has been one of the top causes of returns for semiconductor devices and systems. The Industry Council has documented here an extensive study which enhances understanding of EOS and recommends many approaches to reduce EOS damage. This should be of great value in preventing EOS from becoming a catastrophic issue in the next generation of technologies involving even more consumer, medical, military, and automotive applications. It would be important to revisit the information presented here at a later date and conduct another industry wide survey to see how much impact this work has made. EOS *is* inherent in the application of electronic systems. Only through continuous learning and sharing of experiences can future risks be avoided.

References

[1] Industry Council on ESD Target Levels, "White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," August 2007, at http://www.esda.org/IndustryCouncil.html or JEDEC publication JEP155, "Recommended ESD Target Levels for HBM/MM Qualification", www.jedec.org

[2] Industry Council on ESD Target Levels. "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Revision 2, April 2010, at http://www.esda.org/IndustryCouncil.html or JEDEC publication JEP157, "Recommended ESD-CDM Target Levels", www.jedec.org

总结

这是目前所知电子生产应用方面第一个关于EOS的综合文档，藉以鼓励对EOS的理解，确定根源以解决EOS问题，以及实施缓和EOS的方法。此文档里阐述的关于EOS的共同语言是帮助解决和缓和EOS问题的最初最重要的一步。IC供应商，客户，应用工程师，以及系统集成者们需理解并解决EOS。最后，客户和供应商们须把所有应用条件列入协议，并就不允许有未定义的条件而达成共识。对这些重要方面的教育是各参与方的义务。

展望

四十多年来，EOS一直占据半导体器件及系统返品的首要原因之一。工业协会在此文档里通过大量研究来促进对EOS的理解及推荐很多减少EOS损坏的方案。这对于防止EOS成为下个技术时代的灾难性问题有极大的价值，尤其会有更多消费类，医疗，军事，以及车载应用参与进来。一段时间后需重访此文档里展示的信息并实施下一次业界调查，来确认此工作带来的影响。EOS*是*固有存在于电子系统应用中。只有通过持续学习及经验分享才能避免将来的风险。

References

[1] Industry Council on ESD Target Levels, “White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements,” August 2007, at http://www.esda.org/IndustryCouncil.html or JEDEC publication JEP155, “Recommended ESD Target Levels for HBM/MM Qualification”, https://www.jedec.org/

[2] Industry Council on ESD Target Levels. “White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements,” Revision 2, April 2010, at http://www.esda.org/IndustryCouncil.html or JEDEC publication JEP157, “Recommended ESD-CDM Target Levels”, https://www.jedec.org/