TRANSMISSION LINE PULSE TESTING:
THE INDISPENSABLE TOOL FOR ESD CHARACTERIZATION OF DEVICES, CIRCUITS AND SYSTEMS

By Theo Smedes for The EOS/ESD Association, Inc.

Transmission Line Pulse testing is the default method for characterizing the behavior of devices under ESD circumstances. This article will introduce the method and its differences with classical ESD qualification methods. The history of the standardization work for TLP will be summarized. After two examples of the application of TLP, an outlook towards future developments will be presented.

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Founded in 1982, EOS/ESD Association, Inc. is a not for profit, professional organization, dedicated to education and furthering the technology Electrostatic Discharge (ESD) control and prevention. EOS/ESD Association, Inc. sponsors educational programs, develops ESD control and measurement standards, holds international technical symposiums, workshops, tutorials, and foster the exchange of technical information among its members and others.

WHAT IS TLP?

Transmission Line Pulse (TLP) testing is a method to characterize the behavior of components and circuits under ESD stress conditions [1], [4]. In contrast to classical component level Electrostatic Discharge (ESD) testing methods, like Human Body Model (HBM) [2] and Charged Device Model (CDM) [3], TLP provides more than a pass/fail result. It actually provides a quasi-static I-V characteristic that describes the behavior of the DUT. It can be regarded as a pulsed I-V measurement, using pulses with duration, rise time and current levels that are relevant for ESD events.

The pulses are made by charging a transmission line (typically 50Ω) to a pre-determined voltage and subsequently discharging into the DUT. By recording the incident and reflected waves with an oscilloscope, the DUT response can be measured. From the data in a defined measurement window in the stable part of the pulse, a quasi-static I-V point can be determined. Figure 1 shows a drawing of a typical pulse shape.

By repeating this charge/discharge procedure for multiple charge levels, a complete characteristic is established. Typical pulse duration is 100 ns, while typical current values can go up to a few Amperes. Generally, after each TLP pulse a low current DC measurement will be done in order to establish whether the DUT has been damaged by the preceding pulse. If the result of the DC measurement changes this often is an indication of device damage.

HISTORY OF TLP STANDARDIZATION

Although the idea of using transmission lines to generate short electrical pulses already existed earlier, it was not until 1985 that it was first introduced as a means to study semiconductor devices under ESD conditions [4]. Initially most semiconductor companies built their own TLP system, but in the early 1990's the first commercially developed systems became available. By now more than 10 companies offer TLP equipment.

To bring some commonality in the applied methods the ESDA started a working group to develop standard TLP approaches. This led to the publication of a Standard Practice document (SP 5.5.1) in 2004 [5]. After successful Round Robin testing the document was elevated to a Standard Test Method (STM 5.5.1) in 2008 [1].

In 1996, a new version of TLP with shorter pulse duration and shorter rise times was introduced: very fast TLP (VF-TLP) [6]. In 2007, a Standard Practice document on VF-TLP (SP 5.5.2) was released and a Round Robin experiment was started some years later [7].

Several revisions of these documents have been made. The 2014 version of STM 5.5.1 was republished by the IEC as IEC 62615 [8]. In order to be more effective, the ESDA working group decided it was better to maintain a single generic STM document covering all quasi-static forms of TLP. The results of the VF-TLP Round Robin showed the method yielded accurate and reproducible results and thus could be elevated to Standard Test Method [9]. Work was started to develop the generic document, which led to the publication of a new version of STM 5.5.1 in 2016, now covering VF-TLP, TLP and long pulse TLP.

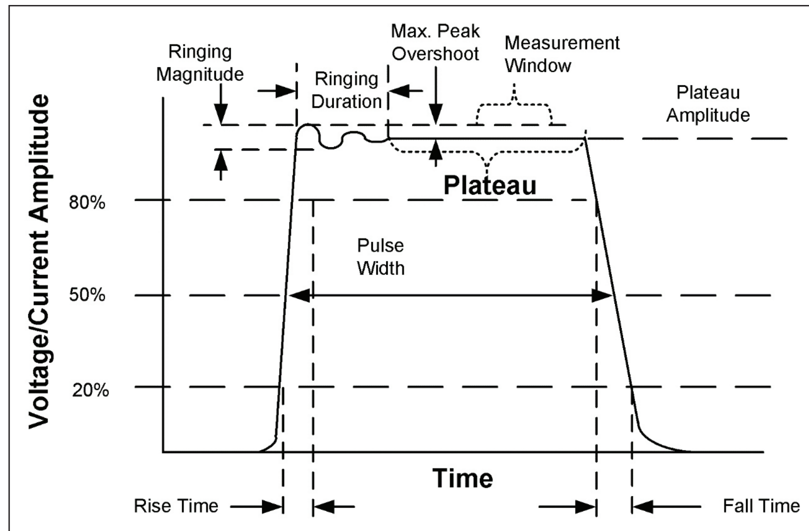


Figure 1: Typical TLP pulse shape. The annotations indicate relevant features that are defined in the standard documents.

ESD APPLICATIONS OF TLP

The most common application of TLP is the characterization of devices to see how they behave during standard ESD stresses, like HBM. A typical example is the 100 ns TLP characterization of a grounded-gate NMOST (ggNMOST), one of the workhorses in the field of ESD protections. Figure 2 shows the resulting TLP characteristics in the standard format introduced in [10]. This should be read as follows. The drawn red curve with symbols is the device I-V characteristic: TLP current (left y-axis) vs. TLP voltage (bottom x-axis). The red dashed curve is the development of the DC leakage current (top x-axis) vs. the TLP current (left y-axis). From this characteristics several important parameters, such as trigger voltage (Vt1), holding voltage (Vhold) and soft/hard failure current (Isoft, It2) can be derived.

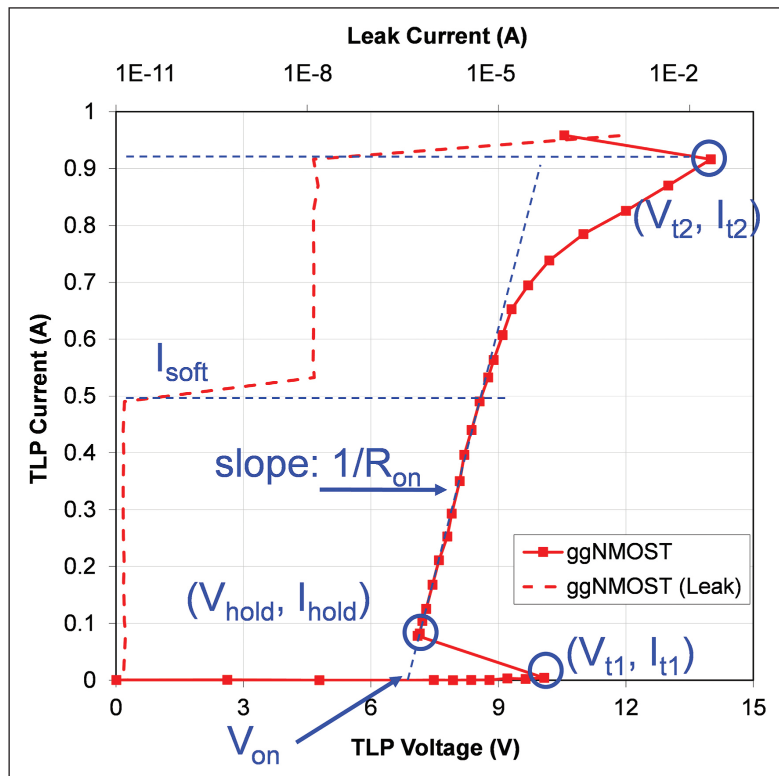


Figure 2: Example TLP characteristics using TLP with 100 ns wide pulses with 10 ns rise time. The annotations indicate relevant points and parameters that are defined in the standard documents.

This characteristic could not have been measured with regular DC curve trace equipment. The DUT would most likely not survive the

snapback when reaching the trigger voltage. If it would, the self-heating would be much stronger and the failure currents would much lower, because of the larger dissipation. Thus, the obtained values would not be realistic for the ESD regime.

Results as those in Figure 1, derived from 100 ns pulses with 10 ns rise time, describe the device behavior well for HBM-like events. A good rule of thumb is that 1 A TLP current corresponds to 2 kV HBM voltage, for dissipation driven failures [11]. The correlation is not exact since TLP is based on square pulses and the HBM current is a decaying waveform with 150 ns time constant and waveform details may affect the device behavior. To understand the behavior for CDM-like circumstances much shorter and faster pulses are needed. Typically 1 ns pulses, with 100 ps rise time, are used. On the other hand, pulses longer than 100 ns may be more suitable for certain system level ESD events.

To get a more complete overview, characterization like explained above, can be repeated by TLP with different pulse widths. Each pulse duration will yield a different failure point (Vt2, It2). This implies that the power-to-failure will depend on the pulse duration. Collecting these points will give the boundary of the safe operation regime. An example is shown in Figure 3 [12]. The Figure also shows that different regions can be distinguished, as explained by the Dwyer model [13]. The power profile covers the ESD spectrum (CDM, HBM, System Level ESD) and even longer duration stress.

The examples above described the application of TLP on ESD protection devices (stand-alone elements). Such information can be used to design protection networks for ICs. It is also possible to perform TLP measurements on the circuit level, e.g. for debugging ESD qualification problems [14]. However, the interpretation of the obtained characteristics is often more complicated, as in general multiple current paths exist between the connected terminals.

FUTURE TLP

With applications like those sketched above, TLP has established a definite position as the indispensable characterization tool for ESD engineers. New TLP methods, options and applications are still being developed. TLP with different pulse shapes has been proposed [15][16] as an alternative to the so-called system level ESD gun (as described in IEC61000-4-2 [17]) for use in HMM [18]. VF-TLP through a capacitor (CC-TLP) is proposed as an alternative for CDM, e.g. for small components that cannot be positioned in a regular CDM tester [19]. Developments like these are expected to continue.

However, also with existing equipment, new applications are being explored. Apart from the quasi-static behavior presented in the above sections, also information about the transient turn-on behavior of ESD protection devices can be derived. Currently the ESDA working group is working on a document that describes the hardware requirements and procedures that are needed to extract parameters like turn-on time, voltage overshoot, etc. from the transient waveforms resulting from transmission line pulses.

In addition, the working group will release a TLP user guide in the form of a collection of application notes. These application notes are short guides on topics, such as correlation between TLP results and other ESD tests, use of TLP on wear-out testing, effects of de-embedding, etc.

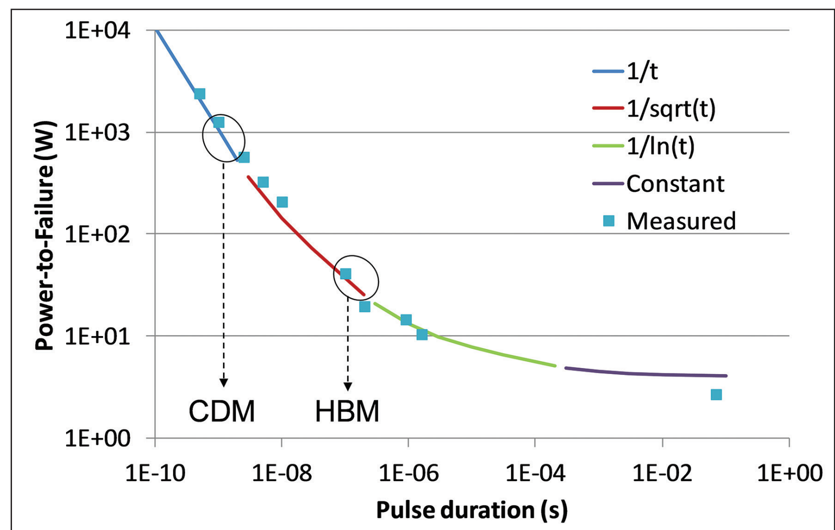
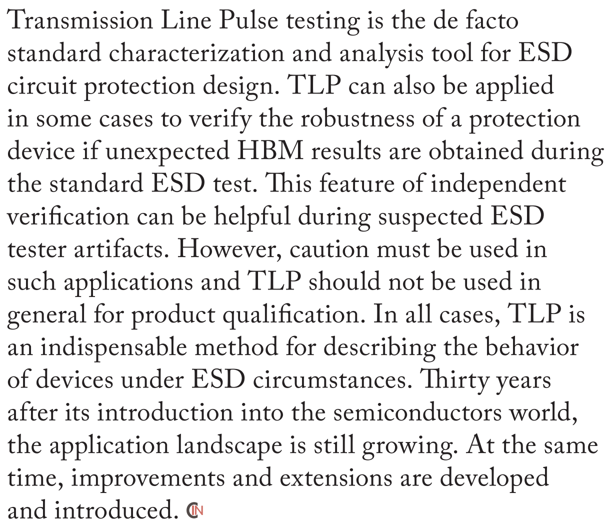


Figure 3: Example power profile, except the last point, all data points are measured using the same TLP equipment. The time regions that correspond to HBM and CDM are indicated.



CONCLUSION

Transmission Line Pulse testing is the de facto standard characterization and analysis tool for ESD circuit protection design. TLP can also be applied in some cases to verify the robustness of a protection device if unexpected HBM results are obtained during the standard ESD test. This feature of independent verification can be helpful during suspected ESD tester artifacts. However, caution must be used in such applications and TLP should not be used in general for product qualification. In all cases, TLP is an indispensable method for describing the behavior of devices under ESD circumstances. Thirty years after its introduction into the semiconductors world, the application landscape is still growing. At the same time, improvements and extensions are developed and introduced.

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