**(Title) A Look at the New ANSI/ESDA/JEDEC JS-002 CDM Test Standard**

**(Subtitle)**

**(Authors) By Alan Righter, Brett Carn and the EOS/ESD Association**

Charged device model (CDM) ESD is considered today to be the primary real world ESD model for representing ESD charging and rapid discharge and is the best representation of what can occur in automated handling equipment used in manufacturing and assembly of integrated circuits (IC) today. It is well known that the largest cause by far of ESD damage to an IC during device handling in a manufacturing environment is from charged device events.[1]

**Charged Device Model Roadmap**
With the ever-increasing demands for higher speed IOs in ICs today, and the need for packing more functionality into a single package driving larger package sizes, efforts to maintain even the current recommended target levels as discussed in JEP157[2] will be a challenge. It should also be noted that while technology scaling may not have a direct impact on target levels (at least down to 14 nm), the introduction of improved transistor performance in these advanced technologies can also enable higher IO performance (transfer rates) which can make achieving current target levels difficult for the IO designer as well. As a result, looking at roadmaps out through the year 2020 as published by the ESD Association (ESDA),[3] it would suggest that CDM target levels will need to be reduced again as shown in Figure 1.



**CDM Forward Looking Roadmap (Typical Min – Max)**
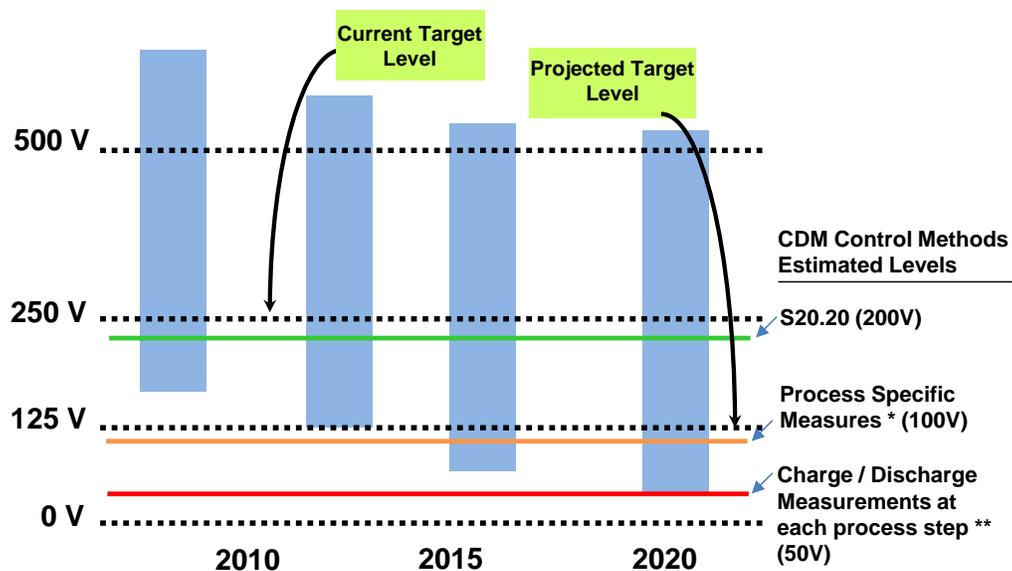
* - Include process specific measures to avoid charging *or* discharge
** - Include process specific measures to avoid charging *and* discharge

**Figure 1: 2010 and beyond charged device model sensitivity limits projections**

While a quick look at the above would not suggest a significant change in the range of CDM target levels a further look at data supplied by the ESDA and shown in Figure 2 does show that there is expected to be a significant change in the distribution of CDM ESD target levels.



2010-2015                                  By 2020
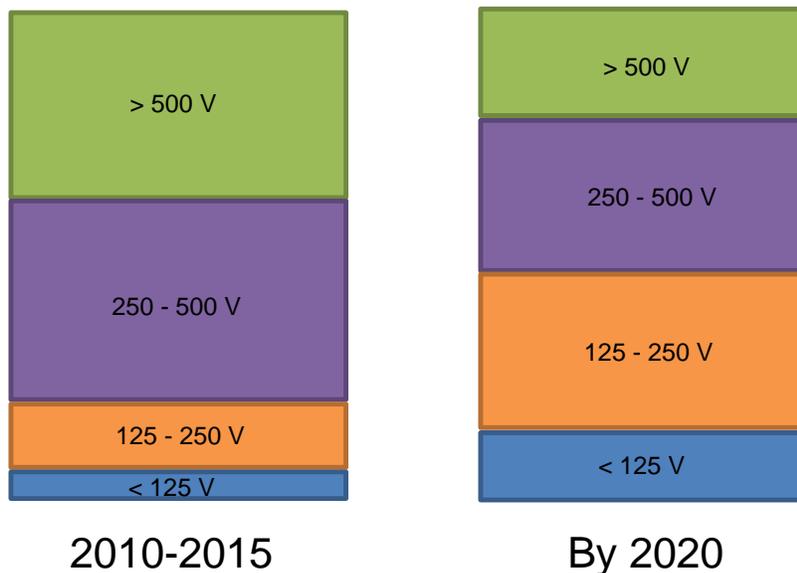
**Figure 2: Forward looking charged device model sensitivity distribution groups (Copyright © 2016 EOS/ESD Association, Inc.)**

Why is this important to discuss? It points out the need for a consistent way to test CDM across the electronics industry without some of the inconsistencies created by having multiple test standards. It is more important than ever to ensure manufacturing is properly prepared for the CDM roadmap discussed by the ESDA. One critical piece of that preparation is ensuring that manufacturing receives consistent data from each semiconductor manufacturer on the CDM robustness level of their devices and the need for a harmonized CDM standard has never been greater. This, coupled with continued technology advancements, may drive higher IO performance as well. This need for higher IO performance (and its need for reduced pin capacitance) may leave an IC designer with no other option other than lowering the target levels, which in turn demands a more precise measurement which is addressed within ANSI/ESDA/JEDEC JS-002.

**A New Joint Standard**

Prior to ANSI/ESDA/JEDEC JS-002, there were four existing standards, the legacy JEDEC (JESD22-C101),[4] ESDA S5.3.1,[5] AEC Q100-011[6] and EIAJ ED-4701/300-2 standards.[7] ANSI/ESDA/JEDEC JS-002 (Charged Device Model (CDM), Device Level)[8] represents a major first push towards harmonization of these four existing standards into a single standard. While all of these methods produce valuable information, the presence of several standards is not a benefit to the industry. The different methods often produce different passing levels, and the presence of several standards requires manufacturers to support multiple test methods with no increase in meaningful information. It is therefore vitally important that a single measurement level of an IC's charged device immunity is well known to ensure the CDM ESD design strategy has been implemented correctly and that the IC's charged device immunity is matched to the level of ESD control in the manufacturing environment to which it will be exposed.

JS-002 was developed by a combined ESDA and JEDEC CDM Joint Working Group (JWG) formed in 2009 to address this issue. Additionally, the JWG wanted to make technical improvements to the field-induced CDM (FICDM) method based on lessons learned since FICDM was introduced.[9] Finally, the JWG wanted to minimize disruption in the electronics industry. To reduce industry disruption, the working group decided that the joint standard should not require purchasing of totally new field induced CDM testers and pass/fail levels should be matched as close as possible to the JEDEC CDM standard. With the JEDEC standard being the most widely-used CDM standard, this keeps JS-002 aligned with current manufacturing understanding of CDM.

While the JEDEC and ESDA test methods are very similar, there are a number of differences between the two standards which needed to be resolved. There are also technical issues which JS-002 seeks to address. Some of the most important issues are listed below.

- Differences between the standards
    - Field plate dielectric thickness
    - Verification modules used to verify systems
    - Oscilloscope bandwidth requirements
    - Waveform verification parameters

- Technical issues with standards
    - Measurement bandwidth requirements too slow for CDM
    - Pulse width in JEDEC's standard is artificially wide
    - Waveform and equipment geometry requirements forced "hidden" voltage adjustments

To address the objectives and harmonize, the following hardware and measurement choices were made. Extensive measurements were made during the five-year process of document creation in arriving at these decisions.

- Hardware Choices
    - Use the JEDEC dielectric thickness

- o Use the JEDEC "coins" for waveform verification
- o Forbid use of ferrites in the discharge path

- Measurement Choices
    - o Require a 6 GHz minimum bandwidth oscilloscope for system verification/acceptance
    - o Allow the use of 1 GHz oscilloscope for routine system verification

- Minimize data disruption and discuss "hidden" voltage adjustments
    - o Align target peak currents with existing JEDEC standard
    - o Specify "Test Conditions" matching JEDEC stress levels. For JS-002 test results, we refer to Test Conditions (TCs) and for JEDEC and AEC we refer to Volts
    - o Field plate voltage adjusted for JS-002 to provide correct peak current corresponding to the legacy JEDEC peak current requirements

- Ensure full charging of large packages
    - o To ensure full charging of large packages, a new procedure was introduced

The next sections describe these improvements.

**JS-002 Hardware Choices**
The JS-002 CDM hardware platform represents a combination of the ESDA S5.3.1 "probe assembly," or "test head" discharge probe and the JEDEC JESD22-C101 verification module and field plate dielectric. Figure 3 shows this hardware comparison. The ESDA probe assembly was designed not to have a specific ferrite in the discharge path. FICDM tester manufacturers found that a ferrite was necessary and was added to increase the full width at half maximum (FWHH) specified minimum value of 500 ps and reduce the Ip2 (second waveform peak) to below 50% of first peak Ip1 to meet legacy JEDEC requirements. JS-002 removes this ferrite to remove this limiting factor in the discharge, resulting in a more accurate discharge waveform eliminating the ringing seen at Ip1 with a high bandwidth oscilloscope.
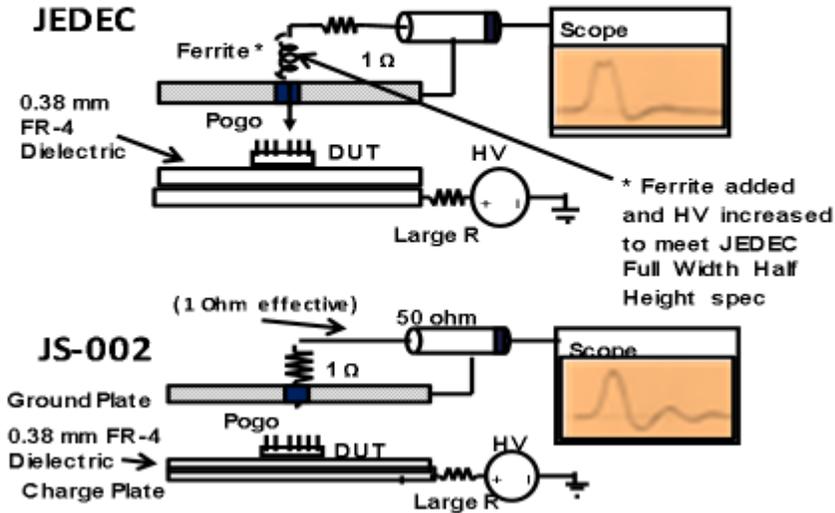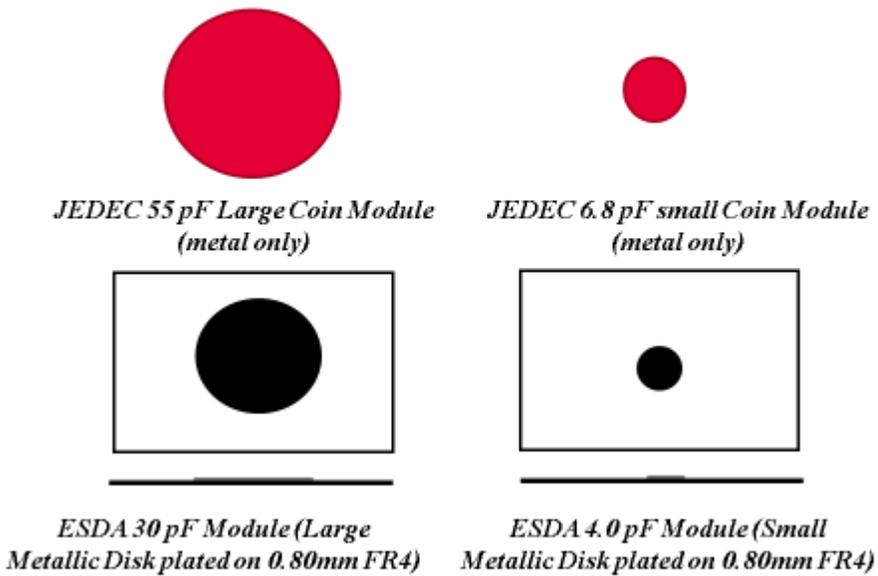
# JEDEC versus JS-002 Hardware



**Figure 3:  JEDEC and JS-002 platform hardware schematics**


Figure 4 shows the difference in the ESDA and JEDEC CDM standards verification modules. The ESDA standard has an option for two dielectric thickness options combining with its verification module (the second option being an additional (up to 130 um) plastic film between its module and the field plate, addressing testing of devices with metal package lids). The JEDEC verification module / FR4 dielectric represents a single small / large verification module and dielectric option supported by the much larger community of JEDEC standard users.

# JEDEC Vs. ESDA Modules



JEDEC 55 pF Large Coin Module
(metal only)

JEDEC 6.8 pF small Coin Module
(metal only)

ESDA 30 pF Module (Large
Metallic Disk plated on 0.80mm FR4)

ESDA 4.0 pF Module (Small
Metallic Disk plated on 0.80mm FR4)

**Figure 4:  ESDA and JEDEC verification module comparisons; JS-002 uses the JEDEC module**

### JS-002 Measurement Choices

The CDM JWG found during their data gathering phase of the JS-002 standard development that a higher bandwidth oscilloscope was necessary to accurately measure the CDM waveform. A 1 GHz bandwidth oscilloscope does not capture the true first peak. Figures 5 and 6 illustrate this.
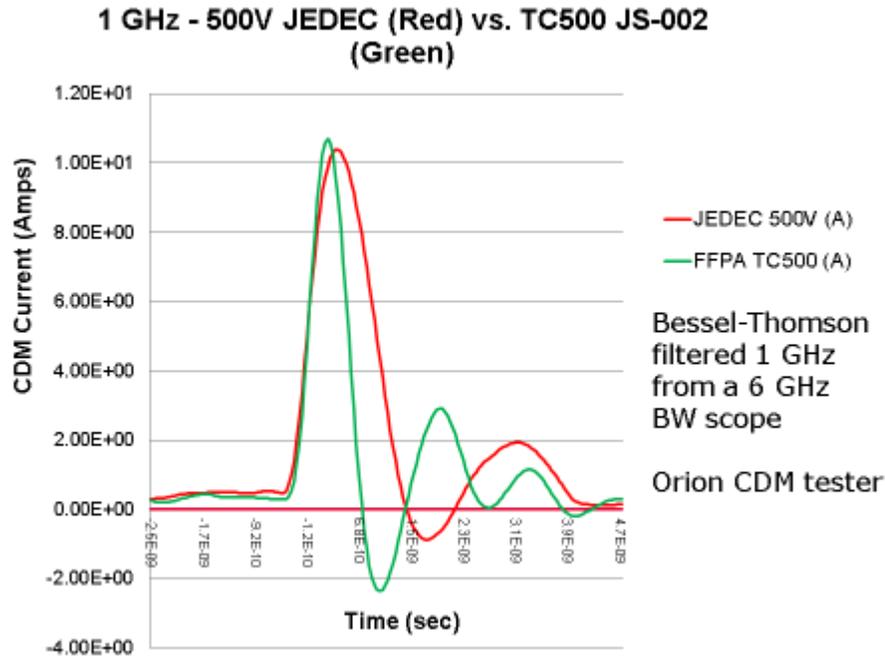
**Figure 5: CDM waveform of a large JEDEC verification module at +500V JEDEC versus JS-002 TC500 at 1 GHz**
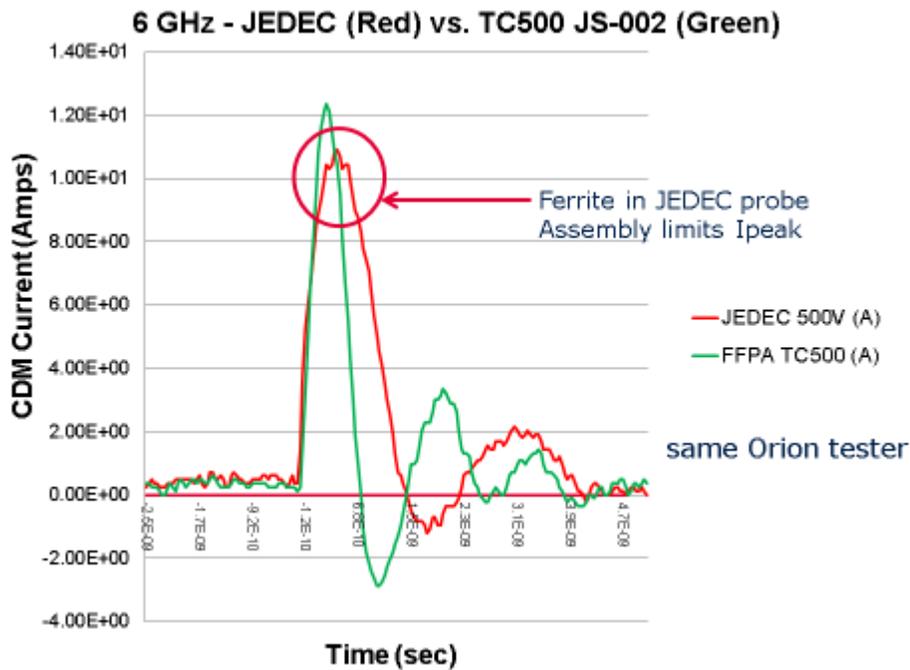


**Figure 6: CDM waveform of a large JEDEC verification module at +500V JEDEC versus JS-002 TC500 at 6 GHz**

Routine waveform checking such as daily or weekly checks can still be done using a 1 GHz bandwidth oscilloscope. However, analysis across lab test sites has shown that a high bandwidth oscilloscope provides better site to site correlation.[10] A recommendation to use the high bandwidth oscilloscope for routine and quarterly checks is included. Annual verifications or verifications after tester hardware changes or repair require the high bandwidth oscilloscope.

**Tester CDM Voltage Settings**
The CDM JWG also discovered that across tester platforms significant variation in the actual plate voltage setting (for example, 100V or more at a specific voltage setting) was needed to obtain standard test waveform compliance in the previous ESDA and JEDEC standards. This was not described in any of the standards. JS-002 is unique in determining the offset or factor required to scale first peak current (and voltage represented by a test condition) to the JEDEC peak current levels. Annex G of JS-002 describes this in detail. A spreadsheet showing an example of verification data incorporating this feature is shown in Figure 7.

| Tester - System #1 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Polarity = Positive | | | Scope Bandwidth = 8 GHz | | | | Factor/Offset Final Setting = 0.82 | | |
| MODULE SIZE | DATE | %RH | Test Cond | Software voltage | $I_{P\ AVG}$ (A) | $T_{R\ AVG}$ (ps) | $T_{D\ AVG}$ (ps) | $I_{P2\ AVG}$ (A) | $I_{P2}$ (% $I_{P1}$) |
| Large | dd/m/yy | X% | TC 500 | 500 | 12.1 | 275 | 610 | 4.3 | 36% |
| Small | dd/m/yy | X% | TC 500 | 500 | 7.30 | 185 | 400 | 3.7 | 51% |
| Large | dd/m/yy | X% | TC 125 | 125 | 2.90 | 283 | 611 | 1.1 | 38% |
| Small | dd/m/yy | X% | TC 125 | 125 | 1.90 | 201 | 395 | 1.1 | 58% |
| Large | dd/m/yy | X% | TC 250 | 250 | 6.00 | 276 | 609 | 2.2 | 37% |
| Small | dd/m/yy | X% | TC 250 | 250 | 3.70 | 186 | 397 | 2.1 | 57% |
| Large | dd/m/yy | X% | TC 750 | 750 | 18.30 | 274 | 611 | 7.2 | 39% |
| Small | dd/m/yy | X% | TC 750 | 750 | 11.00 | 190 | 398 | 6.1 | 55% |
| Large | dd/m/yy | X% | TC 1000 | 1000 | 24.40 | 276 | 612 | 9.2 | 38% |
| Small | dd/m/yy | X% | TC 1000 | 1000 | 14.60 | 187 | 399 | 7.4 | 51% |

**Figure 7:  Example recording sheet of JS-002 waveform data showing factor resulting in the TC (test condition) voltage [8]**

**Ensuring Full Charging of Very Large Devices at a Set Test Condition**
During the data gathering phase of the JS-002 development, another tester-dependent issue was discovered whereby some test systems were not fully charging large verification modules or devices to their set voltage before discharging. It was found that the high value field plate charging resistor (a series resistor between the charging supply and the field plate) was not consistent between test systems, affecting the delay

time required for full plate voltage charging. As a result, the first peak discharge currents could vary among testers, affecting the pass / fail CDM classification especially for large devices.

As a result, Informative Annex H ("Determining the Appropriate Charge Delay for Full Charging of a Large Module or Device") was written to describe a procedure for determination of the delay time needed to fully charge a device. An appropriate charge delay time is reached when a peak current "saturation point" (where Ip attains a basically constant value independent of longer decay time settings) is found to occur as shown in Figure 8. Determining this delay time ensures that very large devices are fully charged to a set test condition prior to discharge.



**Peak Current Vs Charge Delay**
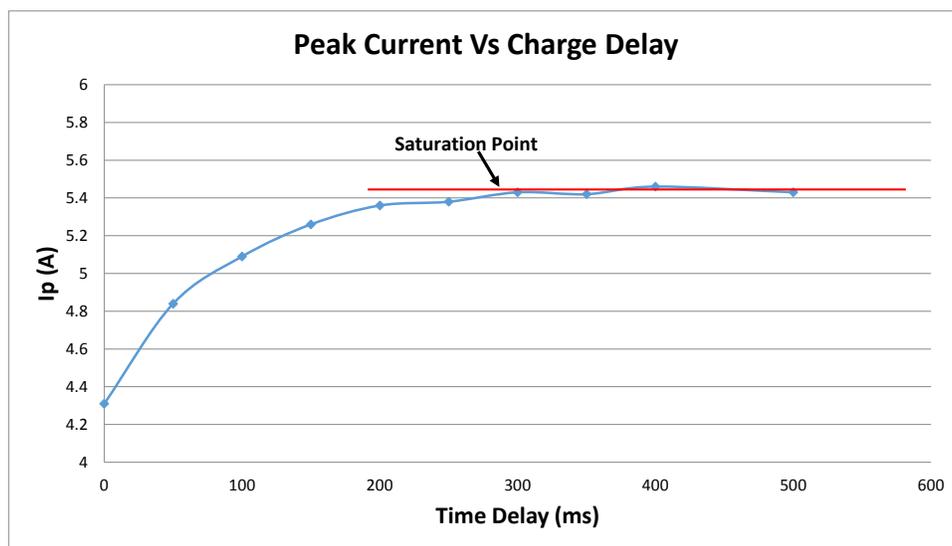
**Figure 8: Example peak current vs. charge time delay plot showing the saturation point / charge time delay [8]**

**Phase-In of JS-002 in the Electronics Industry**
The JS-002 standard replaces and obsoletes the ESDA S5.3.1 CDM standard for those companies using S5.3.1 as the standard. For those previously using JESD22-C101, the JEDEC reliability test specifications document JESD47 (specifying all reliability test methods for JEDEC electronic components) was recently updated to specify JS-002 in place of JESD22-C101 (in late 2016). A phase-in period is now in effect regarding JEDEC member company transition to JS-002. Many companies including ADI and Intel have already transitioned to testing using JS-002 for all new products.

The International Electrotechnical Commission (IEC) recently approved and updated their CDM test standard, IS 60749-28.[11] This standard incorporates JS-002 in its entirety as its specified test standard.

The Automotive Electronics Council (AEC) currently has a CDM sub-team committee updating the Q100-011 (Integrated Circuit) and Q101-005 (Passive Components) automotive device CDM standard documents to incorporate JS-002, with AEC specified test use conditions. These are expected to be completed and approved by the end of 2017.

**Summary**
As we look at the CDM ESD roadmap provided by the ESDA, CDM target levels will continue to be lowered, driven by higher IO performance. Manufacturing awareness of device level CDM ESD withstand voltage is more critical than ever and cannot be accurately communicated by inconsistent product CDM results coming from different CDM ESD standards. ANSI/ESDA/JEDEC JS-002 has the opportunity to be the first true industry-wide CDM test standard. The removal of inductance in the CDM test head discharge path significantly improves the quality of the discharge waveform. The introductions of a high bandwidth oscilloscope for verification, the increase to five test condition waveform verification levels, and an assurance of the correct charging delay time all significantly reduce cross lab variation in test results, improving repeatability from site to site. This is critical to ensure consistent data is supplied to manufacturing. With JS-002 acceptance across the electronics industry, the industry will be in a much better position to address the ESD control challenges ahead.

*About the Authors*
*Alan Righter is a senior staff ESD engineer in the corporate ESD department at Analog Devices, San Jose, CA. He works with ADI design / product engineering teams worldwide on whole chip ESD planning / design, ESD testing, ESD failure analysis, and EOS issues with internal and external customers. Prior to ADI, Alan was with Sandia National Laboratories, Albuquerque, NM for 13 years involved in IC design, test, product engineering, reliability testing, and failure analysis. Alan completed his BSEE and MSEE at Arizona State University in 1982 and 1984, respectively, and his PhD at the University of New Mexico in 1996. In 2007, Alan joined all Standards Device Testing working groups (WG5.x) and is also a member of Systems and Simulators WG14. He was appointed chair of WG 5.3.1, Charged Device Model, in 2008 and currently serves as ESDA Chairperson of the expanded Joint (ESDA/JEDEC) CDM Working Group, which recently completed the new ESDA/JEDEC Joint Standard JS-002. Alan is also currently Vice President of the ESD Association. Alan has been active in the EOS/ESD Symposium as author / co-author of ten papers, and is also currently ESDA Events Director. Alan also is active in the Industry Council on ESD Target Levels. Alan can be reached at alan.righter@analog.com.*

*Brett Carn initially joined Intel Corporation in 1999 and is a principal engineer in the Corporate Quality Network. He has actively worked in the field of device level ESD at Intel. In that role, Brett chairs the Intel ESD Council overseeing component level ESD & Latchup testing across all Intel sites worldwide, defining all internal test specifications, reviewing all Intel ESD design rules, overseeing/defining the ESD target levels for all Intel products worldwide and leading post silicon ESD debug on many products. In more recent years Brett has also been actively involved with addressing EOS challenges.*

*Prior to joining Intel, he worked for Lattice Semiconductor for 13 years where he started working on ESD in the early 1990s. Since 2007, Brett has been a member of the Industry Council on ESD Target Levels and has helped author several whitepapers as well as been the lead editor on the last four whitepapers. Brett is an active member of the ESDA and a current member of the ESDA Board of Directors. Brett is also a member of the ESDA Education Council, overseeing all online training, and is the current chair of the Technical and Advisory Support Committee (TAS) and a member of several ESDA working groups. Brett received his BS in electrical engineering from Portland State University in 1986. He can be reached at brett.w.carn@intel.com.*

***The EOS/ESD Association*** *is the largest industry group dedicated to advancing the theory and the practice of ESD avoidance, with more than 2000 members worldwide. Readers can learn more about the Association and its work at www.esda.org.*

[1] R. J. Peirce, "The Most Common Causes of ESD Damage," Evaluation Engineering, November 2002.

[2] Industry Council on ESD Target Levels. "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," Revision 2, April 2010, at www.esda.org or JEDEC publication JEP157, "Recommended ESD-CDM Target Levels", www.jedec.org.

[3] EOS/ESD Association Roadmap, https://www.esda.org/standards/complimentary-downloads/view/1869.

[4] JESD22-C101F, Field-Induced Charged-Device Model Test Method For Electrostatic Discharge Withstand Thresholds Of Microelectronic Components, JEDEC, October 2013, replaced by [8] in Sept 2016.

[5] ANSI/ESD S5.3.1, Charged Device Model (CDM) Component Level, EOS/ESD Association, December 2009, obsoleted by [8] in April 2015.

[6] AEC-Q100-011, "Charged Device Model (CDM) Electrostatic Discharge Test," Automotive Electronics Council, July 2012.

[7] EIAJ ED-4701/300-2, Test Method 305, "Charged device model electrostatic discharge (CDM-ESD)," Japan Electronics and Information Technology Industries Association, June 2004.

[8] ANSI/ESDA/JEDEC JS-002-2014, Charged Device Model (CDM) Device Level, EOS/ESD Association, April 2015.

[9] A. W. Righter et al, "Progress Towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments and Results," Proc. 2012 EOS/ESD Symposium, paper 1B.1.

[10] T. Smedes et al, "Pitfalls for CDM Calibration Procedures", Proc. 2010 EOS/ESD Symposium, paper 6A.1.

[11] IEC IS 60749-28, Electrostatic discharge (ESD) sensitivity testing – Charged device model (CDM) – device level; International Electrotechnical Commission, 2017.