The ESD Association and JEDEC Collaborate on Standards Development for Harmonized Electrostatic Discharge Test Methods

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In September, 2006 a small group of ESD control and design stakeholders assembled in a small conference room at the LaPaloma Resort in Tucson, AZ to discuss how the ESD Association (ESDA) and the JEDEC Solid State Technology Association (JEDEC) might harmonize some of their key device (component level) standards documents. Some of the stakeholders involved in those initial discussions (and similar meetings over the next six months) were integrated circuit manufactures, integrated circuit test manufacturers, original equipment manufacturers, integrated circuit test service providers, and representatives from the ESD Association and JEDEC. This first meeting was somewhat extraordinary as these industry stakeholders were able to bring JEDEC and the ESDA to the same table to start working on the harmonization efforts after other previous attempts failed. The key individual sponsoring this meeting was Kay Adams, the ESD Association President in 2006-7.

On October 13, 2008, JEDEC and the ESD Association announced that they had entered into a Memorandum of Understanding (MOU) agreement for the development of joint standards and publications in the field of device electrostatic discharge (ESD) sensitivity testing. This important action took place because both parties believed that this MOU was in the best interest of their organizations, their membership, and the industry. After each Board of Directors approved the MOU, and President David Swenson of the ESD Association and President John Kelly of JEDEC signed the MOU, the work began. Under this new agreement, the ESD Association and JEDEC immediately formed their first Joint Working Group for standardization work on a new Human-Body Model (HBM) document to replace ESDA's ANSI/ESD STM5.1-2007[1] and JEDEC's JESD22-A114F[2]. There will be more details about these efforts and the status of this HBM Joint Working Group later in this article.

The beginning of this harmonization effort did not come about without some compromise on the part of both organizations. The initial task of creating a MOU that would enable harmonization of the technical and procedural differences between two industry standards leaders and still allow each organization to follow their own time-tested procedures for standards development was significant. However, both JEDEC and the ESDA believed this combined effort to develop unified ESD test methods would be welcome news to an industry somewhat confused by the various ESD test standards currently available. Also, both organizations have an acute awareness of how ESD can significantly impair the reliability and operation of solid state devices, and that test methodologies are becoming ever more critical to the industry as technology advances and device complexity increases. The combined effort would also eliminate the need for stakeholders to participate in two parallel standards development groups.

How did we get two standards in the first place?

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[1] ANSI/ESD STM5.1-2007

[2] JEDEC JESD22-A114F

In the early days (late 70s to mid 80s) of ESD design and test, most ESD testing was done using MIL STD 883, Method 3015. This method was built around the simplified schematic in Figure 1. This method fixed the R and C values in the HBM to 1500 ohms and 100pF and standardized on a method for verifying the ESD pulse using a relatively low bandwidth voltage waveform measurement. With a standard in place, device users began to impose requirements on their suppliers to conduct the MIL STD test method. The amount of testing done in the industry increased dramatically especially when commercially available HBM simulators conforming to the standard became available.

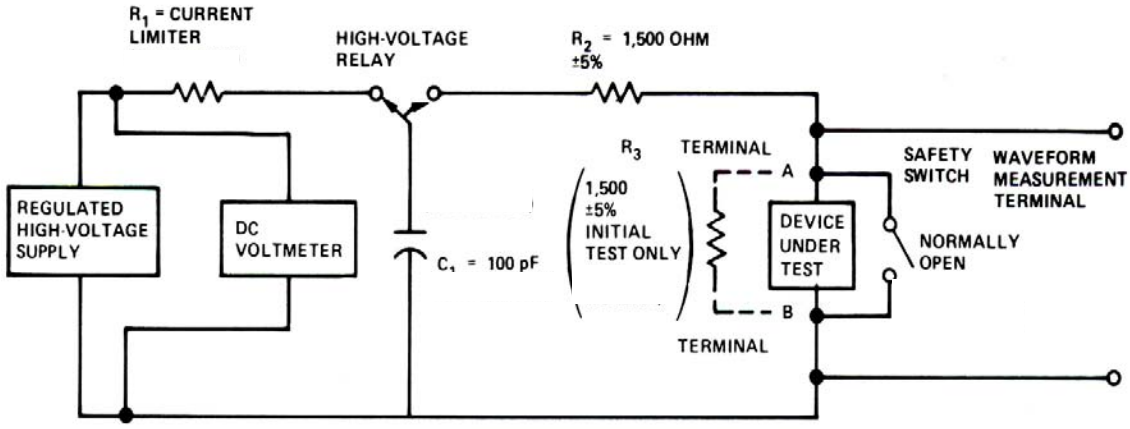

Figure 1: HBM Circuit Schematic MIL STD 883, Method 3015.2

With the increased use of this method, some serious problems became evident. Device failure threshold voltage data were beginning to show very poor correlation when nominally identical parts were tested on different machines. Some systematic studies were conducted[3,4] which confirmed the lack of correlation and it was shown that the voltage-based verification procedure in Method 3015 was not sufficient to expose parasitic effects in the testers such as inductance in the discharge path and test socket capacitance. Then industry experts began to convene at symposia and in standards organizations to address the issue. Other important questions were also emerging such as which pins to stress and ground during testing. At the time, neither JEDEC nor ESDA had standards for ESD testing and there was little communication between the two organizations. Although there were a few early attempts to start the revision of 3015 in a coordinated fashion, for the most part the two, as well as some other standards groups, went their separate ways.

While the same basic solutions paths were followed by the ESD Association and JEDEC, there were differences in detail and emphasis that built up over the years. Both organizations embraced common key elements to create a relatively reliable method: use a current waveform instead of voltage at higher bandwidth; characterize the effect of parasitic socket capacitance using a 500 ohm load current measurement and expand pin combinations to be tested. At the same time, Method 3015 was being similarly modified. As a result of these basic changes, new commercial simulators became available with dramatically improved correlation. Things might not have changed after that if it weren't for the continuing IC technology evolution.

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[3] D. L. Lin, M. S, Strauss and T. L. Welsher, Int. Rel. Phys. Symp. Proc (1986)

[4] L. F. DeChiaro and R. G. Chemelli, Int. Rel. Phys. Symp (1985)

In order to keep pace with the increasing pin count of integrated circuits, ESD simulators were designed with a relay-based switching network to allow for automatic HBM stressing and post-stress parametric pin leakage measurements. Initially the introduction of the relay matrix HBM simulators worked quite well for low pin count IC components. Unfortunately, as the pin-count increased, tester parasitics issues started to reoccur. In addition, the pin combinations which were required in the HBM standard were leading to very long test times and excessive repeated stressing of some pins, especially for devices with multiple power and ground buses. As we will see later, this situation persists to this day.

As a result, the two independent groups embarked on a series of investigations and modifications with different emphasis and, quite predictably, ended up with diverging approaches. These parallel paths were followed for almost 20 years. There were some brief attempts to harmonize the two different standards. One notable attempt took place in 1999-2000 when Sematech facilitated a discussion of differences between the two approaches. This effort led to some harmonization between the two standards between 2000 and 2004 but there still remained two separate test methods in two separate documents.

In the meantime more problems were surfacing with the relay-matrix-based simulators. Among other things, spurious pulses before and after the main pulse were discovered and described[5,6,7]. Between 1993 and 2007, there were 19 papers published on various aspects of real and simulated HBM pulses and on tester parasitics and their impact on the accuracy of ESD withstand threshold voltages of devices. The two organizations took different approaches to responding to these phenomena at least in terms of what changes actually were made in the documents. As a result, at the time of the September 2006 meeting, the two documents were diverging while the industry was looking for a common global standard.

Making One Standard Out Of Two

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[5] R. A. Ashton, B. E. Weir, G. Weiss and T. Meuse, EOS/ESD Symposium Proceedings 2004, pp. 153-159
[6] C. Duvvury, R. Steinhoff, G. Boselli, V. Reddy, H. Kunz, S. Marum and R. Cline, EOS/ESD Symposium Proceedings 2004, pp. 132-140
[7] T. Meuse, R. Barrett, D. Bennett, M. Hopkins, J. Leiserson, L. Ting, J. Schichl, R. Cline, C. Duvvury, H. Kunz, and R. Steinhoff, EOS/ESD Symposium Proceedings 2004, pp. 141-145

While the JEDEC/ESDA MOU was being negotiated, the members of the ESD working groups of both organizations began preparations for the creation of a single merged HBM standard test method. An *ad hoc* Joint Working Group (JWG) was formed and began meeting to create a listing of all differences among the two documents and formed sub-teams to address them. The team was co-chaired by Mike Chaine (Micron) and Terry Welsher (Dangelmayer Associates) who were, respectively, the current chairs of the ESDA and JEDEC groups working on the separate documents. The JWG was comprised of the current membership of the JEDEC ESD Task Group and ESDA Device Testing Working Group 5.1. When the MOU was completed and signed, the group was no longer *ad hoc* and began formal operation. Nearly 80 issues in 12 categories were identified, prioritized and assigned to sub-teams. For many of the issues it was relatively easy to get conceptual agreement but putting details together often took more discussion and work than was expected. The basic philosophy was to create a merged document without addressing the various unsolved technical problems that had not yet been implemented in either document. These issues were placed in a "parking lot" for consideration after the merged document was completed. There were a few exceptions to this. For example, the descriptions of measuring equipment (e.g., oscilloscopes, current transducers) were updated. The circuit schematic (Figure 2) was updated to reflect the additional measurements and machine construction subtleties that had been absent from the 3015 diagram and were not completely represented in either specification.

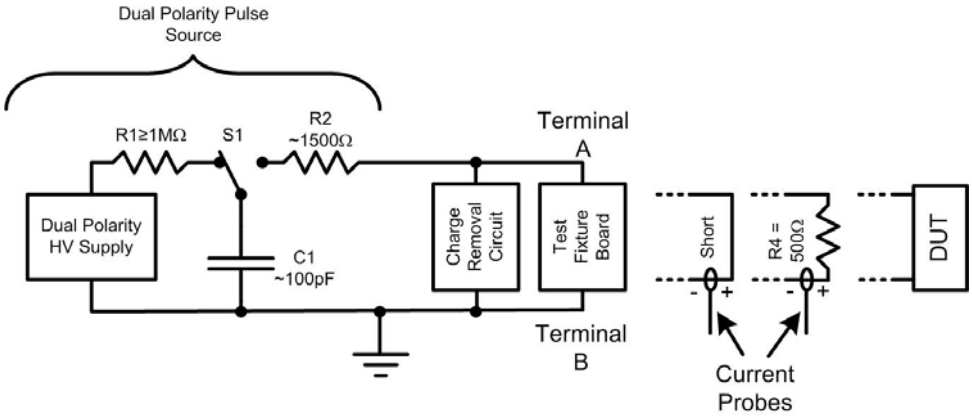

Figure 2: HBM Circuit Schematic in Merged ESDA/JEDEC Standard

Two major points about the merged document are worth noting: 1) The ESDA had given considerably more attention to defining the procedures for qualification and verification of the stress test equipment than had JEDEC. For example, the concept of a "test fixture board" and its qualification was not directly mentioned in the JEDEC standard. As a result the new section on qualification and verification was largely based on ESDA S5.1 but was completely re-written to improve clarity. 2) JEDEC had been quicker to adopt adjustments to required pin combinations in response to specific issues with parasitics and test productivity. For example, the JEDEC document allowed a group of power or ground pins connected to a common "package plane" to be represented by a single pin for stressing and grounding. ESDA had also considered this allowance but had not yet approved it. The Joint Working Group considered each of these items very carefully. Ultimately, the JEDEC allowances for this and two other alternate approaches were adopted in the merged document. The justification for this was that the changes had been used in the field for several years and were working without any problems reported by industry.

How do the two organizations work together?

The MOU is the basis for a joint development process followed by parallel balloting and approval in the two organizations. The initiation of a new joint project is considered and approved by each organization's responsible committee(s). Once approved, the joint working group is formed and can begin their work on the standards document. Each organization selects a working group co-chair for the management of the joint working group. The co-chairs then plan their meeting agenda together. Each organization encourages equal participation from their membership on each joint working group and every effort is made to hold meetings in conjunction with other meetings being conducted by the respective organizations.

When the joint working group has completed a document, the document is submitted to each organization for approval. Each organization operates according to its own respective rules and procedures during this approval process and the document is distributed to the responsible committees within each participating organization. If either organization's voting body declares the document not approved, the document is returned to the joint working group for additional work. Joint documents are not released by either organization until approved by both organizations.

Future Work by HBM Joint Working Group

While creating the merged document, the joint working group had to set aside work to advance HBM test technology and to solve some of the increasing problems such as false failures occurring due to parasitics, unintended cumulative failures due to excessive pin zapping and very long test times especially for high pin count devices or those with multiple power and ground buses. The group is considering several strategies for future discussion. A few examples are listed below.

Reduction of pin combinations: This could be accomplished by a combination of reducing stressing between pins in different power domains[8,9], using statistical samples of the pins to be tested or eliminating testing between signal pins (since failures are rarely seen).

Two-pin testing: In this approach, the existing pin combination strategy is replaced by the simple requirement that each pin will be stressed with respect to each other pin individually. This has the advantage of allowing the complete elimination of the relay-matrix in favor of "flying probes" to make the two-pin contact for each stress.[10] While this would solve many of the problems with parasitics it would actually increase test time. The implementation would probably also require some sampling or other strategies to reduce the number of pin pairs tested.

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[8] R. Gaertner, R. Aburano, T. Brodbeck, H. Gossner, J. Schaafhausen, W. Stadler and F. Zaengl, EOS/ESD Symposium Proceedings 2005, pp. 178-183

[9] T. Brodbeck, R. Gaertner, W. Stadler and C. Duvvury, EOS/ESD Symposium Proceedings 2008, pp. 106-114

[10] E. Grund, 2009 International ESD Workshop , Presentation F.3

Testing of No-Connects: Device pins which are not connected electrically to the die are currently not tested. This is because of unintended effects observed in the relay-matrix testers. [11] This effect results in secondary arcs to adjacent pins. While this might happen in the real world, the tester unrealistically amplifies the magnitude of the event due to the parasitic capacitance of the switching network. Alternate strategies are being considered so that meaningful assessments of no-connects and their adjacent pins can be properly evaluated.

Other Considerations: Other areas of investigation include qualification of test boards with no positive clamp mechanical connection, additional methods to avoid parasitics, better waveform characterization methods, inclusion of wafer-level and bare die test concepts, small device considerations, further protection from spurious pulses and changes in the definition of thresholds or classifications.

Document Status and Future Collaborations

At the time this article was being published, the merged HBM document[12] had been released by the joint working group and was working its way through the parallel approval processes. In the absence of any surprises it will be approved by the JEDEC Board of Directors and ESDA Standards Committee in time for publication in 2010. In addition to the HBM effort, a second group has begun laying the groundwork for a merged Charged-Device Model (CDM) Standard. This will be a tougher challenge because the two methods actually specify different hardware and generally produce different withstand threshold voltage values. A path to a solution to this problem, suggested by Tim Maloney of Intel[13], is being considered and a round-robin experiment based on the idea is being planned. The goal for the merged CDM document is 2011. Now that it has been demonstrated that the two organizations can work together towards a common document, other areas for collaboration may be initiated in the future.

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[11] H. Kunz, C. Duvvury, J. Brodsky, P. Chakraborty, A. Jahanzeb, S. Marum, L. Ting and J. Schichl, EOS/ESD Symposium Proceedings 2006, pp. 24-31

[12] ESDA/JEDEC JSxxx-2010, Month, 2010

[13] T. J. Maloney, Presentation to ESDA/JEDEC CDM Joint Working Group, February, 2009

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About the Authors

Tim Jarrett is an ESD Engineer at the Cardiac Rhythm Management (CRM) division at Boston Scientific. He is responsible for ESD control program management, training, materials and equipment analysis, facility evaluation, standards development, and ESD stress testing. Tim has been an active member of the ESD Association and has served as a Board member, Human Resources Business Unit Manager, Standards Committee Business Unit Manager and STDCOM Chairman, and Symposium Steering Committee member. Tim is a NARTE Certified ESD Control Engineer.

Dr. Terry L. Welsher is currently Senior Vice President of Dangelmayer Associates. He began his career in Bell Labs in 1978 where he worked on electrolytic corrosion failure mechanisms in electrical interconnection materials. In 1986 he began directing Bell Laboratories' core expertise in electrostatic discharge (ESD). The newly formed group proceeded to produce a string of ground-breaking contributions to the field and played a key role in advancing industry standards. At his retirement from Lucent Bell Labs in 2001, he was Director of the Quality, Reliability and Test Center of Excellence. Dr. Welsher has served as Chairman of the ESDA Standards Committee and Technical Program and General Chair of the EOS/ESD Symposium. He is currently a member of the ESDA Boards of Directors and will begin serving as Vice President of the ESDA in 2010. He has also been active in the JEDEC Quality and Reliability Committee and Board of Directors. Most recently he has led the effort to harmonize and

merge JEDEC and ESDA device testing standards. He holds a B.S. in Chemistry from Florida State University and Ph.D. in chemical physics from the University of Texas at Austin.

About the ESD Association

Founded in 1982, the ESD Association is a not for profit, professional organization dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors educational programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: http://www.esda.org.