# ESD Electronic Design Automation Checks

by ESD Association EDA Working Group

The verification of Electrostatic Discharge (ESD) protection in a complex Integrated Circuit (IC) design is extremely challenging. Leading edge designs have many supply domains and voltage levels for different functional parts like RF, digital, and high voltage blocks, making ESD checking a complex and error prone task. Relying on manual verification alone poses a significant risk of missing design flaws, which can be very costly during manufacturing and in the field. Consequently, automated ESD checking is highly desired in today's design flow. This article outlines the essential requirements of the ESD verification flow as defined by the ESD Association (ESDA) Electronic Design Automation (EDA) Tool Working Group [1].

Figure 1 illustrates the timeline and main stages for an example design flow. The IC product design flow (top row) needs to be synchronized with an ESD development and implementation flow (middle row). The latter needs to be supported by an ESD check flow (bottom row).

The following sections describe the main IC development phases and give examples of different ESD checks relevant for these phases.

## Product Definition Phase

The ESD performance specifications usually follow commonly accepted standards. However, depending on the field of application they can be modified by marketing teams and IC customers. Product design specifications and required ESD performance dictate specifications of ESD components and ESD cells. Based on these functional requirements, suitable ESD cells are defined per each pin application node (signal, power, and ground). Typically the ESD cells are made accessible to the designer in a dedicated ESD library.

In a situation when a mature semiconductor technology is used, with already developed ESD libraries, only placement and product specific modifications of the existing ESD components and ESD cells need to be verified. For a new IC product that uses a new semiconductor process, an ESD library may not be available and no specific cell level ESD checks can be executed. However, performance specifications of the needed ESD library could still be defined together with the IC customer based on the available ESD technology development data and ESD EDA data from other products/technologies.

Based on the available design data in this design phase the following ESD checks can be performed:

• Protected device checks to verify that the available ESD library cells can provide the required safe operating conditions for the protected components at each pin, for the given design functional requirements.

• Cell level checks on the existing ESD cells.

• Package level check to determine for example, expected peak Charged Device Model (CDM) currents as well as package and die specifications to meet CDM performance specifications.

Due to the nature of these data, a simple check of the ESD compliance can be done based on the ESD characteristics of the ESD cells in a design database. The following is an ESD EDA check example performed during product definition.

An early analysis of the integrity of I/O cell, bus placement and the overall ESD robustness is one of the essential factors of a successful chip design. An ESD floorplanning checker for the chip could enforce the ESD design rules to be verified while planning I/O cell and power bus placement. In particular, the checker could verify the existence of an ESD cell/device between pads, estimate parasitic resistance between pad and ESD cell/device, and give a rough estimate of the chip ESD robustness by predicting pad voltage (Figure 2).

## Chip Architecture Phase

At this design stage, the functional/behavioral level chip architecture is defined and required ESD components and library cells are identified. No circuit or layout level IC description is available in this phase. Similar to the previous section, cell level checks and protected device checks can be performed. The available design data are similar to those described in the previous section.

## Module and Full IC Design Phase Checks

This is the main design activity phase, involving complex interaction between all product teams. It can be divided into three sub-stages.

1. The first stage is the floorplanning of the chip architecture modules and the standard digital I/O and power banks. The ESD checks that could be done at this design stage are limited to top-level verification of the ESD network within the digital I/O banks and ESD connectivity between the different modules, the related I/O banks in the different power domains and the package level ESD connections. These checks include:

• Protected device checks for the digital modules.

• Cell level checks for the new ESD library cells.

• Intra power domain checks for the digital Intellectual Property (IP).

• Floor plan/top level ESD checks for the power and ground domain bus crossing.

• Basic package level checks.

2. The second stage is the design of IP modules and analog I/O pad rings. At this design stage the analog (and RF) modules and the related I/O banks are physically designed. In many cases, the analog IP module team is different from the I/O and power/ground cell design team, which is often responsible for integrating the ESD library cells. The module team may not have detailed information about the ESD components used at cell level and special attention is needed when checking the overall ESD implementation. A certain level of co-design between the analog modules and the dedicated ESD protection cells may be needed as

well. Based on the available design data, the following ESD checks could be performed:

• Cell level checks for the analog pin ESD library cells (can be newly developed e.g. for custom analog form factors or in-module / off- pad ring placement).

• Intra power domain checks for analog pad rings.

• Intra power domain checks for each analog module.

• Inter power domain checks (if there are several power domains in one analog module).

• Protected device checks for the individual modules.

• Special ESD rule checks on specific analog/RF blocks/IP's – e.g., differing ESD target levels.

Specific tool functionality is needed for the cases where the ESD protection cells are placed in the analog pad ring, which is not available to the team performing the ESD checks at module level. Such tool functionality can be extended to allow verification of module ESD robustness against cross power domain or cross IP stress events. This is especially useful when the counter pins are not available physically but some information about the involved ESD network (ESD cells, connectivity) is present in the design database. This can be considered a "virtual chip integration" where only a particular module design is physically available to the team running the check. This situation also applies to the verification of a given module involving evaluation of ESD performance of third party IP ("black box").

3. The third stage is full chip IP and I/O integration, including package. This is the final level of ESD checks applied to the whole IC. The main purpose is to verify the integration of the individual IP ESD circuits at top IC level, to check for the new cross-IP integration ESD violations, parasitic devices, and to verify that the protected components at each individual IP module are still operating in their ESD safe operating area (SOA) for stress combinations including other IP.

Based on the available design data, the following ESD checks could be executed:

• Inter power domain checks.

• Package level checks.

• Protected device checks for the full IC.

For certain classes of designs (e.g., some digital designs), it might be possible to implement certain hierarchy of checks so that at the full chip level the individual design blocks are considered as "black boxes" and only the integration of the blocks is verified.

The following is an example of ESD checks of the module and full IC design phase aimed at identifying potential ESD weaknesses of I/O assemblies (rings or arrays). An I/O assembly could be checked at this stage with an ESD verification tool covering both the layout checks and the electrical checks. The layout checks could ensure that the predefined ESD rules are strictly followed. In particular, the checker could flag input buffer gates and output buffer drains without adequate ESD protection, parasitic bipolars, violations of minimum ESD metal width, etc. The electrical checks of I/O assembly at this stage can vary in complexity: they can use simplified I/O netlists only or include detailed models of ESD protection elements and parasitics. The verification of primary ESD current path existence and checking alternative current paths for each pin to pin combination is the main objective of the check at this stage [2]. The checker could flag the situation where no ESD current path exists or where an unintended parallel path with weak devices becomes preferred during an ESD event. Basic checks can be done using an extracted netlist from the schematic for all pin-to-pin combinations. This can then be followed by a more detailed analysis for selected pins using the netlist extracted from the layout. Figure 3 shows part of an I/O ring with primary and alternate current paths for a given pin stress combination. An appropriate check of these two current paths would involve high speed static and dynamic simulations on the large netlist of interconnect and ESD relevant components.

## Design Qualification Phase

In this phase, final design audits and ESD performance assessments are executed using the verification results from the previous phases. This is often done based on a custom company defined standard practice methodology, summarized in an "ESD check list" or other document. The goal is to confirm that all required ESD verification activities have been performed.

EDA tools functionality at this design stage is mostly related to reporting and documenting the results of the checks executed earlier and storing the results in a suitable database for further analysis. Such analysis is usually needed for product ESD troubleshooting during IC qualification.

In practical design cases involving complex IC products and ESD solutions there could be situations in which some ESD violations may still be reported when an IC is sent for manufacturing due to limitations of the ESD verification tools or due to non-ESD-related product development priorities. However, under all circumstances, the result of the formal ESD EDA check runs could allow for easy product ESD troubleshooting. The ESD EDA checker output could help with relating possible ESD test failures with identified ESD design marginalities.

The ESD checks of the final IC verification phase are most extensive. They are similar to the checks which have been performed during earlier design phases. However, ESD EDA tools could be capable of operating on much larger netlists, including full chip resistance, capacitance, and package information. The following are a few ESD EDA check examples performed during this phase.

A final ESD IC check could include verification of all designated ESD current paths using an EDA tool. To achieve better accuracy for a given pad stress combination more than one ESD path could be found and analyzed since ESD current flow may not be limited to the shortest path identified earlier. A report from such tool would include calculated node voltages and currents and can be used for the ESD sign off before the tape out. Figure 4 shows an example of the final chip level checker output, where three distinctive ESD paths for a chosen pair of pads (IO_D2 and IO_ANA) were found. Voltages and currents along ESD paths have been found by running DC simulations where an HBM 1.33A current has been forced between the two pads. Simulated voltage potentials and currents at each path node are shown in Figure 4. Bus parasitics have been included in simulations. For example, the voltage difference between nodes V2 (7.76V) and V3 (5.35V) is coming from both diode D1 voltage drop (2.39V) and VSSIO bus resistance voltage drop (0.01V). Voltage stresses

across most sensitive devices are being monitored to ensure that while the total voltage drop between stressed pads may be high (16.48V), devices are not being stressed in excess of their failure limits. In particular, voltage between VDD and VSS in this example does not exceed the 0.68V and IC core can be considered ESD robust.

After completion of the initial IC integration critical cross domain boundaries between different supply voltage networks on chip could be identified. The high voltage drop across these boundaries during an ESD stress makes them more prone to ESD damage than the devices placed within the same power domain. The increasing number of different supply voltage domains in today's generation chips necessitates an automated check to find devices that would be impacted during an ESD event. Depending on the acceptable voltage stress level for the specific devices at the domain interface, ESD design weaknesses could be identified by an EDA tool after checking thousands of possible interface connections. In addition, protection measures already implemented at power domain boundaries (diodes connected to an interface gate oxide, etc.) have to be taken into account as well when analyzing ESD robustness of devices at power domain boundaries. Figure 5 gives an example of a cross-domain level shifter, where a gate connected to node 1 could be overstressed during an ESD event.

## Conclusions

In this article the, essential requirements of an effective ESD EDA verification flow were described. These requirements are aligned within the IC design community ESD verification needs. The proposed verification flow offers a systematic approach to check ESD robustness across all IC blocks at different phases of design flow. This approach allows avoiding many ESD design flaws reducing the overall design cycle time. The ESD EDA tools would improve the ESD predictive capabilities by generating extended netlists (including ESD device, resistance, capacitance, and package) and retiring an approach of crude "back of the envelope" extractions, manual/visual checks, and resource intensive SPICE simulations. Another important benefit of these tools is the possibility to use them for systematic ESD design optimization. The ESD EDA check requirements outlined in this article could be the basis for additional effort by the EDA vendors to adapt their tools and to make a comprehensive ESD verification flow feasible.

More details on the proposed ESD EDA verification flow can be found in the ESDA Technical Report ESD TR18.0-01-11 [1], which is available for free download at http://www.esda.org/standards.html. At the time of writing the ESDA EDA Working Group consisted of the following members: Michael Khazhinsky (Silicon Labs), Fabrice Blanc (ARM), Gianluca Boselli (Texas Instruments), Shuqing (Victor) Cao (Global Foundries), Norman Chang (Ansys), Dan Clement (On Semiconductor), Rosario Consiglio (Impulse Semiconductor), Maxim Ershov (Silicon Frontline), Melanie Etherton (Freescale Semiconductor), Eleonora Gevinti (ST), Harald Gossner (Intel), Matthew Hogan (Mentor Graphics), Larry Horwitz (Synopsys), Kelvin Hsueh (ESD Consultant), Mujahid Muhammad (IBM), Louis Thiam (Cadence), Nitesh Trivedi (Infineon), Vesselin Vassilev (Novorell).

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## References


[1] M. Khazhinsky, et al., "ESD Electronic Design Automation Checks," ESDA Technical Report ESD TR18.0-01-11, pp. 1-75, 2011.

[2] N. Trivedi, et al., "Two Approaches for Design Verification for ESD," IEW, pp. 408-418, 2007.

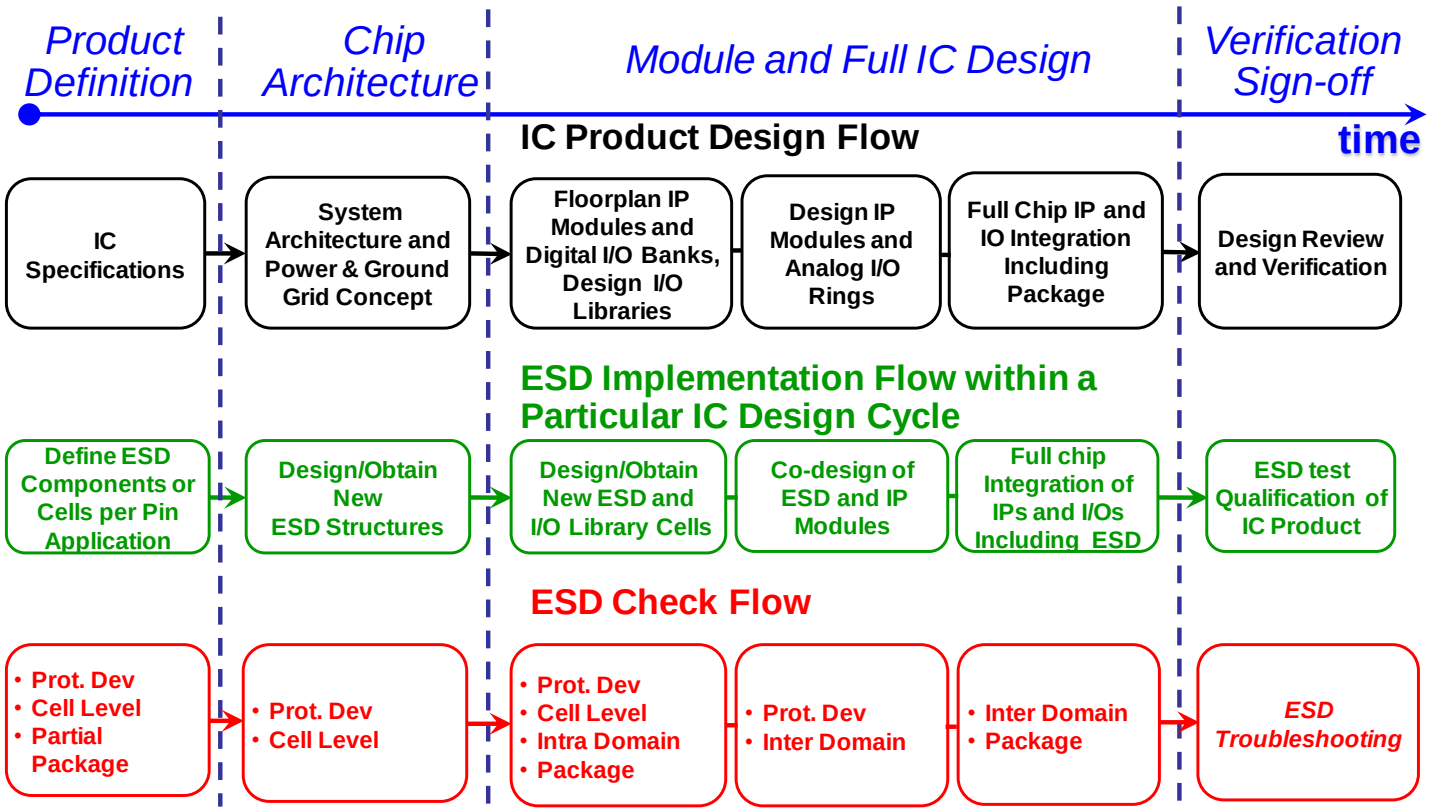


Figure 1: Simple ESD Verification Flow Mapped to Sample IC Design Flow.

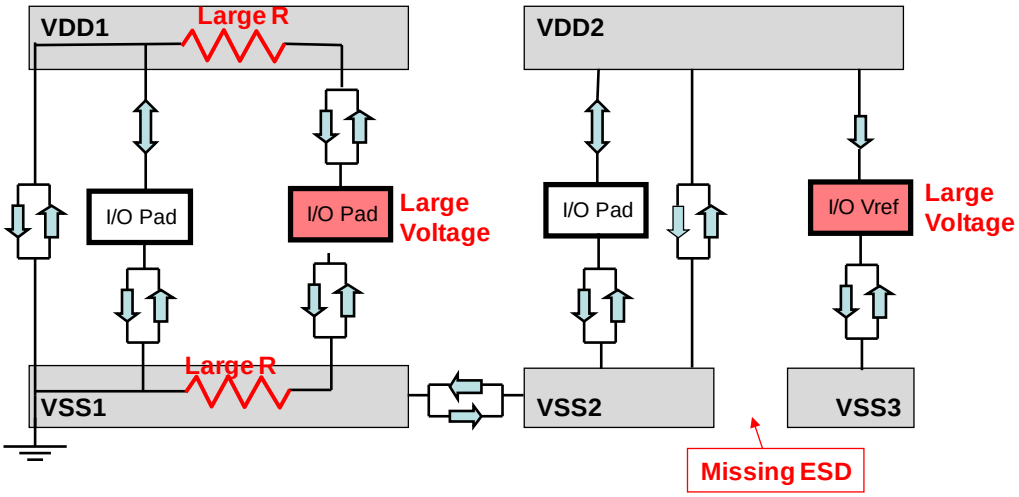


Figure 2: A sample I/O assembly checked with an ESD floor plan checker. Tool output flags missing ESD protection devices and large resistances in the ESD current path.

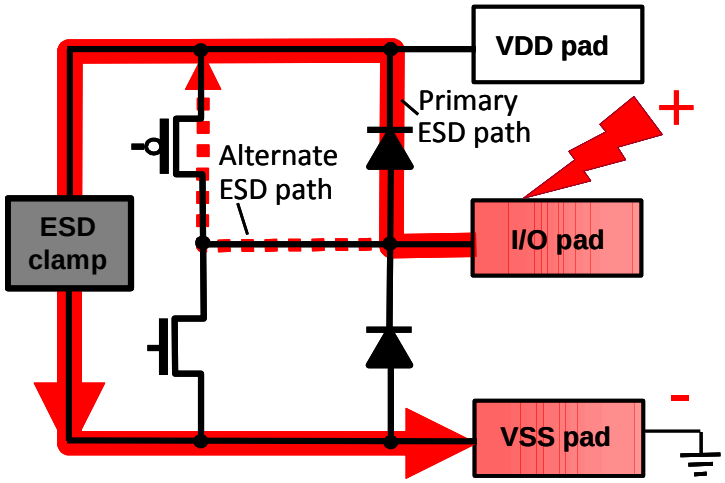


Figure 3: Check of ESD path in an I/O ring. An appropriate check of these two current paths would involve high speed static and dynamic simulations on the large netlist of interconnect and ESD relevant components.

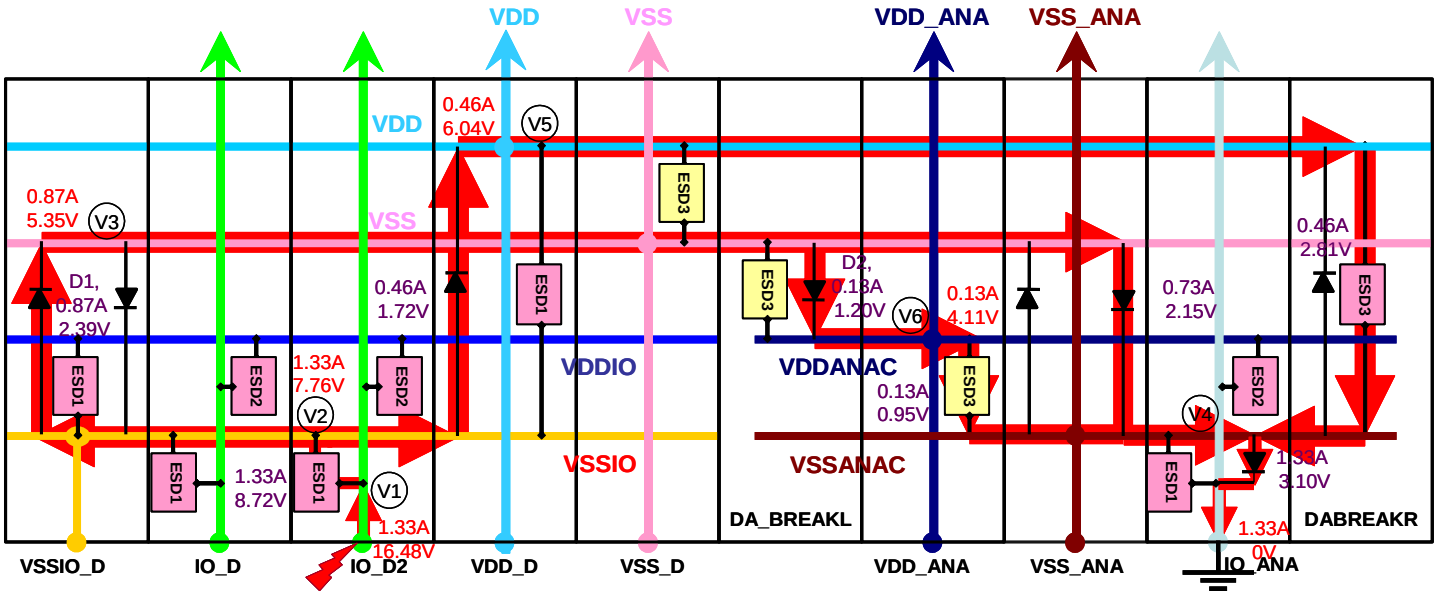


Figure 4: Example of the final chip level checker output. Simulated voltage potentials and currents at each path node are shown. Bus parasitics is included in simulations.

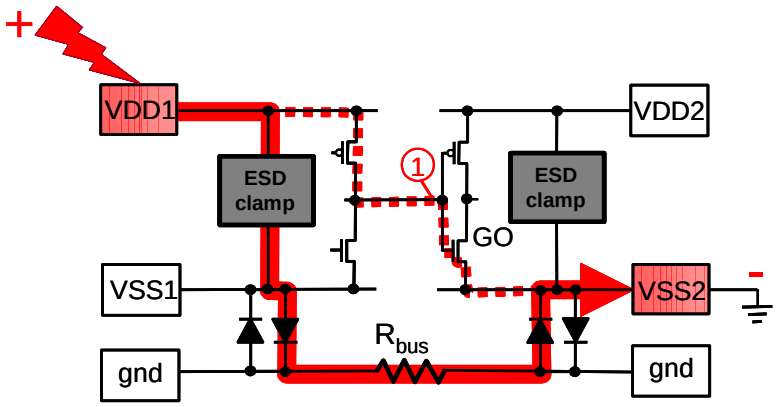


Figure 5: Power domain boundary crossing check: Due to increased Rbus, primary ESD current path (thick line) becomes less attractive resulting in stressed gates at node 1.