(Title) IEC 61000-4-2 Emulation and Simulation

(Subtitle)

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ESD qualification requirements for systems rely heavily on discharge models such as IEC61000-4-2. The basic idea of an "IEC Gun" is to *emulate* (reproduce in the lab) the discharge of a "typical" human, charged to various test voltage threshold levels, with a "typical" discharge resistance holding a metal object. 3D field solver and nodal *simulation* (reproduce in a virtualized computer model) methods can also be applied to help speed the comparison of different configurations and test conditions.

HMM (human metal model) is a broadly used term for system and device models which approximate a human body with a metal object (such as tweezers) making the final contact (see Figure 1) to a semiconductor device installed on a circuit board. As a byproduct of ESD "gun" (also confusingly referred to as "simulators") developed to mimic this type of event, these discharges create substantial E- and H-fields in the RF/EMI spectrum that can couple throughout the nearby circuitry and not just the devices in the nodal circuit model. Additionally, the wide range of calibration tolerances in the IEC definition for gun compliance leaves room for dramatic variances in current pulses currents (Figure 2) and total energy (Figure 3), and thus measured robustness and repeatability between guns, between labs in different locations, between testing dates at the same location and between system configurations.

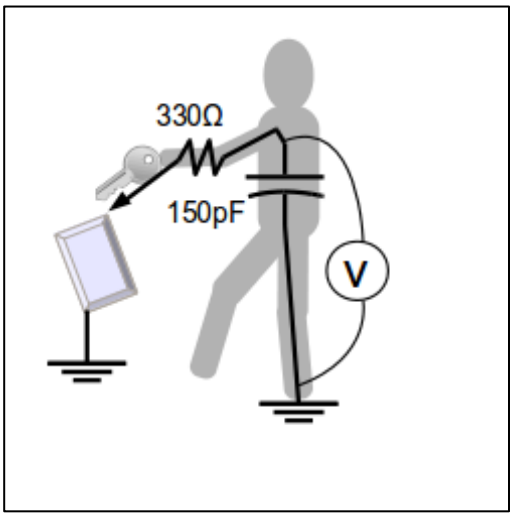

Figure 1: IEC 61000-4-2/ISO10605 human metal model representation

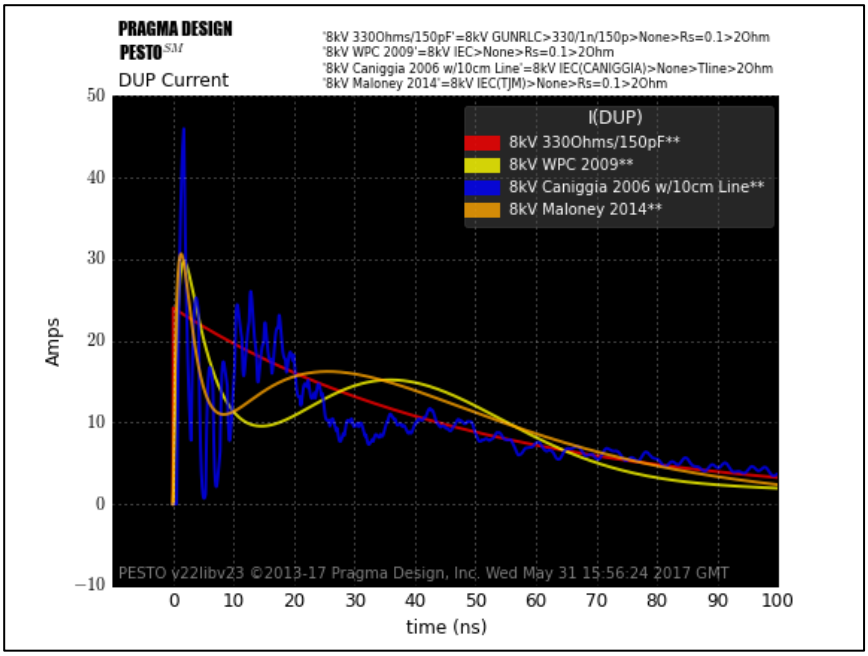

Figure 2: Several simulation models of IEC61000-4-2 gun "emulators"

Other forms of very common and destructive or disruptive ESD discharge models are likely in the field, such as cable discharge events (CDE) and charged board events (CBE) which can be far more destructive to semiconductors at the same charge voltages (higher current and rise time), and can be more prevalent in an application other than HMM/IEC. While there are some tight correlations between energy failures of components in TLP and IEC testing, there are wide differences in CDE and CBE conditions, failure modes and levels (see References at the end of this article).

How does a Designer Deal with So Much Uncertainty?!?

Fortunately, there is a beachhead of sanity carved out on this Island of Misfit ESD Toys. System-efficient ESD design (SEED) or SEED Co-Design utilizes nodal simulation of protection devices interacting with the devices they are intended to protect on a board. This provides a virtual characterization lab where various protection schemes can be at least quantifiably compared for robustness under repeatable settings. It is also possible, through lab verification and validation to associate these results with a minimum threshold of robustness on the IEC61000-4-2 table, and also in the field.

Existing Limitations for ESD Design

First order protection circuit design analysis is often based on datasheet parameters of transient voltage suppressors (TVS) devices, such as ESD Rating (V_{ESD}, IEC61000-4-2 robustness rating, etc.), and clamping voltage (V_{CLAMP}), etc. However, these parameters are usually tested under the one condition which they will never see in a circuit, that is, *by themselves!*

Since TVS devices (here, the device under test, or DUT) are always included in a circuit in order to divert strike energy away from a device under protection (DUP), the actual clamping voltage at the TVS leads to a voltage at the protected device (VDUP) during a strike that is not the same as what

might be promised on the TVS datasheet. The current diverted by the DUT (I_{SHUNT}) is not 100%, and the residual current into the protected device ($I_{RESIDUAL}$) is also not 0% (see Figure 3).

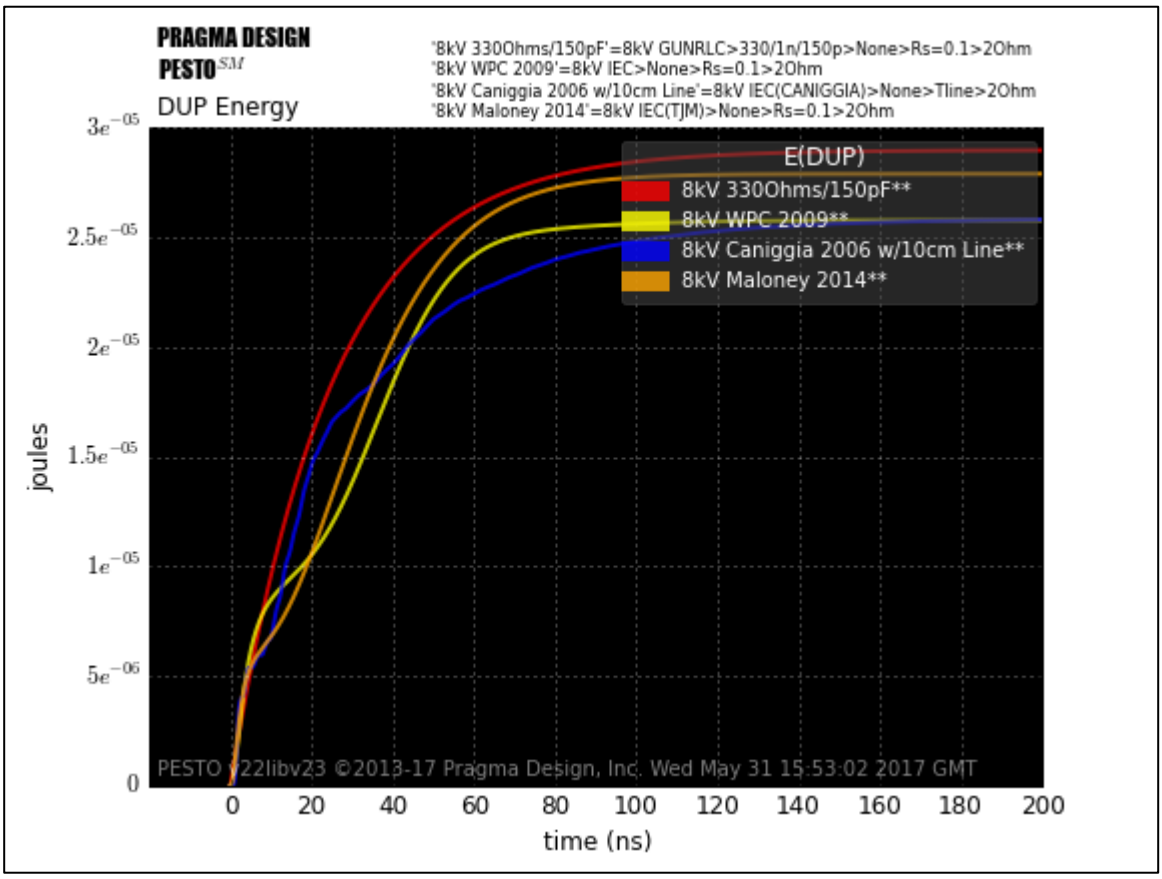

Figure 3: Different gun model total energy delivered into 2 ohms

Second order modeling of this interaction comprehends the Kirchoff's Current Law (KCL) current division between these two dynamic devices, and the current, voltage, power and energy maximum limits which can cause latent or permanent damage in either the DUT or DUP (or in even the PCB traces themselves if the pulses are sufficiently energetic). Most device IBIS or SPICE models available today provide information about "clamping devices" in device I/O's, but these elements were intended to model signal integrity issues like overshoot and ringing within 5-10% above and below VDD and VSS. ESD/EOS strikes inject levels 1000x or more than that are contemplated in those models, and while simulators will happily extrapolate those models out to +/- 50 amps peak for a 4mA clamp, there is no information on when the device will fail and how it will behave on the way there and beyond.

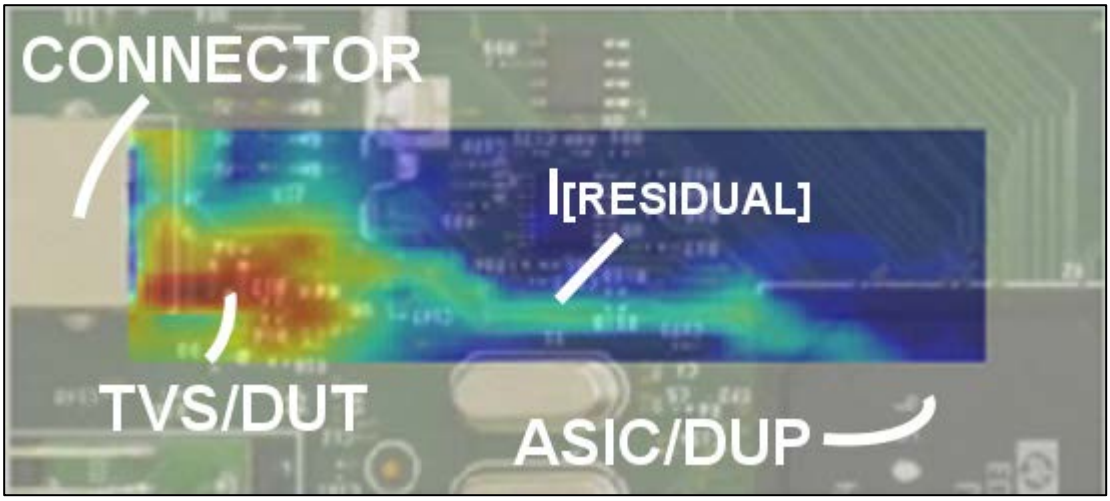

Figure 4: Actual current reconstruction scan of residual current path after TVS clamp (DUT) and ASIC to be protected (DUP)

Given meaningful device models in the ESD/EOS regime, this level of approximation provides superior estimations of the system level robustness for a given *conducted* pulse applied to a given node for the specific devices. However, it still does not necessarily address soft errors, system upsets, secondary discharges or coupled/induced pulses into adjacent conductors and devices.

Third order modeling attempts to virtualize the entire 3D system assembly and solve the aggressor E- and H-field interactions predicted by Maxwell's equations. Given the exorbitant amount of accurate physical and electrical model input required, this can theoretically provide the most complete and accurate representation of an ESD/EOS strike on a system. It is also extremely difficult and time consuming to assemble a meaningful representation of the system. While elegant and expensive 3D field-solvers are commercially available and extremely powerful, given the dearth of accurate ESD-regime electrical models for devices, they can also produce prodigious amounts of “garbage-in, garbage-out.”

For most quantitative “compare and contrast” analysis, though, the second order analysis with accurate models can provide excellent results for “better or worse” analysis. But no simulation under any circumstance should be assumed to answer all questions, nor be extrapolated outside its limited sphere of valid inputs. The pass/fail criteria of a system are defined at the system level.

For example, one TVS device may clamp harder and faster than another device. This additional shunt current may inject undesirable currents and rise times into power rails or ground, causing secondary upsets on other devices. Assumptions outside the scope of any limited simulation are not necessarily valid.

Questions and Considerations for Simulation and Emulation of ESD Events:
The following is a list of items to resolve before diving into ESD robustness analysis and optimization on the virtual workbench or actual test table:

- What are the system level ESD protection requirements? What kind of “aggressor pulse” given ambient voltages, charge capacitance and discharge impedance is the system likely to be subjected to in the user environment?

- What type of lab emulation model is appropriate to represent the “aggressor pulse” definition above? Is HMM, CDE or CBE applicable? All of them? A customized model for a particular application unique to the product environment?

- Do minimum regulatory requirements exist for the system? Are they sufficient to ensure acceptable return/failure criteria in the field for your product?

- What circuit simulation platforms are best suited? Online simulators with integrated libraries? Open Source and Free SPICE simulators? Commercial licensed platforms?

- Where do I get the models to simulate with? What are the model sources and data sources for those models? Are they worst case, typical or “best in class” marketing attempts to gain design wins?

- What circuit models are available for the DUT and the DUP? IBIS? SPICE? Are they applicable to the ESD aggressor pulse regime (10-60A peak, <1ns rise times, etc.) or are they merely intended for small-signal signal integrity modeling?

- Who is providing the device models? Commercial vendor on their best performance data? 3rd party measurements of actual devices?

- What are the failure criteria for the device models? Peak current or voltage? Total energy per pulse? Integrated power to fail? I^2t fusing? Combinations?

- Are the parasitic elements of the simulation sufficient (or necessary) to predict the failure mode? For example, does the model create inductive spikes that replicate gate oxide breakdown voltages accurately, and/or do the devices have that kind of structure that needs additional elements?

- How do I ask a vendor any of these questions if they have never heard of “SEED” in the first place? How to get through the first application engineering layer of a semiconductor vendor and all the way to the TLP/ESD expert in a TVS or ASIC company?

- What “gun” model is to be used? Characterize a model specifically to match the gun used in your qualification lab? A worst case model for all guns? An array of aggressors including IEC, CDE and CBE?

- How much simulation and emulation is enough? Is there a limitation on the amount of BOM costs which can be allocated to protection strategies? Does a simulation need to be done anyway to identify how much margin or risk is likely without additional protection?

- How can the results of the simulation be validated in the lab? Are there industry test methods available or characterization labs which can be hired? Are there baseline tests and models which can be run as a test bench for the simulator? What should an evaluation board look like for correlation testing?

- What about EOS that is not related to ESD? can other pulse types (surge, lightning, electrical fast transients) be modeled with SEED methods? Are the ESD models necessarily applicable? Are there different failure criteria?

About the Author: Jeffrey Dunnihoo *is the founder of Pragma Design in Austin, Texas; specializing in interface design architecture and ESD, EOS, and other transient analysis. He has presented at conferences sponsored by the IEEE EMC Society, the EOS/ESD Association, and ISTFA, and has recently co-authored a new textbook with other ESD experts on ESD co-design fundamentals. He has also been a contributor to industry groups and standards bodies, such as USB, IEEE 802.11, VESA/DisplayPort, and the ESD Industry Council, and has served on EOS/ESD Association, Inc. systems and testing working groups. He can be reached at jeffhoo@pragma-design.com.*

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