Next Generation Charged Device Model ESD Testing

The charged device model (CDM) describes the electrostatic discharge (ESD) event that occurs when an integrated circuit (IC) is rapidly charged or discharged through a single pin to a metallic surface [1]. Because this type of stress can occur in automated manufacturing and handling environments, ensuring device immunity to CDM is increasingly important. Standardized device-level CDM test methods have existed since 1999 [2] and have been crucial for IC characterization and hardening. While these methods have been improved upon throughout the years, some fundamental limitations remain. This article describes the limitations of the existing ANSI/ESDA/JEDEC CDM standard [1], why these limitations are a growing concern, and the likely path toward next-generation CDM testing.

Q: Today, how do CDM testers generate stress?

An illustration of the CDM tester is shown in Figure 1. The IC is placed on a field plate, and the voltage of that plate is then set to the desired value. This brings the potential of the IC to nearly that of the plate. The formation of a spark between a package pin and an approaching grounded pogo pin initiates the electrostatic discharge as the capacitance between the IC and field plate is rapidly charged. The pogo pin connects to ground through a 1 Ω disk resistor. The voltage across this resistor provides a measurement of the current during the discharge and is measured via a 50 Ω coaxial cable to an oscilloscope.

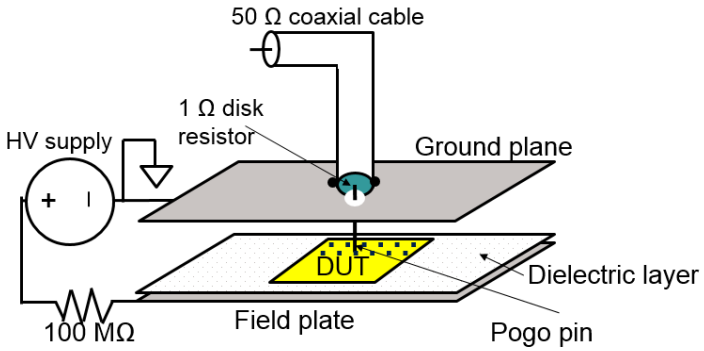

Figure 1: Illustration of the CDM tester used in the ANSI/ESDA/JEDEC standard.

The magnitude of the stress current through the device under test (DUT) is a function of the precharge voltage and the capacitance between the DUT and the field plate. CDM robustness is typically quantified in terms of the precharge voltage. At today's recommended voltages of 250 V [3], an IC could experience between 2 to 5 Amperes of current depending on the package size. Pulse widths are on the order of 1 ns.

Q: What's the problem with the existing method?

As noted earlier, the stress is initiated by an air spark. While this physically resembles the discharge mechanism that can occur in a manufacturing environment, the air spark is inherently variable. The spark characteristics are dependent upon many factors, including humidity, approach speed, pogo pin dimensions and cleanliness, and precharge voltage [4]. The result is a test standard in which the peak current varies – sometimes severely – from zap to zap. Ideally, standardized methods should have no appreciable variation.

Until a few years ago, most products were qualified to 500 V CDM levels or above. As shown in Figure 2, the maximum zap-to-zap variation as a percentage of the mean is approximately 10-15% for precharge voltages greater than 250 V. While undesirable, this variation is not overwhelming and has been viewed as a necessary trade-off in favor of generating a "realistic" ESD event.

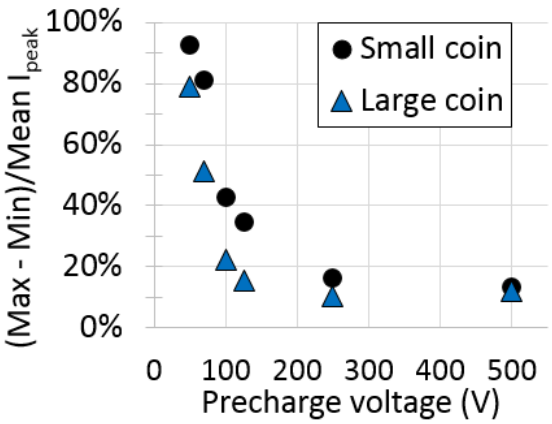

Figure 2: I_{peak} maximum - minimum (top) and the standard deviation (bottom) of 50 zaps to JEDEC calibration coins as a percentage of the mean; 26% relative humidity. Data taken using an 8 GHz oscilloscope.

To satisfy scaling and circuit performance demands, qualification levels of 250 V are now increasingly common. In the near future, components designed for less than 250 V CDM will become necessary [4], [5]. The CDM protection levels for non-exposed intra-package I/Os (e.g., through-silicon vias) is likely to be well below 100 V CDM [5]. When testing below 250 V, the variability transitions from inconvenient to intolerable. As shown in Figure 2, the variation in I_{peak} as a percentage of the mean increases as the precharge voltage V_{pre} decreases. The data in Figure 3 reveal that while the maximum I_{peak} is linearly proportional to V_{pre}, the minimum I_{peak} is not. Runt pulses are increasingly common and the attenuation more severe as the V_{pre} decreases, which in turn decreases the mean.

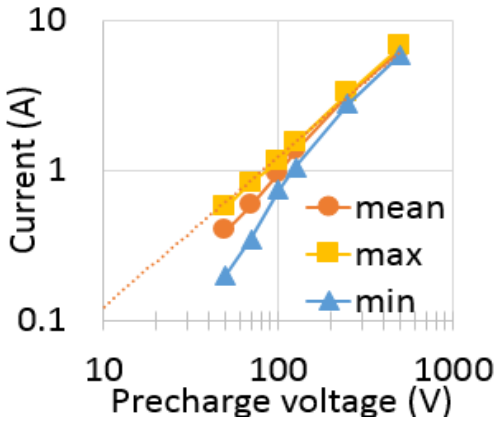

Figure 3: Maximum, minimum, and mean I_{peak} as a function of precharge voltage when stressing the small JEDEC coin.

A repeatable, reproducible alternative to FICDM must be adopted to prevent a significant increase in the testing and design time wasted to accommodate a highly variable standard.

Q: What could be done to reduce or eliminate the pulse variation?

In lieu of an air spark to initiate discharge, a relay can be used to provide consistent, humidity-independent switching. This was proposed as early as 2003 in a method known as capacitively coupled TLP (CC-TLP) [6]. In 2010, a relay-actuated CDM-like tester known as “CDM2” was introduced [4]. In both systems, a relay is used to generate a square transmission line pulse that charges or discharges the DUT and the associated capacitance between it and the tester plates. This concept is illustrated in Figure 4. In the case of CC-TLP, the square pulse is launched by the relay towards the device. In the case of CDM2 the relay is used to slowly charge the device and the coaxial cable connected to it, and then rapidly discharge them.

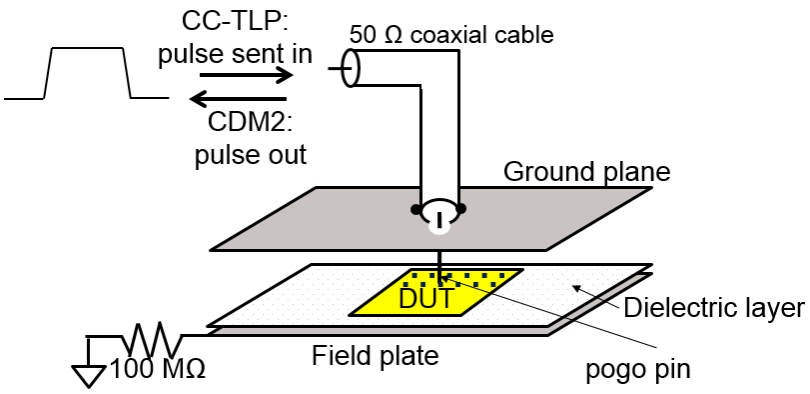

Figure 4: Conceptual illustration of CC-TLP and CDM2. Both use a relay to initiate a square transmission line pulse through a 50 Ω system.

In both CDM2 and CC-TLP, the system impedance is 50 Ω – i.e. that of the coaxial cable connected to the discharge head. However, the impedance of a CDM event is primarily that of the spark, which is on the order of 20 Ω [7]. Recently, a relay-based system was proposed in which the system impedance is reduced below 50 Ω in an effort to more closely approximate the low spark resistance of CDM [8]. As shown in Figure 5, two coaxial cables connected in parallel extend to the pogo pin. Optionally, an additional parallel impedance can be added; this can be either a resistor or additional coaxial cables. The effective system impedance at the pogo pin connection point is now the parallel combination of the two 50 Ω cables and any additional parallel impedance.

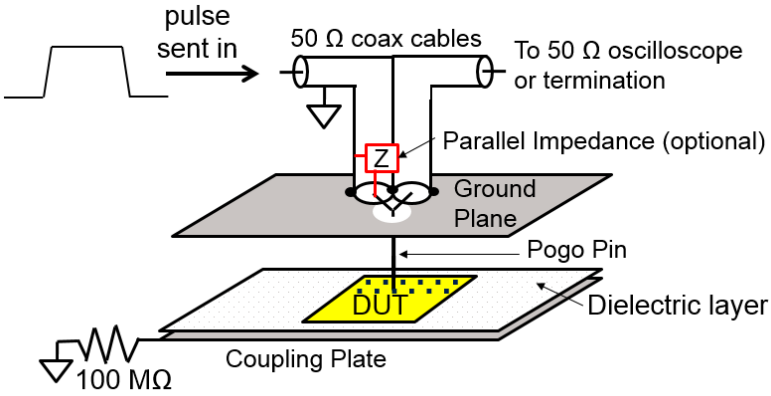

Figure 5: Illustration of low-impedance contact CDM. Parallel impedances in the pulse delivery network reduce the system impedance below 50 Ω.

In all of these relay-based testers, displacement current generates a non-square CDM-like stress ***after*** contact has already been made between the pogo pin and the DUT. **Because contact between the pogo pin and the DUT is made before stress occurs, these systems are often referred to as contact CDM, or CCDM.** Any spark would occur in the controlled environment of the relay, making the stress highly repeatable.

Q: How well does contact CDM correlate with the legacy tester?

Because the legacy CDM tester has been successfully used for decades to assess device-level CDM risk, it is desirable that any alternative test method replicate the stress of the legacy tester. Ideally, both the waveform shape and the device failure mechanisms should be similar.

A comparison of the discharge waveforms from legacy CDM and CCDM when stressing calibration coins is shown in Figure 6. The larger system impedance of 50 Ω CCDM results in a slower discharge and broader

pulse than that of legacy CDM. By decreasing the system impedance, one can tune the system to approximate the legacy CDM waveform; an impedance of 11-16 Ω achieves a close fit for large and small devices [8]. Alternatively, recent work on CC-TLP demonstrates that the width of the transmission line pulse can be narrowed to prevent full charging of the DUT [9]. In this way the waveform can be truncated to achieve a narrower pulse width.

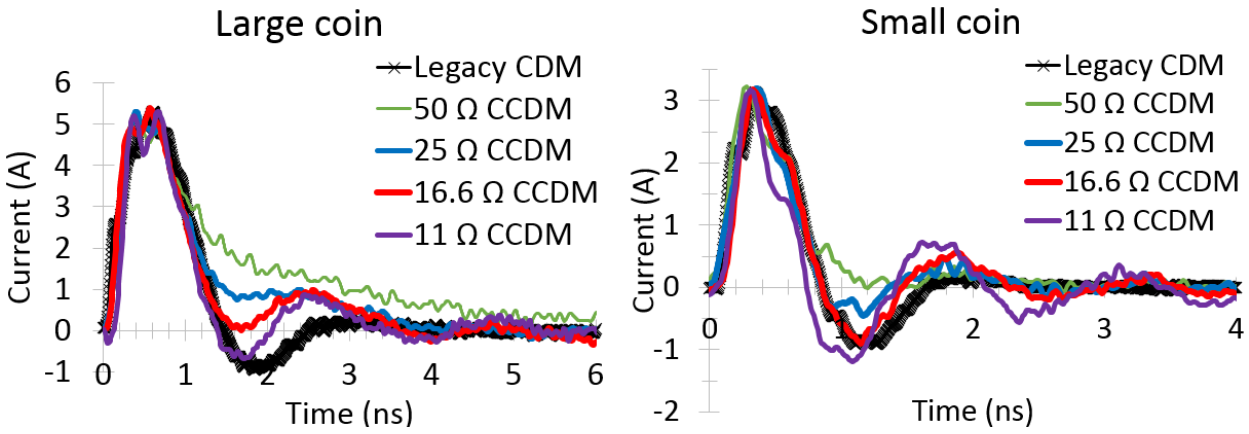

Figure 6: A comparison of the discharge waveforms from the legacy CDM tester and CCDM testers of various system impedances. Calibration coins are used as the DUT.

Several published and unpublished studies have examined the correlation of the induced damage and failure thresholds of CCDM vs. legacy CDM. It has been shown that while the wider pulses of a 50 Ω system are more severe on certain pins, strong correlation is achieved when the CCDM pulse widths are tuned to approximate legacy CDM [8]. To-date, this has held true for both CC-TLP using truncated pulses [9] and low-impedance CCDM [8]. Further correlation studies are necessary and are underway, but all indications are that the legacy stress can be preserved through relay-based systems through careful system design.

Q: What might future CDM test standard documents look like?

Future CDM standards must allow the use of relay-based testers. This could likely be achieved while simultaneously preserving support of the legacy tester. Such a standard might look like the following:

1. Specify the critical parameters and corresponding tolerances of the discharge waveform. These could include the rise time and pulse width at the 20% and 80% points. Do not specify how the pulse itself is generated.
2. Specify the dimensions of critical tester components such as the field plate, ground plane, and the separation distance between these. These dimensions influence how the charge is distributed across the device.
3. Define a look-up table specifying the required peak current as a function of device capacitance and legacy precharge voltage.
4. Refer to CDM robustness levels in terms of the peak current in addition to the equivalent legacy precharge voltage. It is the peak current, not the precharge voltage, which damages the device. CCDM testers will require different precharge voltages to generate an equivalent peak current. Yet, the legacy precharge voltages have served as a guide to those in factory ESD control and must be preserved.

While such an approach must be validated, it opens the doors for innovation and improvement in this crucial ESD test method. The future of CDM testing looks to be one of improvement and innovation.

References

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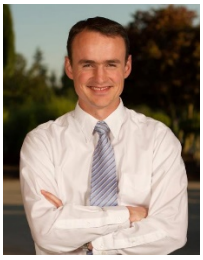

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