ESD Association

ESD Open Forum

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Q: We have a 466-ball IC component with 8 independent power and ground domains and the test time is quite long to do the Human Body Model (HBM) test on an individual component according to either the JEDEC or ESD Association HBM Standards. In the near future, we expect to have IC components with more than 800 pins and 12 independent supply pins. Is there any work in the Standards Groups to reduce the total HBM test time, as it is becoming a major issue in completing HBM qualification tests in a reasonable amount of time?

A: Both JEDEC and ESD Association HBM Work Groups have continued to make changes to the HBM test methods to reduce the total test time required for HBM qualification testing. The original Mil STD 883 method 3015.7 test method [1] required five stresses applied to each pin on the IC component with a one second delay between pulses. Fortunately, the most recent HBM test methods have significantly changed these requirements. The current standards now only require a single pulse to each pin and the delay time between pulses has been reduced to 0.1 seconds. In addition, the JEDEC HBM standard [2] has recently modified how many power pins needs to be stressed if the IC package incorporates a power and ground plane. If the supply pins are shorted in the package, then as few as one pin would need to be HBM stressed. The changes that have been made to date have helped reduce the total test time, but the problem continues to be a serious issue. Several alternative test methods have been proposed and are now under consideration.

The HBM test methods, as defined in both the JEDEC [1] and ESDA [2] HBM standards, clearly describe specific pin combinations that must be stressed. In both documents, Table 2 defines how to stress a single pin to each independent power and ground pins as well as to a group of non-supply pins (signal pins) shorted together. In a Conformity article written by Robert Ashton [3], he explained that the HBM test time increases dramatically when an IC component has large number of independent power and ground supply pins. This increase in test time occurs because Table 2 requires that each pin under test needs to be HBM stressed to all independent power and ground pins.

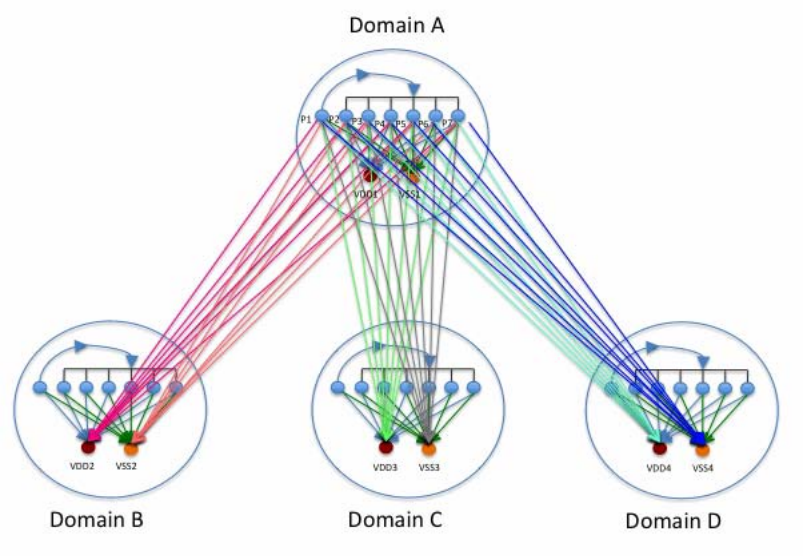

Figure 1 shows a simple case where 7-pins must be stressed to their local power and ground pins in domain A and again for three additional supply domains, B, C and D.

In Reinhold Gaertner's paper [4], he presents data that shows a new alternative HBM test method that simplifies the pin combinations used for stressing each pin. He calls this alternative test method the "Partitioned HBM Test Method" and he proposes that each pin be HBM stressed to its local power and ground pins but not to all other independent power and ground pins. Instead, the new test method requires that only the power and ground pins for a single domain be stressed to each of the other independent power and ground pins. This change in the pin combination test requirement dramatically reduces the total test time for complex IC components because each pin does not have to be stressed repetitively to each independent power and ground domain. In an example in his paper, he shows the case that an IC component with 31 independent supply pins and 185 IO pins, the number of pin combinations can be reduced from 15300 to 4750 zaps. As a result, the test time is reduced by almost 1/3 the normal test time.

The Partitioned HBM Test method reduces the test time by removing a large percentage of pin combinations from the test method. All of the pins of an IC component are fully tested to its local power and ground pins, so any weakness in the design of the actual ESD circuits and IO drivers could potentially be found during these tests. Any special layout interaction between pins would be found so the ESD performance in the local domain would not change. The one basic change that would occur would be the elimination of HBM cross-domain stresses for individual pins. The power and ground pins cross domain stress would still be present so very weak cross domain ESD designs would most likely be found. The fundamental question that this proposed alternative test method raises is: "What is the relative risk associated with HBM stress between pins in one domain and power and ground pins in a different domain?". The assumption in this proposed test method is that the probability that this type of HBM event is not that common, so the risk is low.

The other assumption is that if the ESD circuits are robust in their local domain and if the cross power and ground stress to different domains is robust, then the risk of damage at low stress HBM voltages to a pin stress in another domain is low.

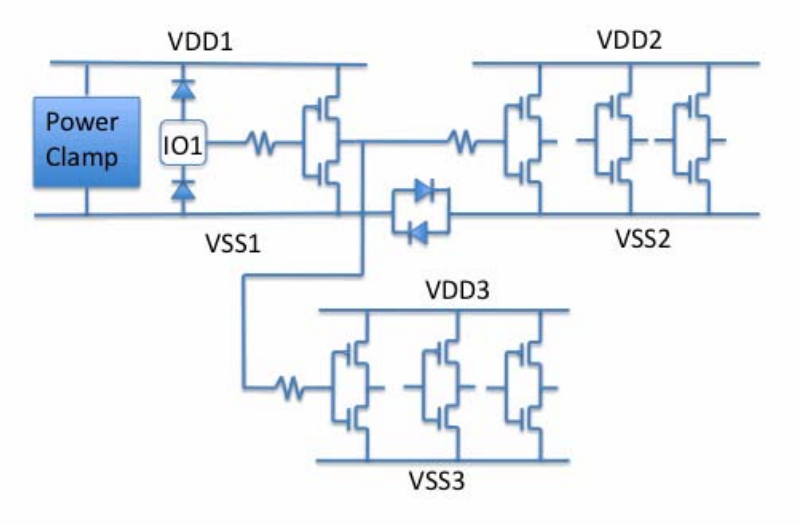

Figure 2 shows a schematic of an input signal from power domain 1 (VDD1) to CMOS inverters in power domain 2 (VDD2) and power domain 3 (VDD3).

If a pin interacts with another circuit in another power domain, the most likely interaction would be signals from the pin through cross-domain CMOS inverter circuits. This type of signal interaction is shown in Figure 2. The other type of interacts would be due to parasitic bipolar devices due to the placement of diffusions placed near one another. The proposed test method would fail the first type of interaction since the local power supply to different ground supply would be tested. The second interaction would not be detected by this test method, since the parasitic bipolar device requires the stress of the signal pin.

There are other alternative test method ideas that have been proposed for test time reduction. One of these ideas argues that since many of the IO and signal pins placed on the silicon are designed and laid out from common standard cell libraries, HBM stressing of all of these identical pins is not required for complex high pin count IC components. Instead, a subset or sample of IO and signal pins would only need to be HBM stressed. This smaller sample of pins would be stressed to the standard JEDEC or ESD Association's full test methods including the standard Table 2 Pin combination table. The test time reduction would be achieved because a smaller number of pins would have to be stressed.

The pin sampling method appears to be a quick and easy method for reducing the HBM test time. Since only a sample of pins is HBM stressed, the test time reduction could be easily determined. Since all like IO and signal pins are tested, the ESD properties of an individual library cell could be determined.

The conversion to pin sampling HBM test method would not be easily implemented. Several important questions would need to be resolved before this type of method could be standardized:

1. How are the signal pins selected for sample testing?
2. How many pins would need to be selected?
3. Should the sampling method require a minimum number of identical pins?

Although identical IO and signal pins appear to be the same when viewed from the standard library, the placement of these cells on the chip and the placement of the nearest power and ground pins changes their ESD high current properties [5]. In addition, the ESD properties may

also change depending on the left or right orientation of the IO cell with respect to an adjacent IO cell. This makes the sampling pin selection process more complex than just selecting pins randomly. Detail knowledge of the layout of the IO cell would be required before a detail HBM test plan could be implemented. Since the user must select the small set of pins to be HBM stressed, this opens the test method to possible manipulation to achieve desired HBM test results. If a certain pin in the selection process fails the HBM stress at some critical voltage level, the user could potentially select another pin sample and theoretically obtain different test results. Since the pin selection process is very design specific, standardization of this method could be more problematic.

The increased complexity of IC components with increasing number of pins or balls in the package combined with additional functionality that multiplies the number of independent power supplies has resulted in extremely long time to HBM stress an individual IC component. Reduction in the number of zaps, times between zaps and in some cases reduction of supply pins to zap, have helped to reduce the HBM test time. Even with these changes, the HBM standards still need to be improved and more test time reduction improvements need to be made. Two new ideas are under consideration by both JEDEC and ESD Association Work HBM groups, the “Partitioned HBM Test method” and the Pin Sampling method.

References

1. Mil STD 883 method 3015.7 (1989)

2. EIA/JEDEC Standard, Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM), EIA/JESD-A114F, 2008

3. ESD Association Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing, Human Body Model (HBM) Component Level, ESD STM5.1 2008

4. R. Ashton, “Human Body Model: The Hidden Challenges”, Conformity Magazine, Jun 2008

5. R. Gaertner, R. Aburano, T. Brodbeck, H. Grossner, J. Schaafhausen, W. Stadler and F. Zaengl, “Partitioned HBM Test – A New Method to Perform HBM tests on Complex Devices”, EOS/ESD Symposium 2005, p 326

6. Private Communication Robert Ashton