ESD Open Forum

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Q: *Is there a problem with the ANSI/ESDA STM5.1Human Body Model (HBM) 2-pin current waveform verification test procedure?*

A: There is no simple yes or no answer to this question. The 2-pin current waveform verification test procedure is still correct, but it may be not be achieving its original purpose. The component level HBM standard test method ANSI/ESDA STM5.1 [1] requires that a 2-pin peak current waveform measurement be performed to verify that the HBM simulators are operating correctly. The measured waveform is compared to established calibrated waveforms in the test method and to appropriate peak current versus applied HBM stress voltage tables. The STM5.1 measurements use both a short wire and a 500-ohm resistor that is placed into any two pins in a socket. The fundamental assumption that has been made for the past 18 years has been that the discharge current waveforms for a 2-pin test were the only tests required to control the HBM simulator test parasitics. Today, this fundamental assumption is in question [2].

The existing STM5.1 HBM component level test methods all originated from the Mil-Std-883 Method 7 notice 8, which was release in 1989. At that time, the largest IC packaged components used only 40 pins or leads. The first HBM simulators were 2-pin manual simulators where the high-voltage pin was placed directly into terminal A and the ground pin was placed into terminal B. These very basic systems discharge current waveforms were at first verified by just a short circuit wire placed between terminal A and terminal B. The basic assumption made at that time was that the interaction between the HBM simulator test system parasitics and the IC component were quite small.

In 1990 the first relay matrix 64-pin and 256-pin HBM simulators were introduced into the market. The introduction of the relay matrix test equipment allowed the user to write test software programs that automated the 2-pin test manual procedure. The new HBM simulators also included a new automated curve trace parametric analyzer. The new relay matrix system allowed software to control the operating state of the IC pins in the socket. The user could define which pins were stressed, grounded, or were to be left floating or disconnected.

Although the complexity of the HBM simulator had significantly increased with the introduction of the multiple relays, the 2-pin waveform verification test procedure remained unchanged. The ESD Association WG5.1 introduced in 1991 a new HBM standard test method [3] that added a new 2-pin 500-ohm waveform requirement. This new waveform requirement was added to limit the newly discovered test board capacitance tester parasitic problem. HBM tester correlation studies showed that different HBM simulators produced different current waveforms and variable rise time values to a 500-ohm load during the 2-pin test. In 1993, Koen Verhaege reported that a new HBM equivalent circuit had been developed that accounted for many of the known “2-pin” relay-matrix HBM simulator tester parasitics [4].

Even with this new equivalent circuit model of the HBM simulators and the introduction of the 500-ohm resistor verification test, tester-to-tester correlation problems still continued. This miscorrelation problem could not be explained because in many of the cases both HBM

simulators met the 2-pin short and 500-ohm load peak current waveform requirements for each pin in the simulator.

This miscorrelation problem has persisted through the late 1990s and continues to live on until today. In 2006, the ESD Association WG5.1 published a HBM tester parasitic paper [1] that expanded on the work that Koen Verhaege had reported in 1993. This new research work introduced a new method for calibrating the short circuit and 500-ohm load discharge current waveforms. The 2-pin short circuit verification method was replaced with a multiple pin short circuit wire configured as an IC chip. For the first time, the discharge current waveform test method could measure all of the relay-matrix tester parasitics. These new parasitics could now be added to a more complete equivalent circuit for relay-matrix HBM simulators.

The paper reported that there existed other tester parasitics that the existing 2-pin verification method could not identify. The complexity of the interaction of the IC component and the HBM simulator could not be fully analyzed using this 2-pin test technique. A new verification methodology was needed to uncover these hidden parasitic elements.

The basic lessons learned from this research found that as the ESD test equipment becomes more complex, the test system verification test procedure also needed to be improved and updated. If new test equipment still has miscorrelation problems, then this is a clear indication that the verification procedure is still inadequate and needs more work. As the ESD test equipment continues to adapt to the changing IC components and complex packages and number of pins, the HBM verification test procedure must be carefully reviewed. The procedure is not a finish measurement until all major tester parasitics that interact with the IC component can be clearly identified. After this result can be accomplished, then the test method and test equipment can be used with confidence to truly measure the HBM performance of just the IC component, and not the interaction of between the test equipment and IC component.

References:

1. ESD Association Standard Test method -S5.1-2001, for ESD Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM)- component Level, 2001.
2. M. Chaine et al., “HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Groups”, Proc. EOS/ESD Symposium 2006, pp111-113.
3. EOS/ESD-S5.1-1991,” in Standard for ESD Sensitivity Testing – HBM- component Level, June 6, 1991.
4. K, Verhaege et al., “Analysis if HBM Testers and specifications using a 4th Order Lumped Element Model, Proc. EOS/ESD Symposium 1993, pp129-137.

About the Author

Michael Chaine is a Fellow Technical Member at Micron Technology, Inc. in Boise, Idaho. He holds a BSEE degree from Arizona State University and has worked at Micron since 1998. Today, he is working in the R&D Reliability Group as the ESD Section Manager supervising three ESD engineers.

He is currently working in the area of On-Chip ESD protection design for all advanced DRAM and FLASH and CMOS Imager technologies. This activity focuses on ESD wafer and device level characterization analysis, ESD circuit failure analysis, and ESD design and layout rule development.

Mike has authored several papers on a variety of ESD areas ranging from ESD device test issues, ESD protection circuit analysis and unique ESD circuit interaction phenomena. In 1994, Mike received the EOS/ESD Symposium Best Paper Award. In addition to publishing papers, Mike holds 9 ESD patents and has several patents pending.

Prior to working at Micron Technology, Mike worked at Texas Instruments as a member of the Group Technical staff from 1990 to 1998. He worked as the EOS/ESD Section Manager for the MOS Memory Reliability Group.

Mike has been actively involved in the ESD Association since 1993. He is the chair of two different IC device test work groups, the component levels Human Body Model (HBM) WG5.1 and Socketed Device Model (SDM) WG5.3.2. He is a former member of the ESDA Board of Directors.

About the ESDA.

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org**.