ESD Open Forum

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Q. The Industry Council on ESD Target Levels has proposed that OEM (Original equipment manufacturer) reduce their Human Body Model (HBM) minimum passing stress voltages from 2000 V to 1000 V [1], how does this recommendation affect the existing HBM test standards?

A. The HBM test standards, ESDA STM5.1 or JESD22-A114E, both define how to perform the HBM test, what type of ESD equipment to use and a method for validating the discharge waveforms. Each standard defines HBM classification levels as a way to compare the electrostatic sensitivity levels between different IC components. Thus, the standards do not set any specific HBM requirements that an IC component must meet. The end customer (OEM) who is purchasing the IC component defines the minimum acceptable HBM voltage level requirements.

Q. The Industry Council on ESD Target Levels has reported that the customer factory failure rate for IC components that fail at 1000 V do not have any higher customer return rate than components that fail at 2000 V [1]. Does this new HBM data suggest that the existing HBM standard test methods are too restrictive?

A. This is a good question. The existing HBM test methods were first developed in the late 1980's as replacement test method for the Mil STD 883D, Method 3015.7. When the HBM standard was first developed, the largest IC components tested at that time had at most 64 pins with one Vcc and Vss pin. Some of the first HBM test simulators were manual two pin testers and all testing was done manually. The same test pin combinations, all signal pins (Inputs, I/O, Control pins) were each stressed to the single power and ground pins. In addition, a new pin combination was introduced that required that each signal pin be stressed to each other signal pin. This test combination was quickly modified when the total number of manual pin stresses became extremely excessive. The signal pin to signal pin stress test was modified to the case where each signal pin was stressed to all other signal pins ganged together and grounded.

In today's semiconductor industry, IC components with more than 512 pins or balls are quite common for both low-cost and cost-performance packages [2]. In addition, many of the IC components have a minimum of 4 – 5 independent power or ground pins with as many as 100 power and ground pins or balls. Since the HBM pin combination stress methods have not changed, the total number of HBM stresses for a single test voltage level for this type of device would easily reach 3300 pulses. In contrast the 64-pin IC component built in early 1990's received approximately 640 pulses. In 1990, the HBM standards required that each signal or I/O pin be stressed 5 times per HBM ESD stress level, instead of existing HBM requirements of 1 stress per polarity and stress level.

Even though the existing HBM test method has increased the total number of HBM pulses to a single pin, the HBM Component Level Classification Tables have not changed. All pins in an IC component must pass all pin combinations tests at any given voltage stress level independent of the number of pins in the package or number of HBM stress pulses.

The existing HBM standard classification levels treat a 500-pin IC component with 1 or 2 pin failures the same as a 64-pin package device with 1 pin failure. The existing test methods describe how to perform an HBM stress, but the test methods are missing an important factor in defining the classification levels. As the number of pins or balls increase in an IC component, the probability that a specific pin combination will have an ESD discharge event is ignored. For example if the 64-pin IC component has one pin fail below 2000 V, the pin failure rate would be 1.56% risk of occurrence, while 2 pin failure on a 512 pin IC component would have a 0.4% risk of occurrence. The probability numbers change even more if the probability of the exact pin combination is included. Since the number of different pin combinations for the 500-pin IC component versus the 64-pin IC component is 11 versus 3 for, the above probabilities would be even lower for the high pin component.

None of these probability factors are considered in the existing HBM standard test methods. The probability that a specific pin combination would receive an ESD discharge event becomes much lower as the pin count increases; this information is currently being ignored. Are the existing HBM standard test methods too restrictive? The best answer, in my opinion, is yes; especially for high pin count IC components with multiple independent power supplies.

Q. During the product qualification HBM tests, we stressed a total of 2 IC components from three different wafer lots for a total of 6 parts. Five out of six IC components passed all HBM pin combinations at 4000V, but one device had functional failures at 1500 V. The product was retested with a larger sample size of 12 additional IC components and none of these parts failed. The HBM standards only require a minimum of three samples to be tested, but we have tested a total of 18 samples with only one failure. Why should this product's classification be lowered to 1C (1000 – 2000 V) instead of Class 3A (4000 – 8000).

A. The existing HBM standards allows for repeating HBM tests at the fail voltages with fresh new samples. This step in the test method was added to make sure the failures were not due to some type of wear out failure mechanism [3]. If the new samples pass the new tests, then the HBM tests can continue. If the additional testing shows that the product passes at much higher HBM stress levels until repeatable failure occur, then the classification level will be the highest level reached. In your case, since the repeatable failures did not occur to > 4000 V, the HBM standards allow you to rank your product as a Class 3A product.

References:

1. Industry Council on ESD Target Levels, “White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements”. (http://www.esda.org)
2. INEMI, “2005 Packaging Roadmap Overview”. (http://thor.inemi.org/webdownload/Industry_Forums/Productronica_2005/2007_Roadmap_Kickoff/2005_Packaging_Roadmap.pdf)
3. ANSI/ESD STM5.1-2007 or JESD22-A114E

About the Author

Michael Chaine works at Micron Technology, Inc, in Boise, Idaho, as a Section Manager in the R&D Reliability Group. He holds a BSEE degree from Arizona State University and has worked at Micron since 1998. Today, he is leading the R&D Reliability Group in the area of ESD/LUP design and development and has two engineers reporting to him.

He is currently working in the area of On-Chip ESD protection design for all advanced DRAM and FLASH technologies These responsibilities include ESD wafer and device level characterization analysis, ESD circuit failure analysis, and ESD design and layout rule development.

Mike has authored and co-authored several papers on a variety of ESD areas ranging from ESD device test issues, ESD protection circuit analysis and unique ESD circuit interaction phenomena. In addition to publishing papers, Mike holds more than 10 ESD patents and has several patents pending.

Mike has been actively involved in the ESD Association since 1993. He is a former member of the ESD Board of Directors. Currently, he chairs two different IC device test work groups, the component levels Human Body Model (HBM) WG5.1 and Socketed Device Model (SDM) WG5.3.2. In addition, Mike has been actively involved with the ESD Symposium working in a variety of different positions, currently contributing as Session Moderator for the 2008 Symposium.

About the ESDA.

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org**.