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The Machine Model Standard- ANSI Review 2006

Q: I have just read the ESD Standards Activity update in the March /April 2007 issue of the ESDA Threshold newsletter. It states that Machine Model, MM-5.2 has just completed a 5-year review and will be sent out for voting. I cannot attend these ESD meetings, but our company does use the ESDA documents. Please tell us what changes were made to the document, and when the document will be available for download.

A: Since its last publication there have been developments that require some change to the document. To meet ANSI requirements, a standard must be reviewed every 5 years, and revised and updated where necessary. Since writing the last article, there is significant evidence that component manufacturers have increased their use of the MM standard due to Asian and European auto manufacturer requirements.

Here are the changes that were made

1. Changes were made in the definitions section. Definitions are important to complete the understanding of a document. Several definitions were added including differentiating among active, passive and discrete components, and no connect pins. These definitions, though sounding familiar, had to be added for clarification, and reflect the same definition changes made to the HBM document, which was submitted earlier this year for ANSI review.

2. Changes were made regarding the waveform capture procedure in the Qualification and Verification procedures section. The changes are associated with those new ESD testers that support multiple pulse heads with the pulse generation circuits used to simulate the waveforms. Here, a reference pin pair is defined for each pulse generating circuit, and is relevant to the test fixture board being used. Because of the more-than-one-pulse generation circuit, the standard changed to state that every pulse generation circuit must be tested individually; no daisy chaining is allowed. The waveform from every pulse generation circuit must be verified and all high voltage discharge paths must be tested and verified.

3. The table in the document that identified the measurable parameters and the parameter values for the waveform associated with verifying the results of a 500 ohm resistor measurement was also changed. The peak current at the 100 nanosecond position (I_{100}) was changed from the range of 0.26- 0.32 amps to the wider range of 0.23-0.40 amps. Justification for this was provided with data from circuit simulation and testers collected by at least two companies. Their data showed that $I_{100.}$ was greatly influenced by parasitic inductance and resistance.

4. In the same table, for the same 500 ohm measurement, the current at the 200 nanosecond position (I_{200}) was changed from the range of 35-45% of (I_{100}) to 30-55% of (I_{100}). It is a

widening of the spec, also justified with both simulated and tester-collected data. Even though (I_{200}) is not really influenced by inductance or resistance in the circuit, the peak current value is so small that noise in the tester influences the value. Yes, 30% of 0.23 amps is quite a small number (0.069 amps), but there should be little to no ringing out at 200 nanosecond for a MM pulse using a 500 ohm resistor in the circuitry. See figure 1 for the I_{100} and the I_{200} positions on the 500 ohm waveform. Ipr is the maximum current at 400 volts.

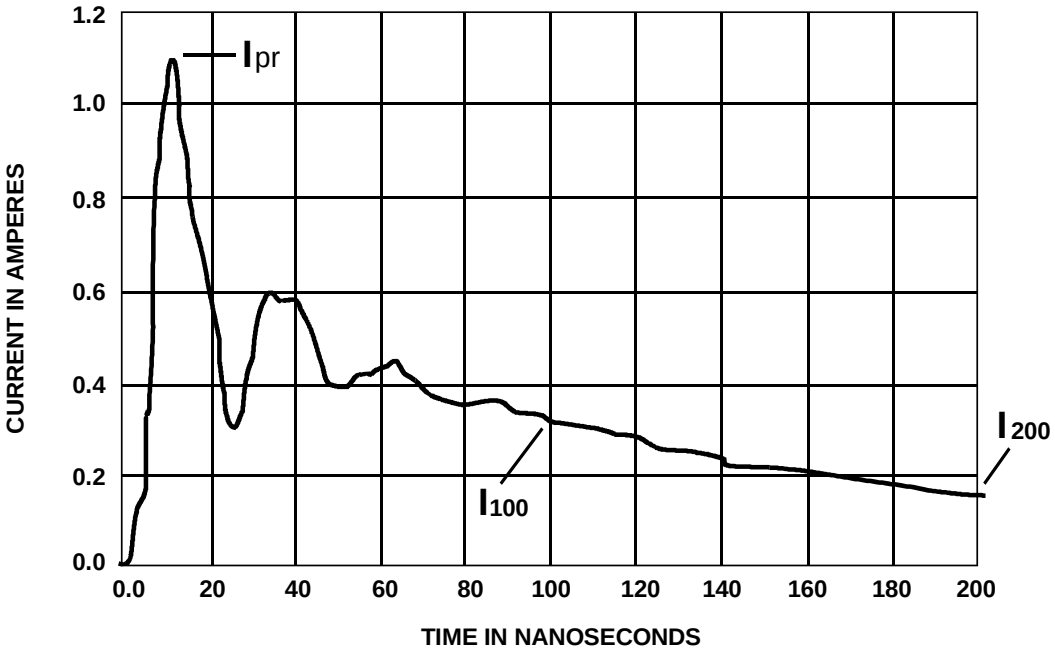

Figure 1: Current MM waveform through a 500 ohm resistor for a 400 volt discharge

5. The next change is the Pin Combination stress testing table for user clarification. Pin Combination (Pin-C) stress testing is becoming more complex as the pin counts in device increases. The Pin-C table in the original document was developed when devices had less than 184 pins in the early 90s. We now have 1000+ pin devices. The old table shows sequence testing (pin 1 to Vss, pin 2 to Vss, etc.) steps from #1 to #14 and assumptions were made for sequence testing step #9 (swapping Vdd and Vss) and sequence testing step #10 (swapping Vdd and Vcc pins). The table simply states that sequence #1 to #8 should be repeated for the Vdd and Vss swap and for the Vdd and Vcc swap. Because of the proliferation of Vdd, Vss, Vcc and Vee pins, the original sequencing was deemed to be inadequate to completely explain the required pin combinations. The new sequencing in the table is fully expanded to the 28 sequences required for the pin count (10 pins) example used in the standard. Now it is quite clear which pin is to be tested against which pin.

6. We did not change our stress pulse per pin to 1(+/-); it is still 3 (+/-) because the ESDA MM WG members collected data during several round-robin evaluations indicating ESD

sensitivity levels could be affected by the reduction of ESD test pulses from 3 to 1. No additional data has been presented to prove otherwise. More information regarding the round-robin evaluations and results can be found in a Technical Report titled *Machine Model (MM) Electrostatic Discharge (ESD) Investigation – Reduction in Pulse Number and Delay Time*, which is available to ESDA members for free download (non-members can contact the ESDA for more information).

Lastly, I cannot resist repeating this: The purpose of the standard is to establish a test method that will replicate MM failures and provide reliable, repeatable results from tester to tester, regardless of component type. Repeatable data will allow accurate comparisons of MM ESD sensitivity levels.

About the author

This article was prepared on behalf of the ESD Association by Dr. Leo G. Henry, an IEEE Senior member. He is a member of the ESDA's Board of Directors, with Chair responsibilities for the Workshops at the 2007 EOS/ESD Symposium. Dr. Henry is also chair/facilitator for the ESDA's Device Testing 5.0 Standard Committee that has several subgroups (HBM, CDM, TLU, TLP etc). Dr. Henry is Founder/CEO for ESD/TLP Consultants, LLC. Dr. Henry has a B.Sc. & M.Sc. in physics from UWI, Caribbean, and an M.S. & Ph.D in Materials Science & Engineering from U.C. Berkeley, CA. He can be reached at 510-708-5252 (Mobile) and at leogesd@pacbell.net or leogesd@ieee.org.

About the ESDA.

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org**.