ESD Open Forum

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Provided by the ESD Association

Q: Will testing my device with a Transient-Induced Latch-up (TLU) test help in isolating transient susceptible device designs?

A: The answer is *yes!* Transient-Induced Latch-up testing, using the ANSI/ESD SP5.4-2004 Standard Practice, has been shown to replicate field failures or failures occurring during burn-in testing, that other standard latch-up test methods have not.

The ESD Association (ESDA) standard practice ANSI/ESD SP5.4-2004 outlines testing techniques that may help reproduce in-field failures, which up till now, have not been reproducible. The ESDA Transient Induced Latch-Up (TLU) working group (WG5.4) developed the Standard Practice based on information gathered from a number of years of experiments using different device technologies. Different transient stimuli's were also evaluated, in an attempt to replicate real world failures. This information is presented in the ESDA TLU Technical Report (ESD TR-5.4-01-00) and can be used as a reference when trying to understand how the Standard Practice was developed and how to implement it.

Since the Standard Practice was released, the work group has focused their experiments on using a *negative going rectangular pulse* as the stimulus. The test requires the device be biased to its nominal Vdd voltage level, the transient pulse generator would then force the Vdd rail negative, holding it there for 20us before returning it to the nominal Vdd voltage. During the time of the pulse, current and voltage measurements on the power supply rail are recorded and used as the basis for determining whether latch-up has occurred. During the event, if there is a sudden and sustained increase in the supply current, then latch-up has occurred. Figure 7, taken from ANSI/ESD SP5.4-2004, shows

an idealized representation of how the stress is applied to the Vdd rail, while the voltage and current measurements are being recorded during the event. Figure 8, also taken from Standard Practice shows the results of an actual device test. Idd current being measured on channel 2 of the oscilloscope clearly shows an increase in the current draw, after the negative going transient event has been applied to the Vdd rail.

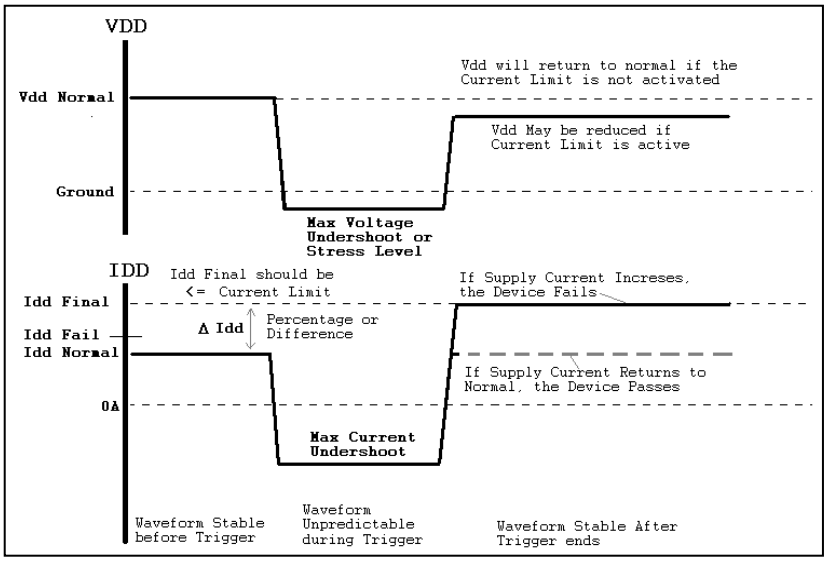

Figure 7: Example of Latch-up failure using Combined Bias/Stimulus TLU (Idealized Oscilloscope Graph)

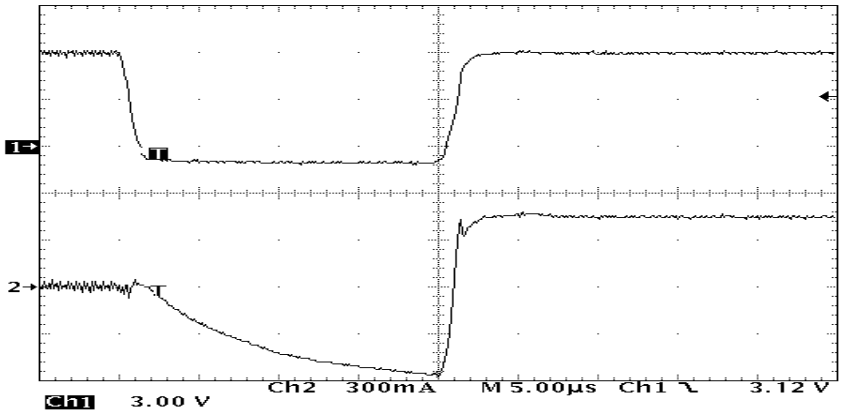

Figure 8: Example of Latch-Up failure using Combined Bias/Stimulus TLU (Actual Oscilloscope Plot)

Unlike other latch-up test methods, which force or sink current on an IO pin, or attempt to over-volt the supply rail, possibly causing an EOS event, the TLU test method introduces a short duration negative pulse, which reduces the time that the trigger current flows thereby reducing the possibility of EOS damage due to over-current or thermal runaway. The committee has also found, that by using this method the transient signal is distributed to all parts of the die powered by the supply under test, greatly increasing test coverage to a larger proportion of the device's structures.

The TLU Work Group (TLU5.4) is in the process of writing a second Technical Report (TR) which outlines some of the recent findings during our additional experiments. This report should be available later this year. Equipment manufacturers are now offering systems that will allow designers to test their devices using the Standard Practice, which will also lead to new discoveries and further improvements in the test methods.

Q: When will the TLU standard practice become a real standard, with specific stress levels and failure criterion?

A: A number of companies have begun to use the method on a wider variety of parts, however, more feedback on the SP's implementation and actual result data is needed by the ESDA working group. This information can help drive changes to the standard practice, which will also drive the SP towards a Standard Test Method (STM).

Please review and implement the Standard Practice and provide feedback on your findings to the ESD Association headquarters.

References

EIA/JEDEC, EIA/JESD78A "IC Latch-Up Test," February 2006

ANSI/ESD SP5.5.1-2004 Electrostatic Discharge Sensitivity Testing Transmission Line Pulse (TLP) Component Level; ESD Association, Rome, NY

ESD TR5.4-01-00 Transient-Induced Latch-up Technical Report; ESD Association, Rome, NY

IEC61000: Electromagnetic Compatibility (EMC); Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test; Basic EMC Publication, ESD Association, Rome, NY

About the Author

Tom Meuse is currently the Product Line Manager at ThermoFisher Scientific, for their ESD/Latch-up simulator product lines. He has worked for ThermoFisher Scientific (formally KeyTek) for over 28 years and has focused on ESD and Latch-up system development and customer technological development. Mr. Meuse is a member of the ESD Association and the chair of Device Level Working Group 5.4 TLU (Transient Latch-up). He became chair of the Working Group, after the departure of Gary Weiss from Lucent, who had championed the development of TLU. He is also a member of JEDEC's JC-14 device level work groups, where he participates in the development on the device level standards.

About the ESD Association

Founded in 1982, the ESD Association is a not for profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors educational programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: http://www.esda.org.