ESD Open Forum
Conformity Magazine
Provided by the ESD Association
October 2007
Dr. Steven H. Voldman
Author

Transmission Line Pulse (TLP) Standard Development

Q: I am interested in Transmission Line Pulse (TLP) testing. Is there a standard practice today?

A: Today the ESD Association has a document for the TLP testing of semiconductor components. The document is ***ESDA DSP5.5.1 Standard Practice for Electrostatic Discharge Sensitivity Testing - Transmission Line Pulse (TLP) Component Level***. The document provides the guidance for the TLP waveform specification, test system and testing methodology. Today, round robin testing of TLP has been completed, and a true Standard Test Method (STM) will be released for the semiconductor industry in 2007.

Q: Why are engineers interested in TLP testing?

A: TLP testing provides the ability to understand semiconductor devices, circuits and chips response to high current pulse testing. One of the reasons TLP testing is popular is that it provides the actual current and voltage across the device under test (DUT). A pulsed TLP I-V characteristic is provided which allows visualization of the semiconductor device response. A second reason is that testing can be completed "on wafer" or on product chips. With this capability, it can be used for semiconductor development, product design, to failure analysis.

Q: Are there TLP commercial test systems?

A: Today there are TLP test systems internationally. Corporations that sell TLP test systems exist in the U.S., Europe, and Asia. These TLP systems provide wafer level or product level testing.

Q: What is the difference between TLP and Very Fast TLP (VF-TLP)?

A: Very fast transmission line pulse (VF-TLP) is a new test method for faster rise times and shorter pulse widths. The ESD Association will be releasing a new standard practice document on VF-TLP. The VF-TLP test method requires a rise time less than 1 ns, and short pulse width between 1 and 10 ns. TLP testing standard practice method is a 100 ns pulse width. Today, the VF-TLP Standard Practice (SP) document is ready for release from the ESD Association, and round robin testing is in process to demonstrate this as a standard test method.

Q: Who is interested in VF-TLP testing, and why?

A: VF-TLP testing provides the current-to-failure and power-to-failure for fast rise time events and short pulses. Today, this is relevant to quantify pulse events in the GHz time regime; hence, this can be used to quantify noise, and pulse events on products, to test systems. With fast events there is also interest for radio frequency (RF) components. Technologists are also studying dielectric breakdown of ultra-thin oxide to quantify the response of fast high current events on dielectrics.

Q: What advantage is there to doing both TLP and VF-TLP testing?

A: First, TLP testing is "HBM-like" in its total energy for a 100 ns square pulse. Hence, TLP testing provides a sense for the anticipated HBM testing results. VF-TLP represents the response to fast pulse testing. By doing both TLP and VF-TLP testing, one will have the power-to-failure for both fast and slow phenomena. This is useful for development of a power-to-failure characteristic for the semiconductor device, circuit, chip or system.

About the author

This article was prepared on behalf of the ESD Association by Dr. Steven H. Voldman. Dr. Voldman is the first IEEE Fellow in the field of Electrostatic Discharge (ESD) in semiconductor devices for Contributions in electrostatic discharge (ESD) protection in CMOS, Silicon on Insulator (SOI) and Silicon Germanium (SiGe) Technology. He has served as Chairman of the SEMATECH ESD Committee from 1995 to 2000, ESD Association Board of Directors from 2000 to 2007, and is presently an Appointed Board Member. He has served as Technical Program Chair, Vice Chair and Chairman of the ESD Symposium from 2000 to 2002. He is founder of the university lecture program known as "ESD on Campus," which provides ESD university lectures in the U.S., and internationally including China, Taiwan, Philippines, Malaysia, and Thailand. Dr. Voldman is a member of the ESD Association Technology Roadmap Committee, Chairman of the ESD Device Testing 5.5 Standard Committee on Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF-TLP) Testing from 2000 to 2008. Dr. Steven Voldman is author of three books, *ESD: Physics and Devices*, *ESD: Circuits and Devices*, and *ESD: RF Technology and Circuits*. He can be reached at 802-769-8368 and at voldman@ieee.org or **a108501@us.ibm.com** .

About the ESDA.

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069 USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org**.