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Dr. Steven H. Voldman
Author

Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF-TLP) Standard Development

Q: I am interested in what is new in the area of Transmission Line Pulse (TLP) testing. Is there a standard practice today?

A: The ESD Association just released the standard test method (STM) ***ANSI/ESD STM5.5.1-2008, ESD Association Standard Test Method for the Protection of Electrostatic Discharge Susceptible Items – Electrostatic Discharge Sensitivity Testing – Transmission Line Pulse (TLP) – Component Level***, which is a revision of the standard practice (SP) *ANSI/ESD SP5.5.1-2004*. Round robin testing of TLP was completed in 2007. This document provides the guidance for the TLP waveform specification, test system and testing methodology. This methodology uses a 100 ns pulse width for evaluation of components.

Q: What about the Very Fast Transmission Line Pulse (VF-TLP) Standard Practice (SP) methodology?

A: The ESD Association has also just released ***ANSI/ESD SP5.5.2-2007, ESD Association Standard Practice for Electrostatic Discharge Sensitivity Testing – Very Fast Transmission Line Pulse (VF-TLP) – Component Level***. This document is the very fast transmission line pulse (VF-TLP) standard practice (SP) for the VF-TLP testing of semiconductor components. It provides the guidance for the VF-TLP waveform specification, test system and testing methodology for this short pulse testing methodology. The VF-TLP testing method uses a shorter pulse width in the range of 1 to 10 nanoseconds. Round robin testing of VF-TLP is in progress in 2008, with an anticipated release of a standard test method (STM) in early 2009. Today, results demonstrate no roadblocks to the methodology; hence, it is anticipated that the standard test method will be released soon!

Q: Why are engineers interested in TLP and VF-TLP testing?

A: TLP testing provides the ability to understand semiconductor devices, circuits and chips response to high current pulse testing. One of the reasons TLP testing is popular is that it provides the actual current and voltage across the device under test (DUT). A pulsed TLP I-V characteristic is provided, which allows visualization of the semiconductor device response. A second reason is that testing can be completed “on wafer” or on product chips. With this capability, it can be used for semiconductor development, product design, to failure analysis.

Q: Are there both TLP and VF-TLP commercial test systems?

A: Today, there are both TLP and VF-TLP test systems that exist internationally. These TLP systems provide wafer level or product level testing.

Q: What is the difference between TLP and Very Fast TLP (VF-TLP)?

A: Very fast transmission line pulse (VF-TLP) is a new test method for faster rise times and shorter pulse widths. The VF-TLP test method requires a rise time less than 1 ns, and short pulse width between 1 and 10 ns. The TLP standard test method is a 100 ns pulse width. By combining TLP and VF-TLP methods, the power to failure of components can be quantified. Today, the VF-TLP Standard Practice (SP) document has been released from the ESD Association, and round robin testing is still in process to demonstrate this as a standard test method.

Q: Who is interested in VF-TLP testing, and why?

A: VF-TLP testing provides the current-to-failure and power-to-failure for fast rise-time events and short pulses. Today, this is relevant to quantify pulse events in the GHz time regime; hence, this can be used to quantify noise and pulse events on products, to test systems. With fast events there is also interest for radio frequency (RF) components. Technologists are also studying dielectric breakdown of ultra-thin oxide to quantify the response of fast, high-current events on dielectrics.

Q: What advantage is there to doing both TLP and VF-TLP testing?

A: First, TLP testing is "HBM-like" in its total energy for a 100 ns square pulse. Hence, TLP testing provides a sense for the anticipated HBM testing results. VF-TLP represents the response to fast pulse testing. By doing both TLP and VF-TLP testing, one will have the power-to-failure for both fast and slow phenomena. This is useful for development of a power-to-failure characteristic for the semiconductor device, circuit, chip or system.

Q: What is the next task of this standards work body?

A: In the future I believe we will be focusing on the transient response of the semiconductor device during the rising edge of the VF-TLP pulse. In this region, the device is not in a quasi-static regime, but a transient state leading to different I-V response.

Q: What else is ahead of us for future device testing?

A: Today, there is already research at Stanford University by T.W. Chen on ultra-fast transmission line pulse (UF-TLP) methods. These pulses help evaluate the dynamic response of materials when undergoing pulses in the range of 20 to 50 ps; this has value for understanding of the power to failure of components in the 40 to 50 GHz application regime. An UF-TLP test system has been utilized to understand soft- and hard breakdown of dielectrics, and is already being applied to the tunneling magneto-resistor heads (TMR) for the magnetic recording industry, (to be published in the EOS/ESD Symposium in 2008).

About the Author

This article was prepared on behalf of the ESD Association by Dr. Steven H. Voldman. Dr. Voldman is the first IEEE Fellow in the field of Electrostatic Discharge (ESD) in semiconductor devices for "Contributions in electrostatic discharge (ESD) protection in CMOS, Silicon on Insulator (SOI) and Silicon Germanium (SiGe) Technology." He received the ESD Association Outstanding Contribution Award in 2007. He has served as Chairman of the SEMATECH ESD

Committee from 1995 to 2000, ESD Association Board of Directors from 2000 to 2007, and Appointed Board Member 2007–2008. He has served as Technical Program Chair, Vice Chair and Chairman of the ESD Symposium from 2000 to 2002 and once again in 2008 and 2009. He is founder of the university lecture program known as "ESD on Campus," which provides ESD university lectures to over 27 campuses in the U.S.; and internationally, including China, Taiwan, Philippines, Singapore, Malaysia, and Thailand. Dr. Voldman is a member of the ESD Association Technology Roadmap Committee, and Chairman of the ESD Device Testing 5.5 Standards Committee on Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF-TLP) Testing from 2000 to 2008. Dr. Voldman is author of four books: *ESD: Physics and Devices*; *ESD: Circuits and Devices*; and *ESD: RF Technology and Circuits;* and a companion text, *Latchup*. He is presently independent and formed a limited liability corporation (Dr. Steven H. Voldman, LLC). Dr. Voldman has 170 U.S. patents, and 90 U.S. patent applications pending. Dr. Voldman has served as an expert witness in patent litigation cases. He can be reached at 802-769-8368 and at voldman@ieee.org

About the ESDA

Founded in 1982, the ESDA is a not-for-profit, professional organization directed by volunteers dedicated to furthering the technology and understanding of electrostatic discharge. The Association sponsors education programs, develops ESD standards, holds an annual technical symposium, and fosters the exchange of technical information among its members and others. **Additional information may be obtained by contacting the ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440-2069, USA. Phone: 315-339-6937. Fax: 315-339-6793. Email: info@esda.org. Website: www.esda.org**.