Statistical Sampling Comes to ESD Testing

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Is it necessary to test 100% of device pins to determine HBM sensitivity?

The Human Body Model (HBM) test has been used to evaluate the electrostatic discharge (ESD) sensitivity of new IC products since the early days of ESD testing. While there are a number of slightly different HBM standards used around the world, they all follow from the original MIL SPEC 883-3015.7 HBM standard developed in the 1980's. In order to conduct a full ESD test covering 100% of an IC's pin combination possibilities, the test would need to include all possible two-pin pair combinations. Even 25 years ago, when the IC packages were relatively small, it was recognized that the number of HBM pulses needed to conduct such a 100% coverage test could be unreasonably large.[1] Therefore, to provide good test coverage at reasonable testing times, HBM testing was defined as stressing each pin to every power and ground rail with a sample size of at least three ICs. HBM testing has continued to stress all pins[2] to power rails, resulting in considerable time savings over testing all possible combinations. However, with today's system-on-a-chip solutions with wide data buses and multi-chip modules having thousands of pins, test times of many hours are still required.

How can we provide a quantitative measure of ESD robustness but control the rising test times while preventing major overstress and wear out from thousands of ESD strikes per IC? One answer is to remove the redundant pin combinations to be stressed. For example, complex ICs are often organized around power supply groups, or power domains, and HBM now focuses on testing data pins (IOs) to their local power rails. This has been proven[3] to be adequate to provide full ESD assurance without unnecessarily overstressing the devices being tested. Recently the standards took a further step by defining proper pin sampling in a statistical manner. Since much of semiconductor reliability testing relies on sampling methods, this opening of sampling and statistical approaches for ESD testing is a significant and evolutionary step forward [1], [2].

The HBM Testing Goal can be met without 100% pin testing

HBM test results provide guidance to IC users as to the level of ESD stress that devices can be subjected to without damage, which allows users to institute proper transportation protection and safe handling methods during assembly. HBM is similar to reliability studies that use sampling such as Time Dependent Dielectric Breakdown and Electro-Migration measurements. If we want a good measure of ESD sensitivity and don't need to determine the exact worst case pin combination, why not sample pins for ESD testing? The JS-001-2014 joint HBM standard from the Electrostatic Discharge Association and JEDEC has introduced a method for the Sampling of IC Pins. This method first measures failure levels of a random selection of *identically designed pins,* then if analysis of their data shows they meet certain statistical requirements, sampling is allowed. This article explains the background of this statistical sampling and provides an overview of its use.

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[1] The number of pin pairs increases with the square of the number of package pins.

[2] The only exception to testing all pins has been skipping *unconnected pins* which is allowed in the widely used JEDEC and ESDA standards (see JS-001-2014).

[3] Data from multiple companies were reviewed by the JEDEC and ESDA Joint Working Group on HBM.

Sampling of Identical Pins

Sampling is only allowed on ICs and modules that have a large number of identically designed pins. ICs like gate arrays and ASICs have many IOs with identical cell layouts and the same ESD protection. They may have data and address busses with all the pins having the same macro name in the layout.[4] These pins are referred to as Clones, and some ICs may have several groups of clones. Using statistics, we treat a group of identical pins as a population and find their failure voltage mean μ and standard deviation σ. Then we apply common statistical methods to predict the HBM performance of this population.

The key statistical tool used is the Central Limit Theorem [3], which assures us that if given sufficiently large samples from a population, the mean of all samples from the population will be approximately equal to the true mean of the whole population. Accordingly, we can take a random sample of 30 pins and by stressing them with increasingly strong HBM current pulses until they fail, find the μ and σ of the sample, and use those measurements to predict the failures of population.[5] Specifically, we can calculate the probability that all the untested pins will pass a target HBM level. Being conservative engineers, we can set this probability at 99%. If our calculation determines we have less than 1% probability of being incorrect, we can safely sample the cloned IOs by testing only 30 of them. Knowing this, we can proceed to test by the usual HBM method but test only 30 of the clones in the full test. That is, all the clones are properly statistically represented by these 30 clones.

If we test the clone pins on an IC, we can find the individual failure voltage of each pin and plot the number of pins failing at each HBM voltage level. Then we can determine the range of failure voltages, which is a key parameter of the distribution of the clones. By entering the target spec limit (SPL), the highest voltage that all 30 sampled pins passed (V1), the lowest voltage that at least 15 pins failed (VM), and the number of clones (population size M) into a spreadsheet,[6] it is easy to determine the probability that all the untested pins will also pass the SPL. See Figure 1.

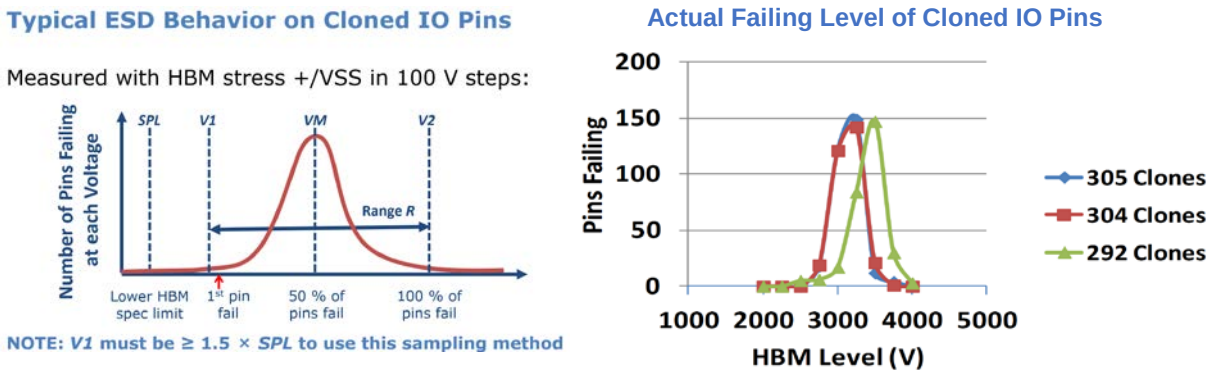

Figure 1: Distribution of HBM failure voltages for identical pins. Typical behavior is shown on the left side denoting the important parameters. Actual measured failure distributions from three different sets of clones are shown on the right side for three different products with cloned IO pins.

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[4] Verification of identical pins may require software rule checkers or design engineering data.

[5] The clone's failure points must be independent from each other, and for reasonable test time we need failures to be detectable from changes in DC curve traces.

[6] The spreadsheet 'ClonedIO-SamplingWorkbook.xlsx' can be downloaded from www.esda.org. This also contains a random number generator for selecting pins. Statistical methods are only valid if all sampling is done by selecting pins randomly.

If the probability of all the untested pins passing is greater than 99%, then using a *random sample of only 30 of the clones* (the rest being treated as "No Connect" pins) is justified. The group of clones can be treated as if it was a group of only 30 pins and use the normal HBM test method to test the clones along with all the other pins.

HBM Sampling can provide Confidence

With the introduction of sampling, we have added the concept of HBM testing to failure. This by itself is an important new measure of robustness. Traditional HBM testing does not find the typical failure voltage, but only determines if all tested pins can pass a target HBM voltage level or spec limit (SPL). Finding the "headroom," or safety margin of the HBM classification, is not required. Again, as conservative engineers we set a requirement for sampling that the clones must all pass 150% of the SPL, providing 50% headroom.

The statistical calculation we use finds the area under the left tail of the Normal Distribution (bell curve) of failure voltages and determines if it is so small that only 1% or less of the untested pins would be lower than the Spec limit. The larger the difference between the Spec limit and the sample mean, the lower the area in the tail below the Spec limit. It is interesting to note that the standard deviation is as important as the mean in the calculation of pin failures. The narrower the distribution (the smaller the standard deviation) the faster the lower tail drops. We can note that if the standard deviation is large, then even a distribution with a higher voltage mean may identify "out of spec failure" voltages in the left tail of the distribution. See Figure 2.

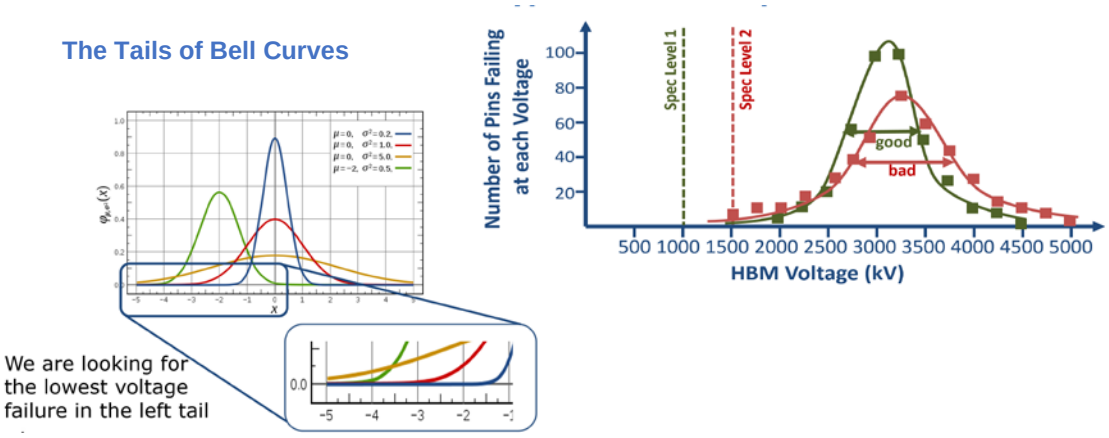

Figure 2: Theoretical shapes of Bell Curves. Actual measured data on two samples on the right-hand figure.

Production variations in devices like CMOS processors usually produce a normal distribution of failure voltages when testing clones. While there may be some production technologies that can skew the distribution, stepping the HBM stress until we measure the mean failure voltage allows us to carefully evaluate the lower failure voltages and provides assurance that our predictions will be valid even for non-normal distribution populations.

HBM sampling today and into the Future

Sampling statistics can now be used for HBM classifications provided sampling is only done on verifiable cloned IO pins. For more details on how to use sampling, refer to the ESDA on-line tutorial on the subject [4].

In summary, the method is as follows:

- Characterize 30 cloned pins chosen at random
- Step increase HBM stress voltages, recording failures until at least 15 have failed
- Perform statistical analysis, using a spreadsheet, on the 30-pin sample to ensure all unmeasured pins will be above the target SPL voltage with a confidence level of 99 %
- Test the parts as normal, but with only a 30-pin random sample of the clones

ESD testing of large ICs will become even more challenging in the future, but new test methods are currently being evaluated. We can expect future standards to allow sampling pins that are internally connected (almost identical), and eventually to also sample pins that aren't clones or identical by using valid random selection to produce repeatable and reliable HBM results.

As IC products increase in pin count, proper simplification to ESD test methods can be expected to achieve the following benefits:

- Shorter test times
- Reduced chance of random false failure testing errors
- Faster product qualification with equivalent test reliability

References

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[3] Grant and Leavenworth, Statistical Quality Control, McGraw Hill Series

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Author Biography

Evan Grund is the founder of Grund Technical Solutions (GTS), a Silicon Valley corporation specializing in ESD test equipment. Formerly, he managed engineering groups for semiconductor equipment companies including KLA-Tencor, Lam Research, and was a founder of Novellus Systems. He served as vice president of Oryx Instruments and site manager for Thermo Fisher Scientific, working on ESD testers for both companies. Evan and his GTS colleagues introduced 2-pin HBM automated testing.

Evan has over ten patents issued and pending patents on CDM and HBM testers. He has been a frequent presenter at ESD forums, workshops and symposia. Evan is a lifetime member of EOS/ESD Association (ESDA) and is active in their standards working groups. Evan taught college level electronics and programming and is an ESDA instructor for TLP. He holds a BS EECS from UC Berkeley and MSEE from Stanford.