The Industry Council on ESD Target levels

Making an Indelible Impact on ESD from Components to Systems

The Industry Council on ESD Target Levels, since its inception in 2006, has strongly influenced the IC industry's ESD qualification processes. The industry's original ESD qualification requirements were established some 35 years ago, and their relevance has progressively diminished due to a number of changing factors. These include, on the one hand, the much-improved factory control methods and, on the other hand, the ever increasing demand for higher performance circuits with a low tolerance of loading capacitance from ESD networks. Taking into account these factors, the ***Industry Council***, as it is now commonly known, has established interim safe and practical ESD levels that are not only necessary but are imperative for the progression of advanced semiconductor technologies. Another important factor is System Level ESD, which is an area that the Council is bringing into significant new focus. The Council membership has recently expanded to more than 50 different corporations, including IC Suppliers, OEMs, ESD Factory Control Experts, and Consultants (see Fig. 1).

Fig 1: Industry Council Membership. As the work of the ESD Council progresses, more OEMs have been joining the Council.

Changes to ESD Qualification Levels

Based on the vast experience of leading experts from the fields of IC manufacturing, ESD factory control, system design, and ESD consultancy, a strong impact on the way the industry assesses ESD target levels has been made. The success of the Council in establishing ***a new order for ESD qualification*** depended on systematic collection of data involving several corporations that have been willing to share billions of units worth of data. This unprecedented approach is unique in the industry and represents the wave of the future in dealing with the competing demands of technology performance and reliability requirements. Convincing the industry as a whole requires acceptance from the standards bodies such as JEDEC and ESDA. Working closely with these organizations, the Council has documented the basis for changes in component ESD levels through two published white papers [1, 2]. As clearly established from the two white papers on HBM and CDM, **the recommended safe levels are 1kV for HBM and 250V for CDM.** These levels only require **basic mandatory ESD control programs** and still provide significant margin above critical levels that would warrant advanced control programs (<500V HBM, <125V CDM).

As an additional key point of interest, **the Machine Model (MM) has been determined to be obsolete** [1, 3]. This is well documented and the standards organizations such as JEDEC and ESDA now recommend against using MM as part of the IC ESD qualification process. MM is redundant to HBM, and the factory discharge events of metal-to-metal contact are adequately covered by CDM [3].

More recently, high-speed circuit designs that are implemented in high pin count packages are in the process of driving CDM to a lower level of 125V. Improved ESD control programs globally, with detailed methods such as ESDA S20.20 or JEDEC 625B, could enable this path.

HBM Level of IC	Impact on Manufacturing Environment
2 KV	
1 kV	Basic ESD Control methods allow safe manufacturing with proven margin
500 V	
100 V to <500 V	Detailed ESD Control methods are required

Table 1: The new accepted understanding of the impact on manufacturing corresponding to a component IC's HBM level.

In Table 1:

> Basic ESD Control programs include wrist straps, grounded work surfaces, and safe packaging materials, and they are safe with proven margin to 500V HBM [1].

Detailed ESD Control refers to ANSI/ESD S20.20 [4] or IEC-61340-5-1[5] or JESD625B [6]. S20.20 and IEC programs are comprehensive program standards patterned on ISO9000 and can provide the basis for facility certification. JESD625B [6] is a widely used standard in the IC industry.

Implementation of these standards provides protection of devices to at least HBM ≥100 volts, and probably lower.

CDM classification level (tested acc. to JEDEC)	ESD control requirements
$V_{CDM} \geq 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators
$125V \leq V_{CDM} < 250V$ **Additional Controls Required**	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads).
$V_{CDM} < 125V$ **Advanced Controls Required**	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **AND** to avoid a hard discharge (high resistive material in contact with the device leads) + • **Charging/discharging measurements at each process step.**

Table 2: The CDM target levels and the corresponding control requirements are shown. Additional controls are necessary for CDM levels below 250V.

As shown in Table 2, general CDM control programs are necessary [2]. These include both Basic ESD controls and CDM-specific controls. These general CDM steps are basic in nature and are always important, regardless of the HBM performance of a device. Combining the requirements of Table 1 and Table 2 with only general ESD

controls in place, ESD levels ≥ 500V HBM and ≥ 250V CDM are safe. Also, for CDM, Advanced or Detailed Programs should comply with S20.20 or IEC 61340-5-1 and the CDM elements of JESD625. These require regular compliance verification. With the advent of advanced technology IC devices, the majority of the industry is progressing toward these detailed process control steps. Overall, effective implementation of these advanced programs is intended to provide protection for devices with ≥ 100V HBM and ≥ 100V CDM.

Impact on Customers and Time-to-Market

The most important aspect of ESD control is that, as long as realistic requirements for manufacturing and field reliability are instituted the Council has shown that ***a win-win situation*** is always possible for both the customer and the supplier of semiconductor devices. As shown in Fig.2, the benefit to both customers and suppliers becomes more prominent as technologies advance further and the IC chip designs become more complicated.

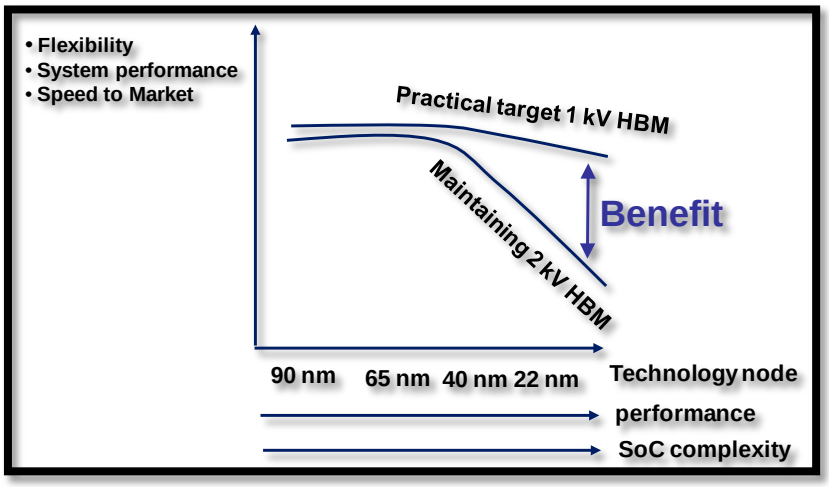

Fig. 2: Changing from 2kV HBM target to the more-than-safe 1kV HBM facilitates the important advantage of meeting high-speed requirements. It has benefits to both the OEM and the IC supplier of enabling delivery of high performance products with advanced technologies on time.

The same benefits shown in Fig. 2 become even more significant when changing from 500V CDM to 250V CDM. The Council has established, based on a vast amount of data, that 250V CDM is a safe level with basic ESD control programs. This new level is becoming well accepted, driven by high speed IOs in large high pin count ICs.

With the technology roadmap in perspective [7], the goals of 100V-HBM and 100V-CDM are not too far in the future. For this reason, implementing the above-mentioned detailed ESD control programs paves a critical path for IC manufacturers.

Realities of System Level ESD Protection

The Council realized that system reliability has much more far-reaching effects than component reliability. After launching the second phase of system level ESD robustness studies, the Council generated two additional white papers on the subject [8, 9]. This required engaging a new set of world experts, including automotive system experts. The first objective of these white papers was to eliminate the prevailing confusion in the industry about system level ESD and the misunderstanding that often results between the OEM and the supplier. The second objective was to clarify what is important for system ESD and to introduce a new concept called ***System-Efficient-ESD-Design (SEED)***. The SEED concept is illustrated in Fig. 3. The Council now aims to spread the implementation of SEED through the standardization of characterization and modelling of PCB discrete and IC components and a simulation-tool-based optimization approach of the board design. This will affect a wide field of the electronics industry, ranging from discrete and IC suppliers, to EDA tool vendors, to system designers. As a result, SEED will enable new and more efficient system level ESD protection designs. The Council is currently extending SEED to address soft failures. System ESD can impact an entire system and can create both “hard” and “soft” failures. So-called soft failures may involve complex EMC/EMI effects and also some Transient Latchup (TLU) phenomena. See Fig. 4 for an example. For these reasons, a proper off-chip system level protection strategy is much more effective and reliable than an on-chip system level protection.

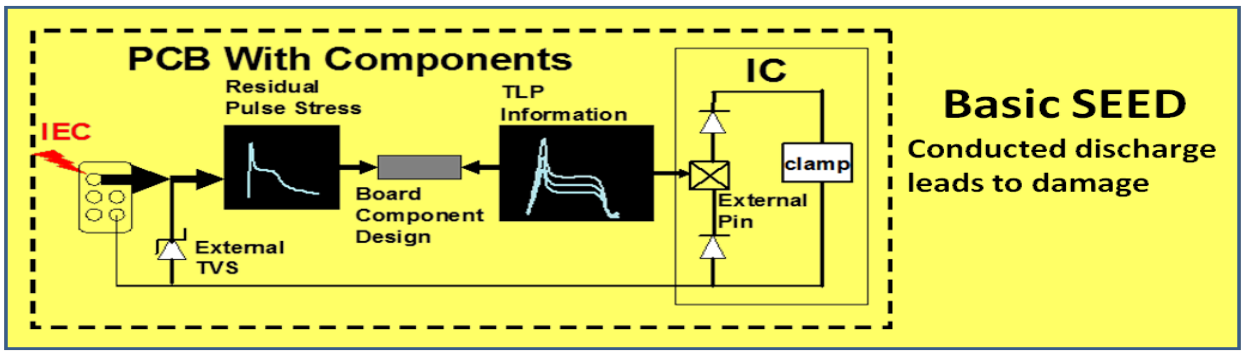

Fig. 3: The new accepted understanding of the impact on manufacturing corresponding to the component IC's HBM level. The residual pulse after external clamp is matched with the TLP information of the interface IC pin for different time domains. The board components are tuned for robust IEC protection.

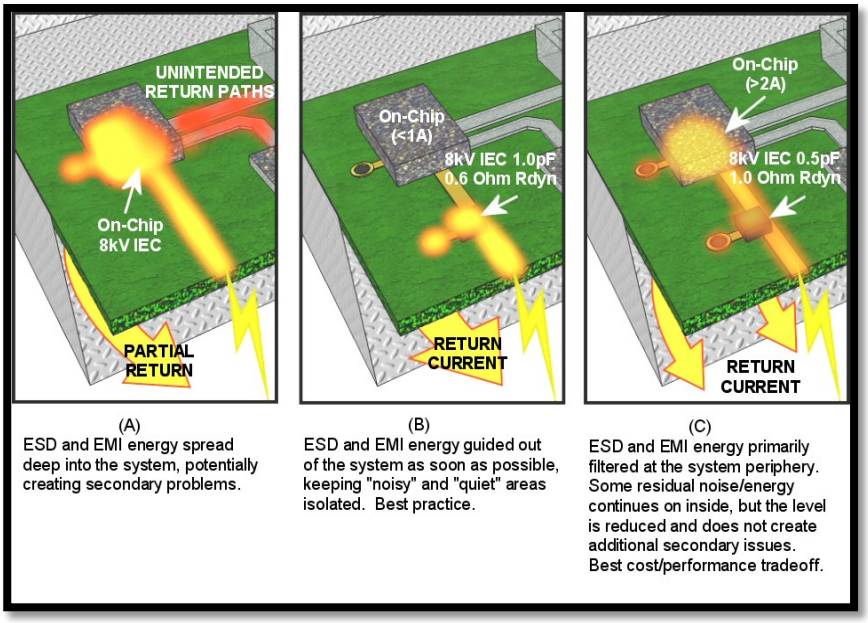

Fig. 4: Discharge paths through a wired network showing the different strategies. On-chip protection for system level ESD does not yield optimum results.

Efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level. An appropriate characterization of the components is necessary. This requires a methodology to assess the whole system using characterization data, such as by simulation. This is done with system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)).This approach relies on improved communication between the IC supplier, the supplier of discrete PCB protection components, and the system builder. SEED is promoted by leading IC suppliers and OEMs to become the prevailing standard for system level ESD design. In parallel, new initiatives have been started to standardize details of data format for SEED models [10].

Electrical Overstress (EOS): The Perennial IC Damage Phenomenon

Finally, the Council has most recently embarked on the topic of IC and system failures from electrical overstress (EOS). Although EOS has been a constant bane of field and application failures, not much attention has been paid in the industry to address these issues with any sense of urgency. This has been mostly due to the complexity of these failures, which can arise from a myriad of root causes at every level from field testing to customer applications. Without in-depth studies of these phenomena, a clear direction to solve ***EOS as a massive and persistent problem*** cannot be determined. The Council has now initiated these studies through extensive data collection from all across

the industry. It is expected that this process will need to continue into early 2014. Publication of a white paper is targeted for the second half of 2014. The most important goal of this white paper is to provide a ***definitive guide to minimize unnecessary EOS failures*** in the semiconductor industry.

In conclusion, what started as a consortium of a few IC suppliers trying to identify practical means of addressing the pervasive ESD component qualification difficulties, has now evolved into a fully recognized organization that can help the industry progress by addressing the **semiconductor electronics technology roadmap in parallel with the necessary but realistic ESD roadmap**.

Anyone wishing to participate and contribute to the Council's activities or take part in the EOS Survey is invited to contact the chairmen (harald.gossner@industrycouncil.org / cduvvury@industrycouncil.org).

Many of the documents from the Council are available on the web site: http://www.esdindustrycouncil.org. References [1, 2] below are also available in Japanese on the Council web site.

Acknowledgments:

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References

[1] White Paper 1, "A Case for Lowering Component Level HBM / MM ESD Specifications and Requirements". www.esda.org/documents/WhitePaper1_HBM_MM_2010.pd, also known as JEP155.

[2] White Paper 2, "A Case for Lowering Component Level CDM ESD Specifications and Requirements". www.esda.org/documents/IndustryCouncilWhitePaper2.pdf, also known as JEP157.

[3] "Discontinuing Use of the Machine Model for Device ESD Qualification", IN COMPLIANCE Magazine, July 2012, pp. 57-63.

[4] ANSI/ESD S20.20

[5] IEC-61340-5-1

[6] JESD JEP125B

[7] www.esda.org/documents/2013ElectrostaticDischargeRoadmap.pdf[8] White Paper 3 Part I, "System Level ESD: Common Misconceptions and Recommended Basic Approaches," www.esda.org/documents/IndustryCouncilWhitePaper3.pdf, also known as JEP161.

[9] White Paper 3 Part II, "Implementation of Effective Robust Designs," www.esda.org/documents/IndustryCouncilWhitePaper3_PII.pdf, also known as JEP162.

[10]. ESDA's New Working Group on System Level ESD