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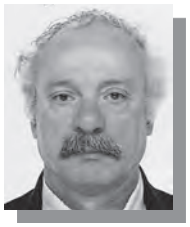

Simon Deleonibus

We look back at 50 years of microelectronics initiated through the famous prediction by EDS Celebrated Member Gordon Moore in 1965. Since 1992, semiconductor manufacturers, equipment suppliers, research institutes and peripheral stake holders have been sitting at the table to make concerted actions towards what is needed to fulfill the technological requirements ahead, with the semiconductor roadmaps as the result. Microelectronic engineering became predictable and was less based on surprising discoveries, as in the pioneering years prior to Moore's Law. However, throughout the Moore's Law era there were still unexpected discoveries, underestimated applications and underrated impacts of electronic materials, process technologies, device structures, techniques and semiconductor technologies, which helped advancing microelectronics in a remarkable way. Coincidentally, the techniques that microelectronic engineers and scientists developed inspired their colleagues in other fields to miniaturize functions that were not expected to come into play one day and co-integrate them with CMOS. For example, the so called pervasion of microelectronic techniques and progress in scaling is now widely recognized and adopted in the photonics or mechanics worlds. A first roadmap was issued by ENIAC in Europe (2002) to define Heterogeneous Integration,

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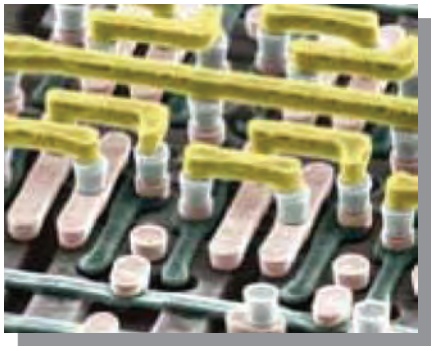
Marvels of Microelectronic Engineering

(continued from page 1)

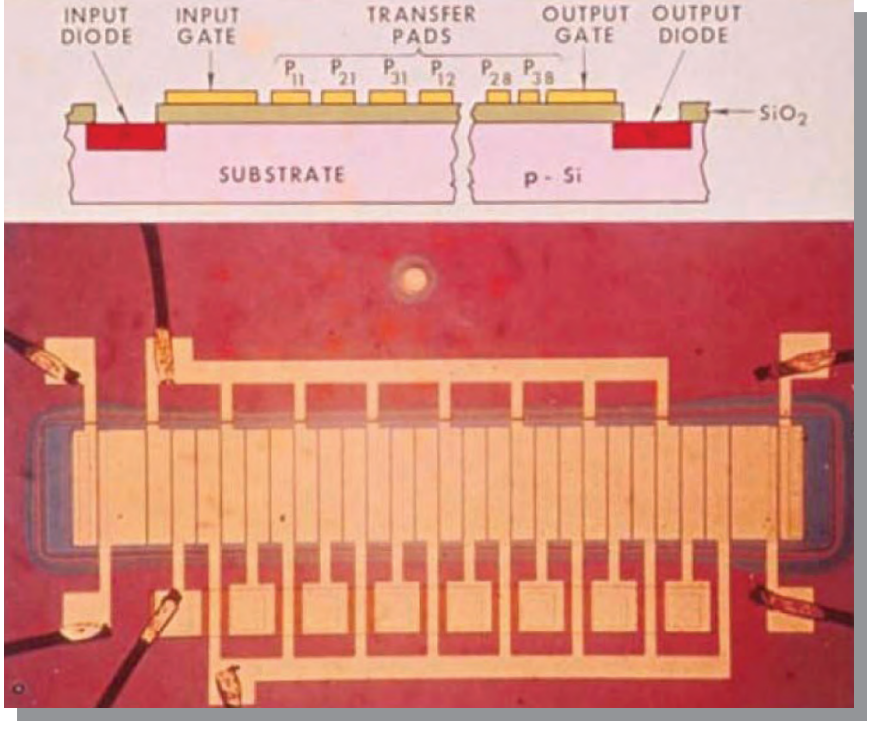
the so-called More-than-Moore domain, besides the More-Moore and Beyond-CMOS devices: these denominations appeared in the ITRS in 2005. As much as we admire the coordinated engineering along the roadmap we should also highly appreciate those Marvels of Microelectronic Engineering. We have tried to identify such marvels and will present and discuss some of them in this and the next five editions of the EDS Newsletter. Certainly, there could be an endless discussion about the definition of a marvel of microelectronic engineering and about the selection *versus* omittance of candidates. Therefore, we have seemed advice from electron device pioneers, from our EDS colleagues and went into thorough literature search. As stated, the selection that will be presented in the six editions of the EDS Newsletter will not be comprehensive though exemplary. The intent of this series of articles is not only to highlight and celebrate those marvels but to show particularly to the younger EDS members how engineering 'with an open eye' can lead to spectacular discoveries with a high and lasting impact.

Let's take a look at some prominent examples to better understand the definition categories of Marvels of Microelectronic Engineering. The senior EDS members will certainly remember that metal interconnects in the 70's were based on aluminum not on copper as today. Aluminum, in fact, is even easier to handle than copper, since it can be dry-etched to shape interconnect lines and is less of a headache than copper which might act as a mid-bandgap trap in silicon and, thus, would dramatically increase leakage currents at device junctions unless precautions, such as diffusions barriers, are employed. However, right after Bob Noyce at Fairchild proposed the planar wafer integration process in 1959, it became obvious that such narrow and thin metal lines would be prone to electromigration, an electrochemical material transport that would lead to an interruption of powered metal lines. This was a particularly nasty problem because it could show up on the customer's side when using the chip. The solution to this problem is an exemplary case of a coincidental discovery with an enormous impact. Without this Marvel Moore's Law might not even have taken off the ground.

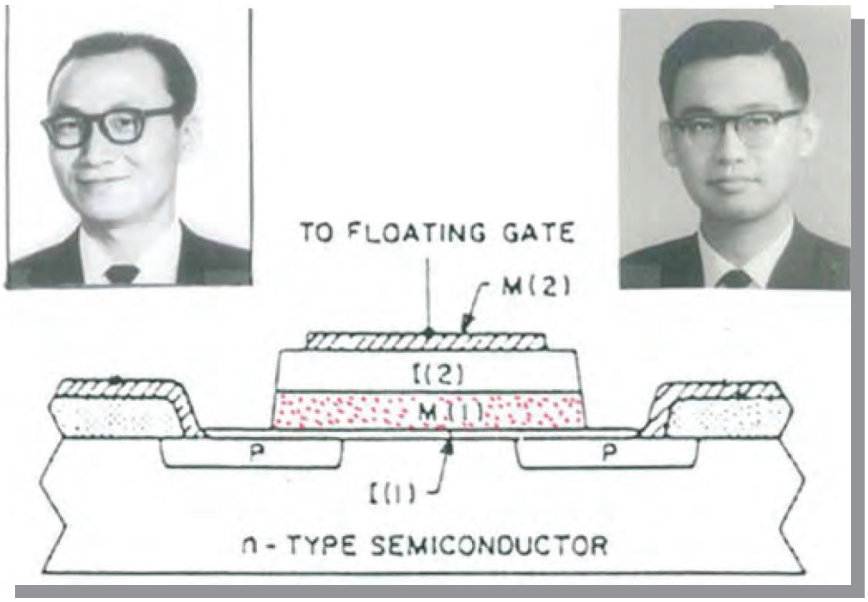
It was in the late 1960's that IBM researcher Francois d'Heurle was asked to look into this bottleneck issue. In his lab he did experiments with several kinds of metals which he deposited in his electron-beam evaporation system. The aluminum lines that were formed out of his 'aluminum' turned out to be far more resistant to electromigration than the Al interconnects of the product technology at that time. Even though this was good news, nobody could make sense of it until Francois found out that the electron-beam also hit the cold copper crucible next to the aluminum. It was then a logical step to intentionally incorporate a small fraction of Cu into Al, thus introducing the AlCu interconnects that are still used today for certain products. This was even the foundation of the Cu interconnects which became inevitable



90 nm VLSI interconnects (Source TSMC) Reproduced by permission of IBM



The first CCD prototype by George Smith and colleagues at Bell Labs in 1970 (Reprinted with permission from George E. Smith, "The Invention and early history of the CCD," J. of Applied Physics, May 31, 2011. Copyright 2011)



First floating-gate memory (FGM) by Dawon Khang (left) and Simon Sze (right). (Courtesy of Simon Sze)

as AlCu hit the electromigration limit in the 1980's. Francois d'Heurle filed a patent on his Marvel in 1969 and received the IEEE Cledo Brunetti Award in 1988 for this breakthrough discovery by him and his colleagues. This was emblematically the beginning of the "contamination aware" era in microelectronics: electrical engineers needed to watch at the purity and possible doping/alloying of the materials or chemicals they were using to obtain good yields and ensure reliability. Microelectronics was no more an electronic engineers business but became a cross disciplinary research field between electronic, materials and device scientists.

Another class of Marvel relates to the charge-coupled device (CCD) invented in 1969 at Bell Labs by Nobel laureates William Boyle and George Smith who is an EDS Celebrated Member. The CCD was first intended as a shift register since the focus of the group was on bubble memory. Just one year after its invention Smith and his colleagues could show that the CCD could as well be used as an electronic imaging device. The EDS web site reports: 'The device they initially sketched was an image sensor based on Einstein's photoelectric effect, in which arrays of photocells emit electrons in amounts proportional to the intensity of incoming light. The electron content of each photocell could then be read out, transforming an optical image into a digital one. The charge-coupled device they created gave rise to the first CCD-based video cameras, which appeared in the early 1970s. "It took about an hour and half to design the CCD," joked George, "but it took 40 years for us to get the Nobel."' The CCD clearly is a case of an underestimated application, first intended and engineered for a particular purpose but then carried over to an entirely unexpected application. Even though CMOS active pixel sensors have a considerable market share of electronic imagers, even today, after more than 40 years the CCD imager concept drives an ever growing industry.

The third class of Marvels relates to the underrated impact of a discovery which may even have been considered useless, as EDS Celebrated Member Simon Sze quoted his former boss at Bell Labs. Simon Sze and Dawon Kahng came up with the concept and first experimental results of a floating-gate MOS device in April 1967. They called it Floating-Gate Memory (FGM) and wanted to publish it in the IEEE Transactions on Electron Devices but only got permission for a paper in the Bell System Technical Journal where it appeared in July 1967. Their FGM device had a second metal gate for the charge storage. Coincidentally, other teams were exercising their curiosity on the capability to store charges inside the gate insulator of the first p channel IGFETs (Insulated Gate Field Effect Transistor). Following a preliminary idea of Szedon at 1967 DRC on alterable MNOS structures, H.A.R. Wegener from Sperry Rand Research Center published a similar structure at IEDM 1967, in which charges were stored in silicon nitride layer traps by injection through the underlying tunnel native oxide, resulting in a memory device with low charge retention capabilities (a few months at room temperature), due to the leakage with the gate or channel. During the same exploratory period, the use of an extra oxide layer on top of silicon nitride was proposed to implement MONOS structures (Keshavan and Lin from Westinghouse at IEDM 1968, and Keshavan's patent 1968), introducing one more degree of freedom to bandgap engineering and applied voltages to write or erase the memory element. Programming (erasing) voltages were in the range of –40 to –50 V (+ 40 to +50 V). Still data retention, endurance and scalability of these devices were major issues. In 1977, almost 10 years later, P.C.Y. Chen published a n+ polysilicon gate SONOS device which partially solved the retention time issue of Szeldon-Wegener's MNOS by oxidizing the nitride layer at high temperature and relaxing the channel tunnel oxide thickness from 15 to 30 Angstroms, reducing the programming voltages to about 20 V, reducing at the same time, but not suppressing, the gap of co-integration with low voltage logic MOSFETs. A huge zoo of possible candidates inhabited the literature. Even though Chen opened a new opportunity,

scaling these devices inside a memory array was a major hurdle because the tunnel oxide thickness was already at its limits and endurance (write/erase cycles) would not be meeting large public applications requirements. At that time, the usage was limited to code and not applicable for massive data files storage. UV erasable and hot electron programmable EPROMs had by far the highest density, using the floating gate to store charge and the ONO layer as a coupling capacitor between the control gate and channel. Whether one-time programmable or multiple times programmable devices would be needed depended much on the application. Fujio Masuoka and his team at Toshiba faced the challenge to make collective erasing of memory sectors by a common erase gate while keeping a NOR type structure for individual cell programming. They named the new architecture Flash EEPROM (1984). Further on, a serial arrangement of bit cells into a NAND type structure was proposed (1987) by the same team. The quest for a solid state disk based on transistors was possible by using a NAND Flash scheme, thus reaching more than several 10^6 write/erase cycles, 10 years retention times and high density (less than 5F2 transistor feature size in an array string) were mandatory. The compromise between reliability and speed would depend on the physical process used for write and erasing. Fowler-Nordheim injection was suited for high capacity NAND Flash (preferably Stand Alone) while low capacity NOR type would still be bearing hot electron programming (preferably Embedded). Under these particularly stressful conditions, combining the difficulties to use high write/erase voltages and increasing the memory density posed very particular problems in scaling and ensuring device reliability.

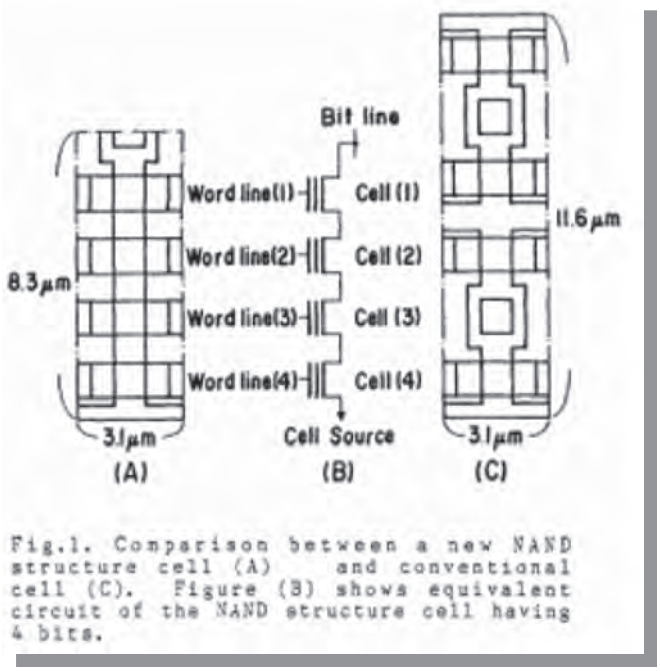
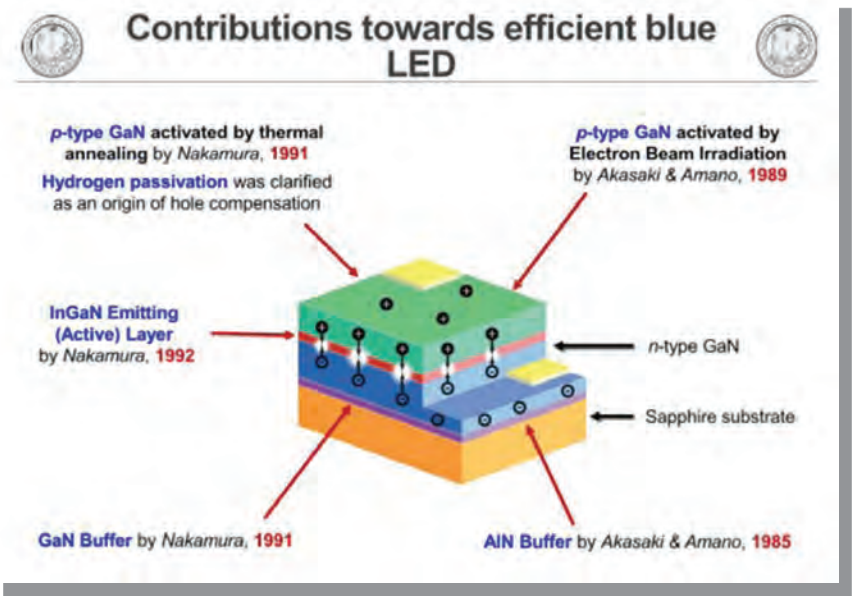


Fig.1. Comparison between a new NAND structure cell (A) and conventional cell (C). Figure (B) shows equivalent circuit of the NAND structure cell having 4 bits.

First paper on NAND Flash Memory by Masuoka et al. IEDM 1987

Many companies worldwide (Toshiba, Samsung, Hynix, STMicroelectronics, Macronix, Micron, Hitachi, Matsushita,...) have carried out huge struggles in the 1990's and 2000's to scale down the ONO stack and the tunnel gate oxide, make sure that short channel devices electrostatic integrity and low parasitics between adjacent cells were kept. A major limitation to the tunnel oxide scaling came from stress induced leakage current (SILC), leading to retention and endurance degradation. This limit reintroduced the interest in barrier engineering based on a revised SONOS concept discrete trap storage. Actually, a TANOS (TaN/Al2O3/Si3N4/SiO2) with a p+ control gate, Macronix 2005) was used to obtain good data retention. Increasing capacity without dimensional scaling was necessary because of the tunnel oxide scaling limitation. 3D integration (Toshiba BICS 2007) was proposed and could include multilevel programming as well.

Group photo at the celebration of Prof. Simon Sze's (mid-front) election to EDS Celebrated Member during IEDM 2017



Blue LED history in Nakamura's Nobel lecture (2014) (Courtesy of S.Nakamura)

Today's flash-memory transistors are close to Kahng's and Sze's FGM device with the differences at the levels of physical structure and operation modes. The operation mode of NAND Flash memory is counter intuitive as compared to the initial FGM, because of its collective program/erase operation and serial reading mode, just as in a CCD. Trying to sort out if the credit for the most significant and pioneering contribution to flash memory would go to Kahng/Sze, Wegener, Szedon, Keshavan/Lin,Chen and Masuoka seems not worth discussing. Without the early work of Kahng/Sze and Wegener in 1967, Szedon in 1967, and Keshavan/Lin in 1968, the concept of charge-storage memory may have been considered much later and not in time for conquering its present significance. Without the work of Chen in 1977 and Masuoka in the 1980s that concept may not have made it into practical use and EEPROM may not have taken off the ground or at least much later. Without EEPROM and its short comings when scaling down and operating the device Masuoka's flash memory may not be there where it is today. The story of flash memory is, thus, not based on a solitary marvel but rather a marvelous chain of discoveries and outstanding engineering efforts in the course of almost 20 years.

As we already mentioned, the phenomenon of seeking grails is not limited to microelectronics. In the area of photonics, the invention of the blue LED is also emblematic whereas it made white lighting possible and up-scalable. The realization of the first room temperature blue emitting InGaN (Nakamura 1992) was a determinant step to further complete the set of red and green LEDs that would make white lighting possible. Initially, EDS Celebrated Member Herbert Kroemer introduced in 1963 the double heterostructure (DH) based on high-bandgap/low-bandgap materials to realize high efficiency lasers and LEDs. There were many hurdles to be overcome for realizing cheap and reliable, highly performant GaN/InGaN (DH). First, the GaN epitaxial growth by MOCVD on a sapphire requested high crystalline quality (Akasaki and Amano 1985), and uniformity (Nakamura, Two flow mode MOCVD 1991). A final interstitial H+ de-passivation of holes was necessary to obtain highly conductive p+Mg doped GaN anode (Nakamura 1992, Akasaki and Amano 1989).

Finally, a demonstration of a bright Blue InGaN/GaN DH emitting 1 candela was obtained in 1994 (Nakamura). The Indium content allowed tuning the LED color emission from yellow to blue. Commercialization by Nichia Corp. of white lighting devices based on InGaN/GaN LED DHs began in 1996. White lighting based on LEDs is massively used today and has revolutionized lighting thanks to its efficiency and device lifetime: 40% of world electricity consumption would be saved by 2030. The inventions brought by Nakamura, Akasaki and Amano thanks to their flexible up and down scalability, make accessible new lighting modes for mobile phones and large area home displays, automotive, agriculture, healthcare, etc…with the possibility to invent new lighting devices and shapes. The innovation in white lighting by LED represents a major benchmark event of the end of the 20th century history.

The coincidental discovery of AlCu interconnects, the alternate application of the CCD as a solid-state imager, the unforeseen emergence of the flash memory and the invention of blue LEDs are just four examples of Marvels of Microelectronic Engineering. We will search through candidate topics in electronic materials, process technologies, device structures, techniques and semiconductor technologies and try to identify the marvels in those areas as well as their impact on the field.

The following articles are planned:

- October 2018—Electronic Materials—Editor: Simon Deleonibus
- January 2019—Process Technology—Editor: Joachim Burghartz
- April 2019—Device Structures—Editor: Simon Deleonibus
- July 2019—Concepts & Techniques: Editor: Joachim Burghartz
- October 2019—Technologies—Editor: Simon Deleonibus

The Many Aspects of Robustness for IoT Devices

Harald Gossner, Intel
Charvaka Duvvury, ESD Consulting LLC

Abstract. The introduction of Internet of Things (IoT) are creating many new challenges. These include critical driving factors such as high integration as well as economical scaling of high volume devices to enable highest performance at lowest cost rates possible. To bring into focus these upcoming issues, this article would address the following topics: 1) understanding of adequate base robustness of semiconductor devices considering technical and economic aspects, 2) appropriate methods to meet overall module robustness based on robustness of ICs in module design, and 3) challenges for test standards to be applied on IC and module level to verify the robustness target for IoT devices.

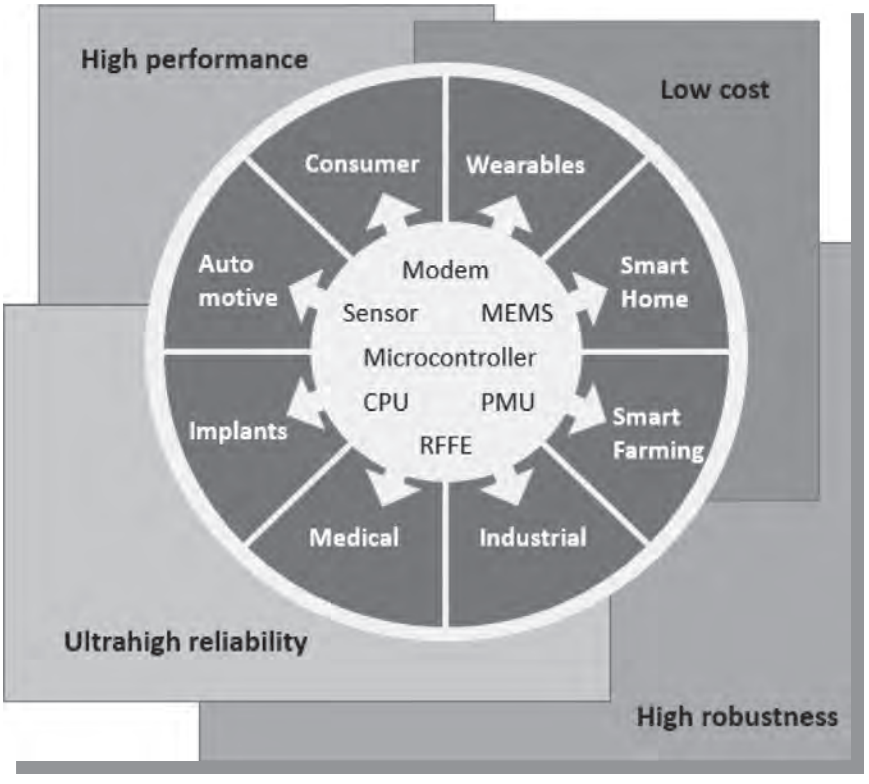


Fig.1. Scaling of semiconductor components into IoT markets with diverging robustness, cost and performance requirements

Introduction

Today's electronic industry is challenged by the need of ubiquitous Internet of Things penetrating into all realms of society, business and personal life. The basic functional building blocks of IoT devices are sensing, computing and connecting. There is a plethora of IC solutions for each of these features available and their performance is continuously growing. This adds up to an enormous number of devices and market opportunities, e.g., a recent report anticipates a market of $56B for low power wide area IoT devices in 2022 [1]. It is also expected that the $1 trillion spending mark of IoT total market would already be surpassed in 2020 [2].

IoT Integration

The driving factors for new applications are flexible integration of multiple functions like sensors, microcontrollers or wireless modem devices and the use of highest performance ICs, but at low cost due to the economical scaling effect of high volume products. To fully exploit this for IoT applications, a single IC solution should be scaled into many applications ranging, for example, from industrial to consumer. However, there is a limitation; IoT modules need to comply with very different reliability and robustness requirements depending on the application and the environment (Figure 1). A comparison for typical reliability and robustness requirements is shown in Table 1.

Reliability Considerations

Since the reusing of IC hardware for diverse applications in the fragmented IoT market is a critical factor for market success, adequate design solutions and development strategies for robustness as well as testing and qualification standards are crucial. The design adaption of a superset of robustness requirements is not a viable solution for cost driven applications. For example, compromising of the silicon area or even performance needs of a high volume mobile phone component to enable the use of the same design for a low volume, ultra-high reliability application, is typically unacceptable. Another approach for high reliability parts is to apply burn-in stressing and comprehensive and tight testing of the components to screen weak parts for reducing early fail rate or selecting components within the distribution of a semiconductor manufacturing process which are compliant with a longer lifetime. Obviously, this comes at the cost of

Table 1. Comparison of typical robustness requirements for different market segments.		
Robustness parameter	**Consumer**	**Automotive**
Zero hour DPM rate	Several 100 dpm	Several ten dpm
In-field quality	Several 100 dpm/y	Single digit dpm/y
Product Life time	5…10 y @T_{amb} = 85 °C	15 y @T_{amb}> 105 °C
Thermal/Mechanical Stress	Specified by JEDEC	Specified by AEC
Dynamic Stress	Specified by JEDEC	Specified by AEC
ESD Qualification Targets	1 kV HBM, 250 V CDM	2 kV HBM, 500 V CDM

Table 2. Parameters for robustness of semiconductors.	
Parameter	**Impact on**
Junction temperature	Life time of circuitry
Max operational voltage	Life time of circuitry
Max operational current	Life time of circuitry
Absolute maximum ratings for voltage and current	Electrical overstress of circuitry
Temperature cycles	Ball or die cracks
Humidity conditions	Corrosion

a reduced yield. Even more important, an appropriate system design can largely mitigate the need for enhanced IC robustness requirements. In many IoT systems the semiconductor components are assembled in an IoT module before they are integrated in the final system. Thus, the module and system design can enable the use of IC components with lower reliability targets in an ultrahigh reliability application. One example of how to implement this is shown by avionics industry which needs to rely on consumer IC parts due to the very low volume of components, with the intention to ensure highest robustness and safety on the system level. Some of the methods applied in these cases belong to the field of safety design. These are examples of redundancy of modules or complete systems, and watchdogs controlling the function of microcontrollers working in parallel. Whilst these are often very costly measures, other critical IoT applications also can benefit from the concept of design for safety following ISO 26262 to handle risks and malfunctions [3].

A more comprehensive assessment of a safe system operation has to include even more factors like availability, reliability and maintainability, which are commonly summarized as dependability [4]. All these system requirements are related to a larger or lesser degree to the robustness performance of IC, module and system.

IoT Qualification

At this point a more concrete definition of the term 'robustness' has to be given. The focus of the current discussion is on hardware related, electrical robustness. This refers to a safe operation with well specified failure rates over lifetime under given environmental and operational conditions including a robustness margin covering excursions in the system operation and ambient stress. Examples of ambient stress and an excursion are electrostatic discharges (ESD) and a supply overvoltage created by a defective charger. However, it has to be understood that for any semiconductor component as well as for any electronic system the margin needs to be specified. As an example, for semiconductors this is covered by the Absolute Maximum Ratings (AMR) in the data sheet as recently discussed in detail through a white paper by Industry Council on ESD Target Levels and endorsed by JEDEC [5]. A list of the most relevant operational and environmental parameters for robustness of semiconductors are shown in Table 2. The challenge arises that in many real-world situations various combinations of environmental and operational conditions appear and it is not clear how the robustness can be described by a simple set of parameters. For example, ICs with high ESD performance can easily fail under low dc stress leading to electrical overstress (EOS) and vice versa [5]. This has led to a creation of a complex landscape of use-specific qualification tests to ensure the robustness in the specific field of application. On the IC side, there are qualification procedures defined for most consumer products by JEDEC, while automotive industry refers to AEC Q100 and industry specific add-ons. Even more confusing is the qualification landscape for systems. Examples are CISPR-35 for electrical immunity of consumer products, DO-160 for avionic systems, IEC60601 for medical systems and AEC standards for automotive. Many of the higher level system standards also refer to various tests of ISO and IEC, and specify use-specific targets. Semiconductor components designed for these markets take this into account and have developed specific design measures and tests over time.

Characterization of IoT Systems

Now moving into the world of IoT with the need of more flexibility in use of IC while serving the constraints of the various system applications, robustness design and characterization has to be revisited.

A first step in this direction has be done in the field of system ESD design [6]. For many years the request to IC suppliers has been to provide high HBM robustness for ICs assuming it

is required to support the system ESD robustness according to IEC 61000-4-2. But recently it was clearly shown by an industry group consisting of IC manufacturers and system OEMs that this is a miscorrelation and needs to be corrected [6]. In consequence, a more appropriate method was proposed called system efficient ESD design (SEED) [7]. A characterization of the IO pin of the IC and the printed circuit board (PCB) discrete components for high transient currents has been defined which allows to match the system design to the behavior of the IC and achieve the system ESD level needed for the specific application. Similar approaches are used for signal integrity and power integrity design. Moving away from preset levels and go-no/go results of an IC qualification to a more insightful characterization of the IC behavior could be a role model for many robustness requirements in the IoT field. This actually goes beyond the previously discussed concept of a robustness validation by testing to fail [8]. This only allows to qualitatively detect trends and give an early warning to system design, but it does not allow to design a targeted system robustness level based on the IC data.

The technical challenge is to find appropriate characterization methods for the wider field of robustness requirements of IoT semiconductor components. This includes diverse components like processors, RF components, sensors and actuators. To pave the way to a cross-industry approach for characterization of robustness of components for IoT applications several questions have to be answered:

- What are the adequate characterization methods and the respective levels of 'base robustness' of semiconductor devices considering technical and economic aspects?
- What are the appropriate methods to design a module and system using the robustness characterization of ICs?
- What are the IoT test standards to be applied on IC and module level to verify the robustness targets?

Finally, it should not be forgotten that besides the importance of robustness at end-customer operation, the aspect of safe manufacturing in a diverse manufacturing environment plays an important role for robustness design of semiconductors, too. ESD protection is here probably the most prominent example. Over several decades electronics industry has developed standards and methods of safe handling of sensitive semiconductors in ESD protected areas (EPA) [9]. Now entering into industry like fashion or building industry, new awareness has to be created. The development of new tools and methods might be needed which are applicable in the rougher manufacturing world and that are cost efficient. The focus will be on the handling of small modules containing the semiconductor component as it is not expected that ICs or other discrete semiconductors will be handled standalone at that level of system manufacturing.

To address these questions a new international workshop on 'Robustness of IoT Devices' has been initiated. It will be held in September 2018 along with EOS/ESD Symposium [10]. The mission is to set a triggering point for in-depth discussion in industry and the standardization authorities about new methods in robustness design and qualification of IoT devices.

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Upcoming Technical Meetings

48th European Solid State Device Research Conference (ESSDERC)

September 3-6, 2018, Dresden, Germany

The European Solid State Device Research Conference (ESSDERC) is organized in parallel with the European Solid State Circuits Conference (ESSCIRC). The conference provides an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design made available by advances in semiconductor technology, calls for a deeper interaction among technology engineers, device experts, integrated circuit designers and system designers. While keeping separate Technical Program Committees, the conferences are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions, bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong. The topic of the 2018 ESSDERC conference are: CMOS Devices and Technology, Opto-, Power and Microwave Devices, Physical Modeling of Materials and Devices, Compact Modeling of Devices and Circuits, Memory Devices and Technology, Sensor Devices and Technology and Emerging non-CMOS Devices and Technologies.

The 2018 edition of the conference includes:

- Four Joint (together with ESSCIRC) Plenary Presentations from Bosch, Globalfoundries, Texas Instruments and IBM.
- Three ESSDERC keynote presentations from University of Tokyo, CEA-Leti and Stanford University, and
- Three ESSCCIRC keynote presentations from TU München and SiTime Corp.
- Two special focused sessions on
  - FDSOI and
  - Power Electronics
- Presentation of IEEE and ESSDERC/ESSCIRC awards
- Get Together and Conference Gala Dinner
- Tutorials on:
  - The Future of Mobility: Reliability, Readiness & Robustness of Integrated Circuits:
  - IC Design for Automotive
  - Ultra-Low Power Sensors for Condition Monitoring
- Workshops

The conference is organized in Dresden, Germany. With about 550,000 inhabitants, Dresden is the capital of the Free State of Saxony and well known as the semiconductor capital of Germany as well as one of the leading semiconductor sites in Europe. The region therefore is often referred to as Silicon Saxony. In Saxony, approximately 2,100 companies with more than 51,000 employees develop, manufacture, and promote integrated circuits, serve as materials and equipment suppliers to the chip industry, produce and distribute electronic products and systems based on integrated circuits, or develop and promote software. Saxony has an excellent research environment with 4 universities, 5 universities of applied sciences, 9 Fraunhofer Institutes, 4 Leibniz Institutes, 2 Max-Planck-Institutes and one Helmholtz Center. ESSDERC is financially sponsored by the IEEE Electron Devices Society. For registration and other information visit the home page at www.esscirc-essderc2018.org or contact Sistema Congressi at essxxrc@sistemacongressi.com.

2018 ESSDERC Local Committee

3rd Electron Devices Technology and Manufacturing (EDTM) Conference 2019

Conference Website: http://ewh.ieee.org/conf/edtm/2019/

Venue and Date: Marina Bay Sands Convention Centre, Singapore

March 12 - 15, 2019

Contact Email: edtm2019.sec@atenga.sg

Important Dates:

Extended Abstract Submission Deadline: October 15, 2018

Notification for Acceptance: December 30, 2018

EDTM

Launched in 2017 in Toyama, Japan, and fully sponsored by the IEEE Electron Devices Society (EDS), EDTM is fast becoming a flagship conference of IEEE EDS in Asia, with expanded focus on Advanced Technology Manufacturing. EDTM 18 was successfully held in Kobe, Japan, and it was well attended by more than 300 attendees and supported by close to 40 companies. EDTM is rapidly becoming a premier conference for the electron devices community, providing an unique forum to focus on research and development from leading universities and manufacturing companies worldwide on a broad range of device-related topics including materials, processes, devices, packaging, modelling, reliability, manufacturing, and yield. The conference location rotates among countries in Asia, and will be in Singapore for the first time in 2019.

Abstract Submission for EDTM 2019

You are invited to submit abstract in topics of devices, materials, packaging, reliability, modeling/simulation, manufacturing, tools, yield, packaging, to create new and innovative technologies. All abstracts must be submitted electronically at the conference website. If you have any questions, please contact our Conference Secretariat via the email edtm2019.sec@atenga.sg.

Save The Date

2018 IEDM—"Device Breakthroughs from Quantum to 5G and Beyond"

The Electron Devices Society's flagship annual conference, the IEEE International Electron Devices Meeting (IEDM) will be held December 1–5, 2018, at the Hilton San Francisco Union Square Hotel in San Francisco, California, USA.

The IEDM is the world's pre-eminent forum for reporting technological breakthroughs in semiconductor and electron device technology, design, manufacturing, physics, and modeling, with strong representation from speakers and attendees from around the globe.

Its scope encompasses silicon and compound semiconductor technology and devices, 2D and emerging material systems, and features topics such as nanometer-scale CMOS technology, advanced memory, neuromorphic computing, 5G and THz devices. Also, optoelectronics, displays, sensors, novel quantum and nano-scale devices and phenomenology, devices for power electronics and energy harvesting, as well as process technology and device modeling and simulation. Abstract Deadline: August 1, 2018. For Details: http://ieee-iedm.org/wp-content/uploads/2018/05/GENERAL-CfP-2018-1.pdf.

2018 IEEE International Flexible Electronics Technology Conference

August 7–9, 2018, Ottawa, Canada

http://2018.ieee-ifetc.org/

Welcome Participants!

On behalf of the IEEE IFETC Organizing Committee, it is our pleasure to welcome you to join us at the 2018 *IEEE International Flexible Electronics Technology Conference* (IEEE IFETC 2018) during August 7–9, 2018 at the Delta Hotel City Centre in Ottawa, Ontario, Canada.

The 1st IFETC 2018 is focused to provide attendees a unique opportunity to share, discuss, and be a part of new concepts, new ideas, and know-hows in all areas of flexible electronics technologies and their applications, including but not limiting to the following topical areas:

- Flexible transistors
- Flexible photovoltaics
- Flexible RFID and NFC Devices
- Flexible antennas and microwave devices
- Flexible energy harvesting
- Flexible sensors
- Flexible lighting and displays
- Smart textiles and wearables
- Chips and circuit design for flexible electronics
- Novel materials and processes for flexible electronics

The conference is scheduled to offer more than 130 presentations including 7 plenary/keynotes, 7 tutorials, over 30 invited talks by world renowned experts in the field, 3 workshops, and more than 90 contributed technical presentations.

The Ottawa Region (also known as Silicon Valley North) is Canada's top hub of technological innovation, enterprise, and research, making it an ideal location for hosting IFETC 2018. Located in the heart of downtown Ottawa—and steps away from the Rideau Canal, Parliament Hill, Byward Market, and much more—the Delta Hotel is perfectly suited for a world class conference like IFETC 2018 to provide you with access to the best that Ottawa has to offer.

We sincerely hope your participation to the excellent technical programs of IFETC 2018 to be held at one of the most beautiful locations in the Canada.

Look forward to seeing you in Ottawa, Canada for IEEE IFETC 2018!

Sincerely,
George Xiao and
Samar Saha
IEEE IFETC 2018 General Co-Chairs

Society News

Message from Editor-in-Chief

Dear EDS Members and Readers,

Carmen M. Lilley
Editor-in-Chief

Welcome to the April newsletter. For this newsletter, you will find articles of EDS events and activities throughout the globe that highlight the breadth of activities and outreach of EDS members. In addition, I would like to welcome two new members have joined our Editorial team; Rinus Lee from GLOBALFOUNDRIES, and Edmundo A. Gutiérrez, from *INAOE*. These two new volunteers will be responsible for promoting EDS activities in Regions 1, 2 and 3 (Eastern USA) and Region 9 (Latin America), respectively.

Rinus Lee is a Senior Member of Technical Staff at GLOBALFOUNDRIES in Malta, NY. He is an inventor of 19 issued/pending US patents and authored or co-authored 102 journal and conference papers. His research interest encompasses materials science and electrical engineering with a focus on process technology development for manufacturing nanometer-scale semiconductor devices.

Edmundo A. Gutiérrez has published more than 100 papers and international conferences in the field of semiconductor device physics, modeling, simulation, sensors, and circuits. He is author of the books "Low Temperature Electronics, Physics, Devices, Circuits and Applications" (Academic Press, 2000), and "Nano-Scaled Semiconductor Devices, Physics, Modeling, Characterisation, and Societal Impact" (The IET Press, 2016). Prof. Gutierrez got his PhD on Applied Sciences from The Catholic University of Leuven (KUL), Belgium, where he also spent 6 years as a research assistant at the Interuniversity MicroElectronics Center (IMEC) in the Advanced Silicon Processing Division. From 2000 to 2002 was the Design Manager of the Motorola Mexico Center for Semiconductor Technology, and from 2005 to 2007 Research Manager of the Intel Mexico Research Center. Currently Prof. Gutierrez is with the Department of Electronics of the National Institute of Astrophysics, Optics and Electronics (INAOE) in Puebla, Mexico. He is also the President of the Puebla EDS Chapter, President of the IEEE Puebla Section, member of the Board of Governors of IEEE EDS, member of the IEEE EDS Region 9 Outstanding Student Paper Award Committee, and Associate Editor of Electron Device Letters.

Carmen M. Lilley
Editor-in-Chief, EDS Newsletter
Email: clilley@uic.edu

EDS Board of Governors (BoG) Members-at-Large Election Process

Samar Saha
Chair of EDS Nominations & Elections

The Members-at-Large (MAL) of the EDS Board of Governors (BoG) are elected for staggered 3-year terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; and Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP—formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening. On May 20, 2017, the BoG approved to set a lifetime limit of two terms for a volunteer to serve as a BoG Member-at-Large, which must be considered for nominations.

The EDS BoG also approved to discontinue the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. Accordingly, all nominees will be voted on by the EDS BoG in its meeting in December, 2018. All electees begin their term in office on January 1, 2019. The nominees need not be present to run for the election. In 2018, seven positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG MAL. Self-nomination is allowed. Endorsers should send a brief email to Laura Riello stating that they would like to endorse the candidate. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be October 15, 2018. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting in December 2018.

Samar Saha
Chair of EDS Nominations
& Elections

Call for Nominations—EDS Board of Governors

Samar Saha
Chair of EDS Nominations & Elections

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting on Sunday, December 2, 2018. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

According to the two related motions passed at the mid-year BoG meeting held in Kochi, India, on May 21, a member can only serve for a maximum of two terms as a BoG member in a lifetime and the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership will be discontinued going forward. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on January 1, 2019. The nominees need not be present to run for the election. In 2018, seven positions will be filled.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Constitution and Bylaws. The electees are required to attend at least one BoG meeting every year. While the December meeting is organized in conjunction with the *IEEE International Electron Devices Meeting*, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend BoG meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the nominators and the endorsers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large.

Please submit your EDS BoG nomination by October 15, 2018, using the online nomination form at: (https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/).

Also, all endorsements letters should be sent to the EDS Executive Office, Laura J. Riello via e-mail: l.riello@ieee.org by October 15, 2018. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at samar@ieee.org.

Samar Saha
Chair of EDS Nominations
& Elections

IEEE Annual Election—Don't Forget to VOTE

This is a reminder for EDS members to vote in the 2018 IEEE Annual Election for the following positions and candidates. Listed below are the positions and candidates that will appear on the 2018 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2019	• Toshio Fukuda (Nominated by Petition) • Vincenzo Piuru (Nominated by IEEE Board of Directors) • Jacek M. Zurada (Nominated by IEEE Board of Directors)
IEEE Region Delegate-Elect/Director-Elect, 2019–2020 Region 2 (Eastern USA)	• Barry C Tilton (Nominated by IEEE Region 2) • Philip M Gonski (Nominated by IEEE Region 2) • Emilio M Salgueiro (Nominated by IEEE Region 2)
IEEE Region Delegate-Elect/Director-Elect, 2019–2020 Region 4 (Central USA)	• Johnson A Asumadu (Nominated by IEEE Region 4) • Tarek Lahdhiri (Nominated by IEEE Region 4)
IEEE Region Delegate-Elect/Director-Elect, 2019–2020 Region 6 (Western USA)	• Charles M Jackson (Nominated by IEEE Region 6) • Timothy T Lee (Nominated by IEEE Region 6)
IEEE Region Delegate-Elect/Director-Elect, 2019–2020 Region 8 (Europe, Middle East and Africa)	• Rafal Sliz (Nominated by IEEE Region 8) • Antonio Luque (Nominated by IEEE Region 8)
IEEE Region Delegate-Elect/Director-Elect, 2019–2020 Region 10 (Asia and Pacific)	• Deepak Mathur (Nominated by IEEE Region 10) • Norliza M Noor (Nominated by IEEE Region 10) • Ziauddin "Zia" Ahmed (Nominated by IEEE Region 10)
IEEE Standards Association Board of Governors Member-at-Large, 2019–2020	• Mark Epstein (Nominated by IEEE Standards Association) • Glenn W Parsons (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2019–2020	• Robby Robson (Nominated by IEEE Standards Association) • Jun Yu (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2019	• F D "Don" Tan (Nominated by IEEE Technical Activities) • Kazuhiro Kosuge (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2019	• James M Conrad (Nominated by IEEE-USA) • Maura Kathleen Moran (Nominated by IEEE-USA)

Balloting period starts on 15 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 1 October 2018. All eligible voting members should look for their ballot package to arrive via postal mail or access it electronically at www.ieee.org/elections. For more information on the election and candidates, visit the IEEE Annual Election Web page at www.ieee.org/elections, or email election@ieee.org.

Enhance Your Career with IEEE Senior Membership!

Dear EDS Members:

Ru Huang
EDS Vice President of Membership and Services

On behalf of the IEEE Electron Devices Society (EDS), we are writing to let you know about an opportunity to elevate your IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. Learn more at, https://www.ieee.org/content/index1.html.

If you have been in professional practice for 10 years, and have at least five years of significant performance, you may be eligible for Senior Membership. One's educational history is counted towards this 10-year requirement (e.g., three years for Bachelor of Science, etc.)

To apply for IEEE Senior Member grade, please complete the online application form.

If you would like to help fellow EDS members upgrade, plan a Senior Member Elevation Event at your local EDS chapter. The step-by-step IEEE Senior Membership Nomination Event Guide is available on the IEEE website, at https://www.ieee.org/membership/senior/senior-member-elevation-toolkit.html.

Thank you for supporting IEEE and EDS!

Ru Huang
EDS Vice President of Membership and Services
Peking University
Beijing, China

Award Winners and Journal EiC Calls for Nominations

Congratulations to Martin A. Green—EDS Celebrated Member!

Martin A. Green

To honor and recognize esteemed EDS alumni, EDS created the Celebrated Member Program. Those of us in EDS can take pride in the accomplishments of these Celebrated Members and draw from the inspiration to advance our field and to achieve more, because it is not only their work but ours as well, that can help transform the world around us.

Recently, Professor Green was presented with the EDS Celebrated Member Award at the 2018 IEEE World Conference on Photovoltaic Energy Conversion (WCPEC-7), held at Hilton Waikoloa Village, Hawai'i.

For a complete bio for Prof. Green, please visit the EDS Celebrated Member gallery, at https://eds.ieee.org/celebrated-members.html.

Martin Green receiving the EDS Celebrated Member Award from Fernando Guarín, EDS President (2018–2019)

2018 IEEE William R. Cherry Award Winner

Vasilis Fthenakis 2018 IEEE William R. Cherry Award Winner

Vasilis Fthenakis, Founder and Director of the Center for Life Cycle Analysis at Columbia University, and Senior Scientist Emeritus at Brookhaven National Laboratory, will receive the William Cherry award for his pioneering research at the interface of energy and the environment, that catalyzed photovoltaic technology advancement and deployment world-wide.

Vasilis was born in Greece, to a family of chemists, and got his first degree in Chemistry from the National University of Athens, Greece. He came to the US planning to pursue graduate studies in Chemistry and to avoid prosecution from the military regime that he actively opposed during his student years. He completed his MS degree in Chemical Engineering at Columbia, where he was awarded a graduate research assistantship (GRA), modeling heterogeneous catalysis systems, under Professor John Happel. He also worked at Columbia's Fossil Energy coal-biomass gasification pilot-plant before joining Brookhaven National Laboratory (BNL) as a research engineer on Energy Modeling and subsequently on Environmental Health and Safety (EH&S).

While at BNL, he obtained a PhD on Fluid Dynamics and Atmospheric Science from New York University developing the model HGSPRAY that has been widely used in the refinery industry for designing water curtain safety systems and authored the book "Prevention and Control of Accidental Releases of Hazardous Gases"; for this work was honored as a Fellow of the American Institute of Chemical Engineers "in recognition and appreciation of superior attainments, valuable contributions, and service to Chemical Engineering."

Vasilis pivotal work on PV–EH&S has enabled PV penetration in many global markets, and for his contributions was made Fellow of the International Energy Foundation and tasked to Head of the National Photovoltaic Environmental, Health and Safety (PV-EH&S) Center, at BNL, where he served as one of only two tenured senior scientists in a Directorate of 140 scientists. The PV-EH&S Center assisted the US PV industry in maintaining safe and environmental facilities and its early studies created the "Gold standard" for EH& in today's production facilities. For his contributions, he received commendations from the US DOE and the Director of the National Renewable Energy Laboratory (NREL) for exemplary performance on PV safety analysis. Dr. Fthenakis expanded the Center's activities to Life Cycle Analysis and Recycling; he conceptualized and conducted innovative research on the life cycle of PV that opened the door to Europe and Asia for the U.S. thin film PV industry. He foresaw the European trends towards banning products containing lead and cadmium and guided the crystalline silicon and the cadmium telluride industries in overcoming these barriers.

In 2006, he accepted an invitation from Columbia to establish a new Center for Life Cycle Analysis (CLCA) and since then he has been sharing his time between BNL and Columbia. He is the author of "Solar Electricity: Systems Integration and Sustainability, 2018," editor of two books on Life Cycle Analysis, a book on "3rd Generation Photovoltaics," and author or co-author of about 400 scientific articles and reports. Among his more noteworthy publications is "A Solar Grand Plan," Scientific American, 2008 with Zweibel and Mason, which was translated into eleven languages. Other representative examples of his prolific work include the development of CdTe PV module recycling technologies, material resource assessments, and leading life-cycle studies that are a crucial contribution to today's key debates about energy and climate change. His peer-reviewed articles have been cited more than 8,000 times, and he serves in the Editorial Boards of Progress in Photovoltaics, Energy Technology, Energies and Journal of Loss Prevention.

Christiana Honsberg
2018 Cherry Award Chair

2016–2017 EDS Region 9 Outstanding Student Paper Award

The Electron Devices Society confers its prestigious Region 9 Outstanding Student Paper Award to the best Region 9 student paper published in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. The winning paper is titled, "*A DC Method to Extract Mobility Degradation and Series Resistance of Multifinger Microwave MOSFETs.*" This paper was published in the *IEEE Transactions on Electron Devices* and was authored by Andrea Sucre-Gonzalez, Fabian Zarate-Rincon, Adelmo Ortiz-Conde, Reydezel Torres-Torres, Francisco J. Garcia-Sanchez, Juan Muci and Roberto S. Murphy-Arteaga. The award will be presented at the Symposium on Microelectronics Technology and Devices (SBMicro), which will be held August 27–31, 2018, in Rio Grande Do Sul, Brazil. The Award consists of a certificate and reimbursement of up to US $1,500 to cover one author's travel and accommodations to attend the conference.

On behalf of the Electron Devices Society, I would like to congratulate Andrea Sucre-Gonzalez and the remaining authors for this achievement. Brief biographies of all the authors of the paper are given below.

Andrea Sucre-González obtained the Electronics Engineer degree (Cum Laude) in 2013 and the M.E. (with Honors) in 2015, both from Universidad Simón Bolívar (USB), Caracas, Venezuela. She currently is a Ph.D. candidate and research assistant at USB's Solid State Electronics Laboratory.

Fabián Zárate-Rincón (S'14) received the B.S. degree in Electronics Engineering from the Universidad del Quindío, Colombia, the M.S. degree in Electronics from Instituto Nacional de Astrofísica, Óptica y Electrónica, Puebla, Mexico (INAOE), and currently is a Ph.D. candidate at INAOE.

Adelmo Ortiz-Conde (S'82–M'85–SM'97) received the Electronics Engineer degree from USB, and the M.E. and Ph.D. degrees from the University of Florida. He is a Full Professor at USB, an EDS Distinguished Lecturer, and editor of Electron Device Letters.

Reydezel Torres-Torres (S'01–M'06–SM'15) is a senior researcher at the Electronics Department of INAOE, Puebla, Mexico. He received his Ph.D. from INAOE. He has worked for Intel Laboratories in Mexico and Imec in Belgium.

Francisco J. García-Sánchez (M'76–SM'97) received the B.E.E., M.E.E. and Ph.D. degrees in Electrical Engineering from the Catholic University of America, Washington, DC. He is a Professor Emeritus of USB, and EDS Distinguished Lecturer.

Juan Muci received the Electronics Engineer degree from USB, and the M.S. degree from Pennsylvania State University, State College, Pennsylvania. He is a faculty member at the Electronics Department of USB where he currently is a Full Professor.

Roberto S. Murphy-Arteaga (M´92, SM´02) received a B.Sc. degree in Physics from St. John's University, Minnesota, and the M.Sc. and Ph.D. degrees from INAOE, Puebla, México. He is a senior researcher with the Microelectronics Laboratory at INAOE, and EDS Distinguished Lecturer.

Arturo Escobosa
EDS Region 9 Outstanding Student Paper Award Chair
CINESTAV-IPN
Mexico

Call for Nominations for Editor-in-Chief
IEEE Electron Device Letters

Since 1980, the IEEE Electron Device Letters (EDL) has been a flagship publication of the IEEE Electron Devices Society (EDS). EDL publishes original and significant contributions relating to the theory, modeling, design, performance and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanoelectronics, optoelectronics, photovoltaics, power ICs and micro-sensors. EDL offers a forum for rapid dissemination of significant original research with an average publishing cycle time 4 weeks.

We invite nominations for the position of Editor-in-Chief (EiC) for either EDL or T-ED for a 3-year term beginning in the fourth quarter of 2018. The EiC's duties include appointing Editors to serve across the scope of either journal; supervising the operations of the journal through ScholarOne Manuscripts with the assistance of the IEEE publications staff; monitoring the quality and timeliness of publications; and leading development to strengthen the journal.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time on the job;
- Demonstrated competence in at least one of the disciplines included in the EDS field of interest;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving on one of the editorial boards of T-ED, EDL (the IEEE Electron Device Letters), or J-EDS (the IEEE Journal of the Electron Devices Society);
- Suitable temperament (ability to work at all levels: editorial boards, IEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS;
- Other desirable qualifications include leadership experience, integrity and ethical standards, organizational and management skills, and a vision for moving the journal to a new level of excellence.

Requirement for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- Endorsement from two EDS members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please e-mail the nomination materials to: James Skowrenski (J.Skowrenski@ieee.org) by **July 31, 2018**.

Hisayo S. Momose
Interim VP of Publications and Products
IEEE Electron Devices Society

Call for Nominations for Editor-in-Chief
IEEE Transactions on Electron Devices

For more than 60 years, the IEEE Transactions on Electron Devices (T-ED) has been a flagship publication of the IEEE Electron Devices Society (EDS). T-ED publishes original and significant contributions relating to the theory, modeling, design, performance and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanoelectronics, optoelectronics, photovoltaics, power ICs and micro-sensors. TED publishes regular full-length papers, review papers, invited papers, and special issues. The average publishing cycle time is 13 weeks.

We invite nominations for the position of Editor-in-Chief (EiC) for either EDL or T-ED for a 3-year term beginning in the fourth quarter of 2018. The EiC's duties include appointing Editors to serve across the scope of either journal; supervising the operations of the journal through ScholarOne Manuscripts with the assistance of the IEEE publications staff; monitoring the quality and timeliness of publications; and leading development to strengthen the journal.

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- Demonstrated competence in at least one of the disciplines included in the EDS field of interest;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving on one of the editorial boards of T-ED, EDL (the IEEE Electron Device Letters), or J-EDS (the IEEE Journal of the Electron Devices Society);
- Suitable temperament (ability to work at all levels: editorial boards, IEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS;
- Other desirable qualifications include leadership experience, integrity and ethical standards, organizational and management skills, and a vision for moving the journal to a new level of excellence.

Requirement for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- Endorsement from two EDS members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please e-mail the nomination materials to: James Skowrenski (J.Skowrenski@ieee.org) by **July 31, 2018**.

Hisayo S. Momose
Interim VP of Publications and Products
IEEE Electron Devices Society

Call for Nominations Editor-in-Chief
IEEE Journal of Microelectromechanical Systems

Over the past four decades the market for Microelectromechanical Systems MEMS has grown to 20 billion dollars at a rate of 10–14% every year. In the early days automotive and consumer applications drove the development of MEMS. Today smart phones, mobile devices, and the Internet of Things would not be what they are without MEMS. Future scenarios for autonomous systems, i.e. sensor systems, cars, drones, and smart environments such as smart buildings and smart cities, will further boost the demand for MEMS innovations in the continuous humanization of technology toward non-obtrusive and ubiquitous human-machine interfaces and the Internet of Healthcare. Research in MEMS is driven by challenges for further miniaturization and ultra-low power consumption while maintaining high performance and negligible cross-talk with adequate reliability. New functional devices will be developed at the interface of mechanics, electronics, and biology, enabled by advanced material integration and novel fabrication technologies like 3D printing on the micro- and nanoscale.

Since 1992 the Journal of Microelectromechanical Systems (JMEMS, https://eds.ieee.org/journal-of-microelectromechanical-systems.html) has developed into the leading journal in the field of MEMS and MEMS technology. JMEMS publishes original and significant contributions describing advances in the field and relating to the theory, modeling, design, fabrication, assembly and packaging, performance characterization and reliability of microelectromechanical systems. In general, JMEMS papers and letters contain experimental data, verifying theory or model/simulation-based new concepts. The journal publishes original papers, letters and review papers. Original contributions are solicited from all sub-fields of MEMS, and in topical focus areas which are continuously introduced and highlighted. Current examples are: "Design, Fabrication, Test and Applications of MEMS Inertia Sensors and Resonators"; "Fabrication and Integration Technology for BioMEMS"; "MEMS Technologies for the Internet of Things (IoT)"; "Nonlinear Phenomena in MEMS and NEMS".

IEEE JMEMS is co-sponsored by the Electron Devices Society, Robotics and Automation Society and Industrial Electronics Society.

Nominations are invited for the position of Editor-in-Chief (EiC) for J-MEMS for a 3-year term beginning in **October 2018**.

The EiC's ongoing duties include assigning submitted manuscripts to one of the associate or senior editors who cover the range of technology and application specific domains. The EiC makes the final decision regarding the disposition of each manuscript submitted to JMEMS based upon the recommendation of the associate or senior editors. The EiC further develops the journal by initiating new special topical focus areas and soliciting review papers with support from the associated and senior editors. JMEMS publishes six issues per year, each approximately 200–250 pages comprising 20–30 Letters and full-length papers.

The EiC is helped administratively by a person from the IEEE publications staff.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time to assign manuscripts and reviewing the acceptance or rejection recommendations made by the associate or senior editors;
- Demonstrated technical leadership within the field of MEMS;
- Formal support from the institution for which the nominee works (waived if self-employed or employed at an academic institution);
- Has served or currently is serving as associate or senior editor of JMEMS or another journal in the field of MEMS and solid-state sensors and actuators.
- Commitment to guide JMEMS according to this Call for Nominations and to further actively develop the journal;
- Willingness to work collaboratively with internal and external stakeholders to ensure the technical leadership and fiscal health of JMEMS.

Requirements for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity (can be waived, see above);
- Endorsement from two IEEE members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please email the nomination materials to: James Skowrenski (J.Skowrenski@ieee.org) no later than **July 31, 2018**.

Hisayo S. Momose
Interim VP of Publications and Products
IEEE Electron Devices Society

Early Career Award

Jack Dempsey, NREL Contract Photographer

CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Early Career Award. The award is presented annually to promote, recognize and support early career technical development within the Electron Devices Society's field of interest.

Prize: $1,000, a certificate, and travel expenses to attend the award presentation at the annual EDS GOLD Lecture that is held in conjunction with the IEEE International Electron Devices Meeting (IEDM).

Eligibility: Candidate must be an IEEE EDS Young Professional member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Deadline: August 15

For more information:

http://eds.ieee.org/early-career-award.html

IEEE Advancing Technology for Humanity

2018 IEEE Electronic Endeavor Match

Following the success of the 1st IEEE Electronic Endeavor Match in 2017, the 2nd IEEE Electronic Endeavor Match was held in Hong Kong Science Park on April 7, 2018. There have been efforts to introduce electronic circuit concepts as part of the STEM (Science, Technology, Engineering and Mathematics) to pre-university students. The IEEE Electronic Endeavor Match is aimed as recognizing primary and secondary school students who have developed their interest and skill in constructing electronic circuits.

The participants were from different elementary and middle schools in Hong Kong. There are totally 98 participants. The participants were divided into 3 different groups according to their age. After a 3-phase competition, the committee selected 3 awardees and the best design award from each group. The students exhibited their interest on electronic circuits and provide positive feedbacks on this event. More event about the match can be found in http://www.ieee-elex.org/eem2018

~ Mansun Chan

Venue of the Competition

Award ceremony

Chapter News

EDS Chapter Subsidies for 2019

EDS is providing funds to those chapters that are requesting a subsidy based on the EDS chapter subsidy guidelines. The deadline for EDS chapters to request a subsidy for 2019 is September 1, 2018. In 2018, EDS awarded subsidy funds to 61 chapters, with most amounts primarily ranging from US$500 to US$1,000. All Chapter Chairs were informed through an email notifying the subsidy details and guidelines in June. Chapter subsidy is pegged to the activities reported and chapter growth. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for EDS student activities at local institutions.

Chapter Subsidies can be requested by completing the EDS Chapter Subsidy Request Form http://eds.ieee.org/chapter-subsidy-program.html. Please note that the 2019 subsidy request needs to be submitted by September 1st, 2018.

Final decisions concerning subsidies will be made in December 2018. Subsidy checks will be issued by early January of the following year. Please visit the EDS website http://eds.ieee.org/chapter-subsidy-program.html for more information.

Your Chapter Could Be Missing Important Notices and Funding Opportunities!

Please remember, whenever there is a change to Chapter Officers, both IEEE and EDS must be notified. Please follow these two steps:

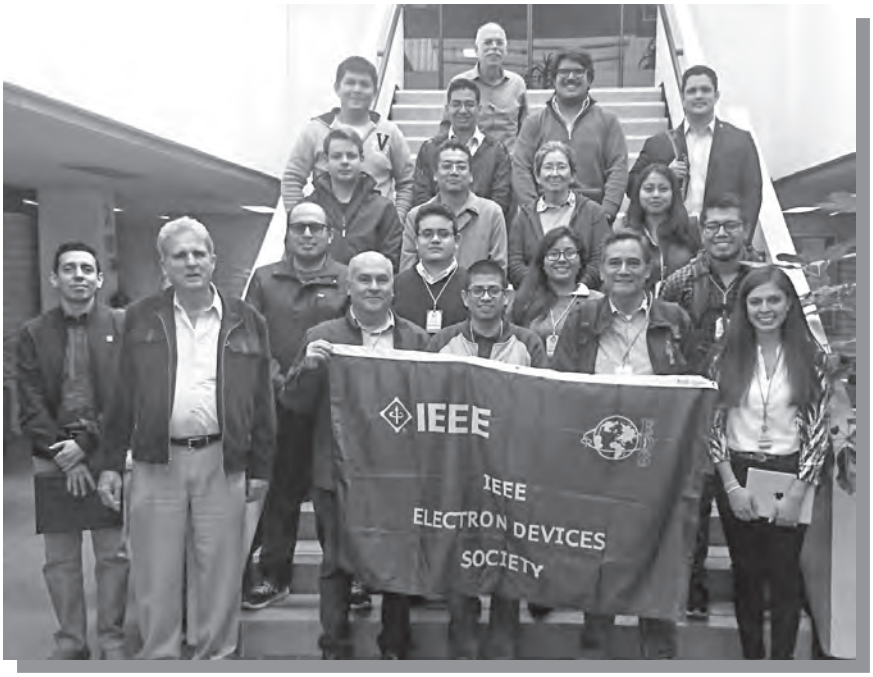
1) Report officer changes to IEEE via the vTools Officer Reporting form: https://officers.vtools.ieee.org/ (*access to vTools requires use of an IEEE account*).
2) Report officer changes to EDS by completing the Chapter Chair Update Form: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

Thank you in advance for your assistance.

Mexican Chapters Meeting

The third EDS Mexican Chapters Meeting took place in Mexico City on November 24, following the events in Cholula, Puebla in 2015, and Boca del Río, Veracruz, in 2016. These meetings have proved to be a useful activity in order to exchange opinions, increase interaction and discuss the different problematic found by each chapter.

There were 20 participants representing six Mexican and two recently created Nicaragua ED chapters. After a brief introduction exposing the IEEE guidelines, every chapter gave a brief presentation of the main activities made during last year. We finished discussing the difficulties found by the different chapters, including strategies to attract more people to join EDS. Worth to mention are the activities of the EDS-ETC program mainly made by the chapter in Puebla and Morelia.



Attendees of the EDS Mexican Chapters Meeting

IEEE ED Schenectady Chapter 2017 Mini-Colloquium

By Rinus Lee

The EDS Schenectady Chapter organized a mini-colloquium (MQ) in collaboration with GLOBALFOUNDRIES in Malta, New York, on September 22, 2017. The theme of the MQ was "Green Electronics". Three IEEE EDS distinguished lecturers and IEEE Fellows; Prof. Paul Yu from UC San Diego, Prof. Suman Datta from Notre Dame and Prof. Michael Shur from RPI were invited to anchor the morning plenary program. Prof. Yu started off the morning strongly by inviting the audience to share in the vision of "Going Green" with UC San Diego's campus wide initiatives in PV, EV, MicroGrids and Building Efficiency. Next was Prof. Datta, who gave us an excellent overview of how semiconductor manufacturing has evolved from classical-scaling to equivalent-scaling, and how energy efficient nano-electronics will be critical to meet the demands of next generation applications. To cap the lectures, Prof. Shur delivered an excellent talk on terahertz sensing technology. These three invited talks provided a well-rounded perspective on future opportunities for semiconductor manufacturing. There were about 300 attendees, comprising of students, faculty members and IEEE members from the capital region.

Left to Right: Rinus Lee, Fernando Guarin, Paul Yu, John Pellerin, Janet Tinkler, Mukta Farooq, Suman Datta and Michael Shur

Workshop on Robustness of IoT Devices

EOS/ESD Symposium-September 23–28, 2018

Today's electronic industry is challenged by the needs of ubiquitous Internet of Things (IoT) penetrating into all realms of society, business and personal life. The basic functional building blocks of IoT devices are sensing, computing and connecting. There is a plethora of IC solutions for each of these features available and their performance is continuously growing. The driving factors are high integration and economical scaling of high volume that enable highest performance at lower cost rates. To fully exploit this for IoT applications, a single IC solution should be scaled into many applications ranging e.g. from industrial to consumer. Here are the expected challenges that arise: IoT modules needs to comply with very different reliability and robustness requirements depending on the application and the environment. At the same time, the costs have to be kept to a minimum for the devices. This can only be achieved by reusing IC hardware for dispersed applications, where the semiconductor components comply with a base robustness level in terms of lifetime reliability and robustness against transients, while the integration on module level ensures the specific requirements of the application. This leads to the questions:

- What is the adequate 'base robustness' of semiconductor devices considering technical and economic aspects?
- What are the appropriate methods to meet overall module robustness based on robustness of ICs by module design? Examples are redundancy, software and firmware adjustment (e.g. throttling), heat sinks, shielding, etc.
- What kind of specific protective measures have to be taken during manufacturing, assembly and test of the IoT modules to guarantee high yield and avoid latent pre-damage? This includes e.g. non-common manufacturing environment of electronics like in the case of wearables.
- What are the test standards to be applied on IC and module level to verify the robustness target?

The workshop intends to bring together experts and industry leaders with strong engagement in IoT and who are concerned about the robustness of IoT devices. As this is a first-of-a-kind workshop, the focus is on sharing of requirements of various application fields and discussion on the need of new approaches and standards beyond what already exists. There will be two discussion rounds addressing this in an open workshop debate and a final panel discussion. The program will offer a row of speeches by technology leaders in the field of IoT. More information on this workshop can be found by visiting: https://www.esda.org/events/symposia/workshop-on-robustness-of-iot-devices/

~ Harald Gossner,
IoT Workshop Chair

How to Plan an EDS Distinguished Lecture or Mini-Colloquium Event

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

✓ **Checklist**

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index)
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

Regional News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

ED/CAS North Jersey

—by Durga Misra

The ED/CAS Chapter of North Jersey Section organized four talks in the 1st half of 2018. The talks in March were jointly organized with the AP/MTT Chapter. On March 19, 2018, Dr. Vincenzo Piuri (DL) of Università degli Studi di Milano, Italy visited and gave a talk on "Intelligent Signal and Image Processing in the Wood Industry." Dr. Vincenzo Piuri described the technologies used for data analysis and knowledge extraction based on machine learning in the wood manufacturing industry. Following that, the chapter hosted Dr. Walid Ali-Ahmad (DL) of UC San Diego, Jacobs School of Engineering on March 27, 2018. Dr. Walid delivered a talk on "Advanced RF Front-End and Transceiver Systems Design Overview for Carrier Aggregation based 4G/5G Radios." Following that, Prof. Dr. Ignacio Gil of Universitat Politècnica de Catalunya, Spain visited and gave a talk on "Antenna and Transmission Lines for Wearable Systems" on April 5, 2018. To cap off the successful 1st half of 2018 in terms of technical talks, the chapter had Dr. K.L. Ganapathi of IIT Madras, India visit and Dr. Ganapathi gave a lecture on "Integration of High-k Gate Dielectrics with 2D Materials for Next Generation Logic and Memory Applications." An overview of the major issues in realizing electronic devices using 2D materials, especially on the development of high-k dielectric thin films for high performance and low power 2D material devices were discussed.

~ Rinus Lee, Editor

Workshop on Technologies, Trends, and Prospects of Renewable Energy Projects at Universidad Simón Bolívar, Venezuela

The first "Workshop on Technologies, Trends, and Prospects of Renewable Energy Projects" took place on Thursday December 7, 2017 at Universidad Simón Bolívar, Caracas, Venezuela. The event consisted of a series of four seminars related to ongoing research and practical challenges in the topic of renewable energy. The first tutorial was lead by Professor Orlando Trejo, who presented a lecture titled "Dependence of the Conversion Efficiency of PV Cells with the Manufacturing Semiconductor Band Gap." Next, Professor Raúl Barroso presented his lecture on "Potential of Metamaterials in Solar PV Cell Fabrication", and was followed by Professor Víctor Guzmán with his tutorial titled "Power Electronics in Renewable Energy Applications." Finally, Professor Miguel Díaz closed the session with his presentation titled "Communication Systems for Smart Grids."

The audience included 15 professionals from multiple disciplines and institutions from Venezuela, who engaged in dynamic discussions with the presenters. The informal meetings after the conclusion of the workshop served as a starting point for further collaboration, aiming to integrate expertise from multiple fields to tackle current challenges relevant to renewable energy technology. For additional information visit gsiep.labc.usb.ve/usbcas2017/ or contact Professor Orlando Trejo at orlandotrejo@ieee.org

~ Edmundo Guiterrez, Editor

Europe, Middle East & Africa (Region 8)

IEEE Ukraine Section (Kyiv) ED/MTT/CPMT/SSC/COM Societies Joint Chapter

IEEE Ukraine Section (Kharkiv) SP/AP/C/EMC/COM Societies Joint Chapter

—by Mikhail Ilchenko, Kateryna Ivanko, Mariya Antyufeyeva, and Yuriy Poplavko

The II International Conference on Information and Telecommunication Technologies and Radio Electronics (UkrMiCo-2017) was organized in the mainland of Ukraine instead of the previous conferences regularly held during 25 years of in the Crimea peninsula. The conference was held September 12–15, 2017 at Odessa National Academy of Communications named after A. Popov. It was co-organized and co-sponsored by IEEE Ukraine Section, IEEE Ukraine Section (Kyiv) ED/MTT/CPMT/SSC/COM Societies Joint Chapter and IEEE Ukraine Section (Kharkiv) SP/AP/C/EMC/COM Societies Joint Chapter as well as by National Technical University of Ukraine "Igor Sikorsky Kiev

First workshop in renewable energy technology: Presenters and part of the audience

Polytechnic Institute," Odessa National Academy of Communications.

The conference program consisted of the plenary sessions and four section sessions: "Radio Engineering," "Electronics," "Telecommunications" and "Infocommunications." A total of 148 papers were submitted for presentation at the Conference and 110 submissions were accepted. The full list of the authors contained 160 researchers from 14 countries, namely from Armenia, Azerbaijan, Belgium, Belarus, Dania, Lithuania, United Kingdom, Israel, Poland, Portugal. More than 150 researchers attended the Conference. The working language of the conference was mainly English.

During the conference many interesting reports were presented in the area of radio-electronics, modern nanotechnology, micro- and nanoelectronics components, design methods of electronic circuits and systems, as well as the latest developments concerning electronic systems and processing of signals and images. There were also fruitful scientific debates to discuss the possibilities of international cooperation and implementation of joint research projects, involving wide range of national and international scientific organizations.

The Conference Proceedings are published in English and meet the requirements of conferences provided under the auspices of IEEE. The conference papers are indexed in IEEE *Xplore*, Scopus, Google Schoolar international scientific-metric databases.

IEEE IRE NASU-Kharkiv ED-S Student Branch Chapter

IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Societies Joint Chapter

—by Daryna Pesina and Kateryna Arkhypova

The 2017 IEEE International Young Scientists Forum on Applied Physics and Engineering (YSF-2017) is one of "the club of six" IEEE IAS co-sponsored student led technical conferences for 2017. The Forum was successfully held on October 17–20, 2017 in one of the most beautiful cities of Ukraine, in magnificent Lviv with its historic part recognized as a World Heritage by UNESCO. The event was hosted by the Scientific Library of Ivan Franko National University of Lviv.

The event was co-organized by the O. Ya. Usikov Institute for Radiophysics and Electronics NAS of Ukraine and its Young Scientists Council, Ivan Franko National University of Lviv, Karpenko Physico-Mechanical Institute NASU, and IEEE IRE NASU-Kharkiv AP-S, ED-S, MTT-S, IA-S, SSC-S Student Branch Chapters. The YSF-2017 gained a lot of support from the sponsors: IEEE Industry Applications Society, IEEE West Ukraine Joint Chapter and IEEE Ukraine Section Young Professionals Affinity Group became the technical co-sponsors of the event, while IEEE East Ukraine

Plenary talk by the IEEE IA-S president Dr. Tomy Sebastian at the Grand Hall of the Scientific Library of Ivan Franko National University of Lviv (left) and general photo of the YSF-2017 attendees (right)

Joint Chapter, IEEE Ukraine Section Women in Engineering Affinity Group, EPS, Kharkiv EPS Young Minds Section, and EuMA provided Forum with the financial support.

The YSF-2017 gathered together over 150 young scientists, engineers, and invited speakers (including more than 40 IEEE members) from all over the world. The geography of participants included 29 cities of 10 countries including USA, UK, Spain, Poland, Estonia, Turkey, Italy, Hungary, Egypt, and Ukraine. The technical program included presentations on a broad range of topics including Biological and Medical Physics, Optics and Photonics, Computational and Experimental Electromagnetics, Microwave and Terahertz Electronics, Nano- and Metamaterials, Information Systems and Nondestructive Testing, Power Electronics and Industry Applications, Solid State Physics, Nuclear and Plasma Physics, Multiwavelength Astronomy, Geoscience and Remote Sensing.

The list of the invited speakers of the Forum included two IEEE Distinguished Lecturers: Dr. Valery Zavorotny (GRS-S Distinguished Lecturer, NOAA Earth System Research Laboratory, Boulder, Colorado, USA) and Dr. Patric Muggli (NPS-S Distinguished Lecturer, Max Planck Institute for Physics, Munich, Germany), Dr. Tomy Sebastian (IEEE Industry Applications Society president, Michigan, USA), Prof. Gregory Quarles (OSA chief scientist, Washington D.C., USA), Dr. Leonid Ponomarenko (Lancaster University, Lancaster, UK), Dr. Carlos Roncero-Clemente (University of Extremadura, Badajoz, Spain), and DSc. Valeriya Trusova (V.N. Karazin Kharkiv National University, Kharkiv, Ukraine).

The unique feature of the event, which traditionally gains interest among the participants, is a successful combination of a scientific program with various soft skill trainings. This year Forum offered workshops on scientific writing in English, improving skills of public speaking, grant proposal writing as well as insights into the grant programs of the European Union, NATO, DAAD and other organizations. On October 21, 2017 the YSF-2017 satellite event, the CS-oriented workshop "Microscope, Money, and Two Useful Nails" was organized at the Ukrainian Catholic University. It was aimed at a collaboration between young scientists and Ukrainian IT companies.

Last, but not least, the YSF has always been not just a scientific platform for the career development of young scientists, but also a place for effective communication. The fascinating social program of this year's Forum prepared by the organizers was an integral part of the event. The welcome reception of the Forum, aimed at enhancing the participants' networking, was organized by the IEEE Ukraine Section Women in Engineering Affinity Group at the Robert Doms Beer House. Social program also included library excursion, city tour and the farewell party.

YSF-2017 was the IEEE conference, so there was IEEE stand working each day of the Forum which contributed greatly to the promotion of IEEE itself and its units involved in the organization of the event.

IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Chapter

—by Nikolay Cherpak and Kateryna Arkhypova

Several times a year, our Chapter holds technical meetings with the themed presentations at the Usikov Institute for Radiophysics and Electronics NASU in Kharkiv. These meetings cover multiple topics concerning all aspects of engineering, theoretical and experimental physics, electron devices, semiconductors, etc. This year, we have already held 14 such meetings. Also, we carry on a tradition to encourage Ukraine IEEE members with the awarding ceremony for publication in the IEEE Journals related to AP/MTT/ED/AES/GRS/NPS technical societies. As a part of the annual IEEE Publication Encouragement Award, there were 15 Ukrainian teams of contributors whose papers have been published this year in IEEE journals, namely in IEEE Transactions on Antennas and Propagation, IEEE Transactions on Electron Devices, IEEE Transactions on Plasma Science, IEEE Microwave and Wireless Components Letters, IEEE Geoscience and Remote Sensing Letters, and others.

ED/COM/AP/MTT/EMC Tomsk Chapter

—by Oleg Stukach

The Moscow Workshop on Electronic and Networking Technologies (MWENT 2018) and Siberian Conference on Control and Communications (Sibcon-2018) were jointly held in Moscow on March 14–16, 2018. The seminar took place in Moscow Institute of Electronics and Mathematics of National Research University Higher School of Economics (MIEM HSE). The event was devoted to numerous issues of electronics development

Session of the joint MWENT 2018 workshop and Sibcon-2018 conference

and its integration into the modern network engineering technologies, as well as to modern achievements in the field of control and communication system development. The aim of the conference was to provide an international forum for discussion of recent scientific advances in the electronic industry. Complementing the technical program, many special keynote lectures were featured at the workshop.

From 296 submissions, 150 papers were selected for presentation and publication in the conference proceedings. A small army of student volunteers handled an incredible number of details both before and during the workshop. We acknowledge the extraordinary work that was done by the Program Committee in providing reviews, on the basis of which an excellent technical program was finalized. The seminar was co-sponsored by ED-S, MIEM HSE, Russian Foundation for Basic Research, and National Instruments Rus R&D. More information on this event is available at https://mwent.hse.ru/en/ website.

The beautiful city of Moscow, the capital of Russia, is especially known for its cultural background with numerous theaters, museums, historical buildings, concert halls, plenty of restaurants and other places of amusement. We cordially invite you to visit us in a near future.

MTT/ED/AP/EP/SSC West Ukraine Chapter

—by Mykhaylo Andriychuk

The Chapter has been selected as the 2017 recipient of the IEEE Electron Devices Society Region 8 Chapter of the Year Award. This award was intended to recognize the quality and quantity of the Chapter activities and programs implemented by the Region 8 chapters during the prior July 1st–June 30th period. The main Chapter activities during this period were focused on increasing IEEE membership, organizing distinguished lectures and technical meetings, as well as providing the technical and financial co-sponsorship

Dr. Olha Zamorska, Chapter Secretary/Treasurer, and Dr. Mykhaylo Andriychuk, Chapter Chairman, presenting the 2017 IEEE Electron Devices Society Region 8 Chapter of the Year Award Plaque

for the International Scientific conferences held in Ukraine in 2017.

The Chapter membership was increased from 27 members in 2016 up to 35 members in 2017. This was realized by applying the 2017 EDS and other IEEE Society's Membership Fee Subsidies, active participation in the IEEE Member-Get-a-Member program, and financial support of regular and student membership from the Chapter budget. The chapter hosted two IEEE Distinguished Lecturers in 2017. In addition, twelve technical meetings in the area of EDS scientific fields were organized by the Chapter.

The main part of Chapter activity was organizing and sponsorship of the International Scientific Conferences. As a result, nine Conferences had received different kind of support from the Chapter during reporting period. The most successful and important of them were the following: CADSM-2017 (http://cadsm.lp.edu.ua), UKRCON-2017 (http://ukrcon.ieee.org.ua), and DIPED-2017 (http://www.ewh.ieee.org/soc/cpmt/ukraine/).

The Chapter administrative meeting dedicated to presentation of the Chapter of the Year Award was held on February 6, 2018. Dr. Mykhaylo Andriychuk, Chapter Chairman, acquainted the Chapter members and invited guests with the conducted Chapter activity and congratulation letter from the ED Society. The problems regarding improvements of the future Chapter activities were also discussed.

~ Daniel Tomaszewski, Editor

ED Scotland

—by Gerard Cummins

The Scottish Chapter of the Electron Devices Society is proud to report that two of our members have been

Newly named Fellows of the Royal Society of Edinburgh, Professors Robert Henderson (left) and Marc Desmulliez

awarded Fellowship in the Royal Society of Edinburgh (RSE). Professor Robert Henderson of the University of Edinburgh and our current Chapter Chair, Professor Marc Desmulliez of Heriot-Watt University were named among the sixty-six Fellows newly welcomed to Scotland's National Academy. They join an existing roll of around 1,600 Fellows who help the RSE to continue to provide independent and expert advice to policymakers, support aspiring entrepreneurs, develop research capacity and leadership, inspire and facilitate learning and engage with the general public through inspiring events. The new Fellows also included former UK Prime Minister Gordon Brown, Professor Ying-Cheng Lai Chair of Electrical Engineering at Arizona State University, and Ian Stuart Callum Director of Design at Jaguar Cars.

Commenting on the new Fellows, current President of the RSE, Professor Dame Jocelyn Bell Burnell, said, "Each year we welcome a selection of nominated extraordinary individuals into the Fellowship and this year is no exception. The diverse range of achievements of these individuals will be an asset to the RSE and I am sure they will strengthen the RSE's standing as a National Academy committed to providing public benefit to Scottish society."

~ Jon Terry, Editor

Modeling of Systems and Parameter Extraction Working Group Spring'18 MOS-AK Workshop, Munich, March 13, 2018

—by Wladek Grabinski

The MOS-AK Compact Modeling Association, a global compact/SPICE modeling and Verilog-A standardization forum, held its Spring compact/SPICE workshop in Munich. The event was hosted on March 13, 2018, by Infineon Technologies AG in Neubiberg. The technical program of the event was coordination by Klaus-Willi Pieper, Infineon, and the MOS-AK TPC Committee. The workshop has received full industrial sponsorship by Infineon Technologies AG (lead sponsor) with technical program promotion provided by ASCENT Network, Keysight Technologies, IJHSES as well as NEEDS of nanoHUB.org

The MOS-AK workshop was opened by Klaus-Willi Pieper, Principal Compact Modeling Smart Power Devices at Infineon, who has welcomed all the attendees and shared Infineon view on the compact modeling and its importance in the TCAD/EDA modeling/design ecosystem.

A group of 40+ international academic researchers and modeling engineers attended 10 technical compact modeling presentations covering full development chain from the nanoscaled technologies thru semiconductor devices modeling to advanced IC design support. The MOS-AK speakers have shared their latest perspectives on compact/SPICE modeling and Verilog-A standardization in the dynamically evolving semiconductor industry and academic R&D. The event featured advanced technical presentations covering compact model development, implementation, deployment and standardization covering full engineering R&D chain: TCAD/processing, device modeling, transistor level IC design support.

These contributions were delivered by leading academic and industrial experts, including: [1] Klaus-Willi Pieper, Overview of the Compact Modeling at Infineon; [2] James Ma et al, Advanced Fast on-wafer Low-frequency Noise Measurement with High Resolution, Wide Bandwidth and Large Biasing Current Range; [3] Volker Gloeckel, Advances in Statistical Compact Modeling; [4] Markus Becherer, et al, Compact Modeling of Nanomagnetic Logic Devices and Circuits; [5] Gražvydas Žiemys, Devices for Nanomagnetic Logic; [6] Paul Roseingrave, Modelling Emerging Devices through EU ASCENT Network; [7] Jushan Xie, How Is CMC Standard Model Implemented and Verified In Simulator?; [8] Maria Cotorogea et al., Virtual Prototyping for Power Diode and IGBT Development; [9] Franz Sischka, et al., Modeling of Device Aging—Example: Diode; [10] Katja Puschkarsky, Device Aging Simulations Enabling Circuit Optimizations; [11] Fabio A. Velarde Gonzalez, Integration of Aging Models Across Different EDA Environments A case study implementing HCI and NBTI models for X-FAB XU035 CMOS technology; During complementary MOS-AK Panel Discussion on Compact Model Licensing Peter Lee, CMC Chair highlighted current status of the CMC compact model licensing status, stating that final discussions are converging to establish official licensing in the next few months. All the presentations are available online for download at http://www.mos-ak.org/munich_2018/.

The participants of the MOS-AK compact/SPICE modeling workshop at Infineon in Munich on March 13, 2018

EUROSOI-ULIS 2018

Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon.

The EUROSOI-ULIS 2018 conference was held on March 19–21, 2018, at Abba Granada Hotel, Granada, Spain. The conference was organized with support of Faculta de Ciencias of Universidad de Granada, CITIC-UGA, SiNANO Institute, IEEE EDS, European Commission Horizon 2020, and many more.

The welcome and opening speech was delivered by Francisco Gamiz, chairman of the conference.

Invited talks were presented by Dr. Byungil Kwak "DRAM Peripheral Transistor Scaling using logic technologies—Future Challenges" (SK Hynix, Republic of Korea), Prof. Adrian Ionescu "Millivolt technology for low power digital and sensing applications (EPFL, Switzerland), Prof. Edward Yi Chang "High performance GaN HEMT for Power Applications" (NCTU, Taiwan), Prof. Hiroshi Iwai "3D scaling of Si-IGBT" (Tokio Institute of Technology, Japan), Prof. Enrique Calleja "MBE growth of ordered InGaN/GaN nano/microrods: basics and applications" (Polytechnical University of Madrid, Spain), Prof. Jesús del Alamo "III-V CMOS: Quo vadis?" (Massachusetts Institute of Technology, USA).

The conference proceedings contained a total of 59 papers which covered the topics:

- Advanced SOI materials and wafers. Physical mechanisms and innovative SOI-like devices
- New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator; carbon nanotubes; graphene and other two-dimensional materials.
- Properties of ultra-thin films and buried oxides, defects, interface quality. Thin gate dielectrics: high-k materials for switches and memory.
- Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, low standby power, high frequency and memory applications.
- Alternative transistor architectures including FDSOI, DGSOI, FinFET, MuGFET, vertical MOSFET, Nanowires, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.
- New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain, nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.
- CMOS scaling perspectives; device/circuit level performance evaluation; switches and memory scaling. Three-dimensional integration of devices and circuits, heterogeneous integration.
- Transport phenomena, compact modeling, device simulation, front- and back-end process simulation.
- Advanced test structures and characterization techniques, parameter extraction, reliability and variability assessment techniques for new materials and novel devices.
- Emerging memory devices.

More information about EUROSOI-ULIS 2018 can be found at https://congresos.ugr.es/eurosoi-ulis2018/.

~ Mike Schwarz, Editor

Asia & Pacific (Region 10)

Annual meeting of the EDS Japan Joint Chapter

—by Masaaki Niwa and Takahiro Shinada

On February 2, 2018, the annual meeting of the EDS Japan Joint Chapter was held at Tokyo campus of the Univ. of Tsukuba. Prof. Masaaki Niwa, Japan Chapter Chair and Dr. Akira Nishiyama, Vice Chair, reported on 2017 activities and 2018 plans of the Chapter. At the meeting, the 2017 EDS Japan Chapter Student Award (VLSI & IEDM) was presented to 6 students, who made excellent presentations at the VLSI Symposia 2017 and IEDM 2017. The award winners are posted on the Japan Chapter's webpage; (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

After the annual meeting, the IEDM 2017 Report Session was held. Nine Japanese members of the IEDM program committee reported on summary, topics and research

The annual meeting of EDS Japan Joint Chapter attendees on February 2, 2018, Tokyo

16th EDS Japan Chapter Student Award winners, together with Prof. Masaaki Niwa; Chair, and Dr. Akira Nishiyama; Vice Chair on February 2, 2018, Tokyo

The executive committee meeting the EDS Japan Joint Chapter on Feb. 2, 2018, Tokyo

trends of their sub-committees for more than fifty attendees. The session provided a good opportunity for the attendees to touch the latest technology trends, especially for those who were unable to attend the IEDM.

The executive committee meeting of the EDS Japan chapter was also held on the same day and the plans for 2018 of the Chapter were approved. The EDS Japan Chapter Executives: Prof. Masaaki Niwa; Chair, Dr. Akira Nishiyama; Vice Chair, Prof. Takahiro Shinada; Secretary, and Dr. Shigeru Kawanaka; Treasurer, invited the 6 guest speakers of the IEDM Report Session, Prof. Hiroshi Iwai, Past President of IEEE EDS, Dr. Toru Mogami, Former Chair, Prof. Toshiro Hiramoto, next Vice Chair and people concerned.

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter hosted the 17th annual Kansai Colloquium Electron Devices Workshop on January 29, 2018, at Umeda Campus of Ryukoku University, Osaka, Japan. The Workshop program committee members carefully reviewed papers published in the past 12 months from various prestige conferences and technical magazines such as IEDM or SSDM as well as IEEE transactions to select excellent 8 papers from authors from Kansai area. The program was divided into three sections: (1) Sensor, Solar Cell, and Emerging Devices, (2) Power and Compound Semiconductor Devices, and (3) CMOS Process, Device, and Circuit.

The Committee selected one paper for the IEEE EDS Kansai Chapter of the Year Award. The winning paper was "High-speed switching and current-collapse-free operation by GaN gate injection transistors with thick GaN buffer on bulk GaN substrates" by Dr. Hiroyuki Handa of Panasonic.

The presented papers were all excellent and stimulated many questions and discussions with the audience, as they were selected from already qualified papers of major conferences and technical journals. This workshop is playing an important role in encouraging students and young engineers in the industry to extend their technical knowledge and career.

~ Kuniyuki Kakushima, Editor

Award Winner with Chapter Chair

Participants Group Photo

EDS Distinguished Lecture—ED Beijing Chapter

—by Kangwei Zhang

On October 30, 2017, Prof. Ci-Ling Pan from National Tsing Hua University visited the ED Beijing Chapter. He delivered a Distinguished Lecture entitled "Nanostructured Indium Tin Oxides and other Transparent Conducting Oxides: Characteristics and Applications in the THz Frequency Range" hosted by Prof. Ling Li. More than 30 local professionals and graduate students attended the meeting.

Recently, biomimic nanomaterials have been shown to exhibit exotic optical properties, e.g., broadband, omni-directional antireflective properties. Indeed, nanostructured ITO was found to exhibit the above desirable characteristics. In this talk, Prof. Pan described the basics of THz science and technology, fabrication and characterization of several TCOs, including ITO nanomaterials, and several types of bulk TCO thin films, e.g., AZO and AYZO. Performance of THz phase shifters with ITO nanomaterials as transparent electrodes and liquid crystals for functionalities were presented.

The ED Beijing Chapter held one invited talk on November 17, 2017, by Prof. Lorenzo Faraone from the University of Western Australia. He gave a talk titled, "Optical MEMS Technologies for Infrared Spectroscopy." Professor Faraone first introduced the natural landscape and local customs in Western Australia. After that he made an introduction about the University of Western Australia and his research direction, which focused on the infrared spectroscopy technology application in national defense security, biomedicine, food safety, etc. Afterwards, he made a detailed explanation of the structure design, working principle, remote sensing and imaging of the optical Microelectromechanical Systems (MEMS) in the infrared spectrum technology. In addition, he also introduced the future direction of this field and the difficulties which need to be solved. At the end of the seminar, he had made a detailed answer to the questions raised by the audience. Furthermore, he also put forward lots of valuable suggestions for the future scientific research work for graduate students.

A DL talk on December 18, 2017 was presented by Prof. David Z. Pan from The University of Texas at Austin. He gave a talk titled, "Design for X(DFx) in Extreme Scaling and Emerging Technologies." In this talk, he first presented some key challenges and practices for how to enable such DTCO, from mask synthesis, to standard cell and physical design, including design-intent aware layout decomposition under multiple patterning lithography (MPL), machine learning based lithography hotspot detection and mask/physical synthesis, standard cell and routing optimizations, MPL aware placement, etc. As new process technologies are being proposed (e.g., new transistor structures, new materials) and new design requirements (e.g., reliability and security) are emerging, he introduced many new opportunities for synergistic DFx. The talk also covered some DFx needs for emerging technologies such as nanophotonic integration and emerging applications such as FPGA.

Prof. Ci-Ling Pan (5th from the front left) pictured with audiences after the talk

Prof. Lorenzo Faraone presenting

Prof. David Z. Pan (4th from the second left) pictured with audiences after the talk

EDS Distinguished Lecture—EDS Tsinghua University Student Branch Chapter

—by Yancong Qiao

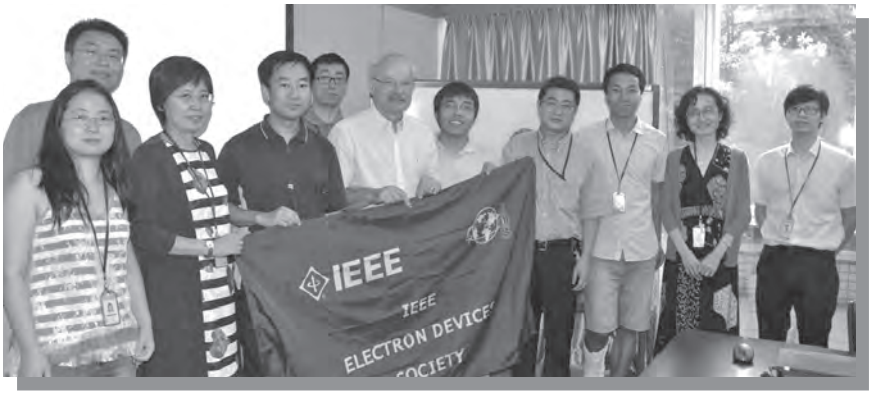
The EDS Tsinghua university student branch chapter held an invited DL talk on November 16th, by Prof. Jong-Hyun Ahn, from the Yonsei University. He gave a talk titled, "2D Materials for Flexible and Wearable Electronics." With the emergence of unusual format electronics such as flexible and wearable devices, an effort has been made to integrate devices with various functions in smart clothing and human body for providing enhanced convenience for the users. However, it is difficult to accomplish such electronics with conventional rigid electronic materials. 2D materials such as graphene and MoS_2, the thinnest elastic material, has superb electronic properties that make it a promising host for device applications and it has a good mechanical property, offering a great opportunity to flexible and wearable electronics that should maintain a stable operation under high strain. In this talk, he presented the research results of his group on fabrication methods of 2D materials and various wearable electronic applications including a touch panel, a tactile sensor and photodetector.

EDS Distinguished Lecture—ED Peking University Student Chapter

—by Zhe Zhang

On Thursday Dec. 21, 2017, Prof. David Z. Pan of University of Texas at Austin visited our chapter and delivered a talk on "Design for Security of Hardware IP and Supply Chain Protection". In this talk, he first gave a brief introduction to security concern of globalized supply chain. Then some proposed solutions were demonstrated to tackle possible attacks, such as hardware Trojans, reverse engineering, and non-invasive attacks. There were about 40 attendees at the lecture. After the talk, Prof. Pan had a discussion with the students and shared his research experience.

On Friday Dec. 7, 2017, Prof. Juin J. Liou from Zhengzhou University was invited to deliver a lecture entitled "On-Chip Spiral Inductor Design and Modeling for RF Applications". First, he gave an overview on the background and concept of Si-based on-chip spiral inductors, then he presented advanced inductor structures for improved RF performance and modeling for accurately predicting the S-parameters. There were about 30 attendees at the talk. After the talk, Prof. Liou had a discussion with our members and some other students.



Dr. Simon Deleonibus (4th from the front left) and Prof. Mansun Chan (3rd from the front left) pictured with some members of the ED Guangzhou Chapter

EDS Distinguished Lecture—ED Guangzhou Chapter

—by Zhangang Zhang

ED Guangzhou Chapter held a mini-workshop on August 3, 2017, at China CEPREI Lab. Two IEEE EDS Distinguished Lecturers, Dr. Simon Deleonibus (CEA-LETI) and Prof.

Prof. Juin J. Liou (5th from the front left) pictured with Prof. Ming Li (4th from the front left), and some other members of the Chapter after the talk

Students and researchers from SCUT, South China Normal University, Jinan University, and University of CAS et al. attended this event and enjoyed the discussion with the lecturers at the ED Guangzhou Chapter MQ

Mansun Chan (HKUST), were invited to present lectures entitled "The Energy and Variability Efficient Era (E.V.E.) is ahead of us" and "Microelectrode Array for Communication between Silicon Chips and Living Cells", respectively. This workshop was co-sponsored by South China University of Technology.

In the lectures, Dr. Deleonibus presented that the electronic market will be able to face an exponential growth thanks to the availability and feasibility of autonomous and mobile systems necessary to societal needs. The increasing complexity of high volume fabricated systems will be possible if we aim at zero intrinsic variability, and generalize 3-dimensional integration of hybrid, heterogeneous technologies at the device, functional and system levels. Weighing on the world energy saving balance will be possible and realistic by maximizing the energy efficiency of co integrated Low Power and High Performance Logic and Memory devices. The future of Nanoelectronics will face the major concerns of being Energy and Variability Efficient (E.V.E.).

Prof. Chan described the development of a biological analysis system based on a standard integrated circuit (IC) fabrication process. Unlike conventional electronic system, bio-based ICs (or biochips) have to handle living cells in an environment that is uncommon in conventional IC technology. In addition, incompatibility between biological processing and electronic signal transduction methodologies requires special considerations to strike for detection protocols that are acceptable for both systems. The work utilizes a CMOS compatible process to fabricate biochip to detect various biological activities from bio-molecules detection (e.g. DNA and protein) to interaction between various active cells. Academics, engineers, and students from institutions of Southern China area attended this event and enjoyed the discussion with the two DLs.

EDS Mini-Colloquia Program—ED Guangzhou Chapter

—by Zhangang Zhang

The 2017 Summer Institute of IEEE Electron Device Society (Guangzhou) was held on August 2–3, 2017. This event was sponsored by South China University of Technology (SCUT), Hong Kong University of Science and Technology (HKUST), and IEEE EDS Guangzhou Chapter. Dr. Simon Deleonibus from CEA-LETI, Prof. Mansun Chan from HKUST, Prof. Waitung Ng from Toronto University, Prof. Hong Guo from McGill University, and Dr. Yang Chai from HKPU were invited to give lectures on the latest research progress in microelectronic area, and also fundamental knowledge. Students and researchers from SCUT, South China Normal University, Jinan University, and University of CAS et al. attended this event and enjoyed the discussion with the lecturers.

EDS Distinguished Lecture—ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU student chapter held three invited talks in the fourth quarter of 2017. The first event was given on October 13, in which Prof. G. C. Liang, National University of Singapore, was invited to give a talk entitled, "Introduction to Non-volatile Electronic System Based SOT Engineering," In this talk, he started with the introduction on the fundamentals of spintronics and followed by three topics covering logic, memory and oscillators. On the subject of nanomagnetic logic device, he presented a Spin Hall Effect (SHE) based asynchronous NML device, in which he proposed majority gate design that can be used as a building block to realize several other NML devices/architectures. On the STT oscillator, he demonstrated a new scheme of Spin-Transfer Torque (STT) oscillators wherein a superior full-switching based design is posited in contrast to extant precessional-orbit based schemes. For memory applications, he presented a three-terminal perpendicular magnetic tunnel junction (pMTJ) that uses voltage-controlled magnetic anisotropy (VCMA) in achieving ultra-fast switching with low energy consumption and WER, which are highly desirable for memory application. This talk was attended by around 120 graduate students, professors, and several engineers from the Science park.

ED Taipei invited talk: October 13-The speaker (Prof. G. C. Liang, 7th from the right) with audience

Another two talks were given on October 19 with two experts on the reliability and resistance memory invited: (1) Beyond Weibull and Poisson Statistical Models: Time-dependent clustering model for dielectric breakdown and RRAM Applications (speaker: Ernest Wu, IBM), (2) Filamentary Analog RRAM for Neuromorphic Computing (speaker: Bin Gao, Tsinghua University). This talk was attended by around 30 graduate students and professors.

One major event is a premier event on VLSI in the region as well as a leading technology conference worldwide for over 30 years, 2018 VLSI-TSA and VLSI-DAT, April 16–19, 2018, http://expo.itri.org.tw/2018vlsitsa. Both are mainly technically sponsored by the IEEE EDS and SSCS, which will hopefully attract more than 800 attendees each year. The paper submission has passed, while online registration is encouraged. Further information and inquiries, please contact Miss Evelyn Chou, vlsitsa@itri.org.tw

EDS Distinguished Lecture—ED/SSC Beijing Section Shenzhen Chapter

—by Qian Li

The ED/SSC Beijing Section Shenzhen Chapter held one invited talk on February 28, 2018, by Prof. Jan Rabaey from University of California, Berkeley. He gave a talk entitled, "Brain-Like Cognitive Engineering Systems." In this talk, he presented his latest research on brain-inspired computing. Prof. Rabaey's talk spanned a wide range of topics from brain-like computing algorithms, hardware acceleration, to system integration. Combined with a variety of emerging computing techniques, such as approximate computing, in-memory computing, as well as 3D integration, Prof. Rabaey enlightened the audience with a promising path towards brain-like computing. This talk was organized by Prof. Hailong Jiao, attended by Prof. Shengdong Zhang, Prof. Yuexian Zou, Prof. Xiaole Cui, Prof. Qian Li, Prof. Xiaojin Zhao, Prof. Hao Yu, Prof. Bo Wang, Prof. Xianfeng Li, Prof. Xian Tang, Prof. Chenchang Zhan, and more around 50 graduate students.

ED Shenzhen invited talk: February 28, 2018-(Middle) Prof. Jan Rabaey (speaker), organized Prof. Hailong Jiao, attended by Prof. Shengdong Zhang, Prof. Yuexian Zou, Prof. Xiaole Cui, Prof. Qian Li, Prof. Xiaojin Zhao, Prof. Hao Yu, Prof. Bo Wang, Prof. Xianfeng Li, Prof. Xian Tang, Prof. Chen-Chang Zhan, and graduate students

EDS Distinguished Lecture—EDS Tsinghua University Student Branch Chapter

—by Yancong Qiao

The EDS Tsinghua University Student Branch Chapter held an invited DL on March 23, 2018, by Dr. Songbin Gong, from the School of Electrical and Computer Engineering, Purdue University, USA. He gave a talk titled, "Radio frequency Microsystems for IoT inspired Front-end Signal Processing."

Recently, IoT has sparked great research interest in developing the next generation frontend that can meet the more stringent requirements on performance, bandwidth, power consumption, and spectral utilization efficiency. This talk discussed several new types of RF micro-systems that can enable conventional signal

ED Tsinghua University Student Branch Chapter invited talk: March 23th-The speaker (Dr. Songbin Gong) with audience

processing functions (e.g. filtering and impedance transformation), or new ones (e.g. RF correlation and non-reciprocity) for IoT applications. Specifically, the most recent development on MEMS resonators, transformers, chirp compressors, gyrators, and circulators was first presented and followed by a discussion on overcoming the remaining technology bottlenecks in their paths to commercialization.

~ Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by Aliza Aini Md Ralib, Norhayati Soin, Noorjannah Ibrahim & Afishah Alias

Technical Talk by Prof Klas Hjort

A technical talk was organized on January 8, 2018, by IEEE ED Malaysia Chapter and Centre of Printable Electronic (CPE) headed by Prof. Norhayati Soin at Faculty of Engineering, University Malaya. The Invited speaker was Prof. Klas Hjort from Division of Microsystems Technology, Department of Engineering, Uppsala University, Sweden. Prof Klas presented on research in Advanced Micro Engineering at Uppsala University during his talk titled "Flexible and printed electronics for MEMS/NEMS sensors/actuators" and "Towards Graphene-Based Printed Electronics" for wearable biomedical sensors. The talk was attended by 15 participants inclusive of staff and students from Faculty of Engineering, University Malaya.

Annual General Meeting 2018

The 28th Annual General Meeting (AGM) of the ED Malaysia Chapter was held on January 27, 2018 at Hotel Le Meridien Putrajaya. The AGM was held to table ED events and financial activities in 2017 and was attended by 31 EDS members from all over Malaysia. New executive committees were elected and Prof. P.Susthitha Menon from IMEN, UKM was elected to lead ED Malaysia Chapter for 2018. During the AGM, the inaugural Outstanding IEEE ED Malaysia Volunteer Award was presented to Prof. Norhayati Soin from Universiti Malaya, while the Outstanding IEEE ED Malaysia Student Volunteer Award was presented to Mohd Nuriman Nawi from IMEN, UKM. All Excom members of 2017 were presented with appreciation certificates. The list of the new Excom members have been updated in the EDS website at http://ieeemalaysia-eds.org/

ED Malaysia wins Outstanding Chapter Award 2017 from IEEE Malaysia Section

ED Malaysia won the IEEE Malaysia Section's Outstanding Chapter Award 2017 during the Appreciation Dinner held at Everly Hotel Putrajaya on January 27, 2018. The purpose of

Participants of the talk by Prof Klas Hjort at CPE, Universiti Malaya

Attendees of the 28th AGM of ED Malaysia Chapter

Winners of the ED Malaysia Outstanding Volunteer and Student Volunteer Award 2017

ED Malaysia receiving the Outstanding Chapter Award 2017 from IEEE Malaysia Section

ED Malaysia and ED Indonesia during the collaborative visit

the award is to recognize the outstanding performance of the best chapter among 27 technical chapters in Malaysia Section, which have successfully served their members and the technical community by voluntary service while retaining membership. Congratulations to ED Malaysia Chapter volunteers!

ED Malaysia and ED Indonesia Collaborative Visit

On February 2, 2018, Prof. Burhanudin Yeop and Prof. Nizar Hamidon represented the ED Malaysia Chapter on a collaborative visit to ED Indonesia at Institute Technology Bandung (ITB), Indonesia. They had a very interactive meeting with Prof Basuki Alam's team discussing future collaboration between both chapters followed by lab visits and lunch.

IEEE International Conference on Semiconductor Electronics (ICSE) 2018

The ED Malaysia chapter is pleased to invite you to the 2018 IEEE International

ICSE 2018 IEEE International Conference on Semiconductor Electronics (ICSE)

Conference on Semiconductor Electronics (ICSE) to be held at the Pullman Kuala Lumpur City Centre Hotel from August 15–17, 2018. This bi-annual technical conference since 1997 aims at bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. This is the 13th ICSE organized by the Electron Devices Chapter of IEEE Malaysia Section and financially co-sponsored by IEEE Malaysia Section. Over the last eighteen years, ICSE conference series has become the prominent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuit device, modeling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, material and devices and nanoelectronics. Please visit our website for further details at http://ieeemalaysia-eds.org/icse2018/.

~ P. Susthitha Menon, Editor

IEEE Journal of the Electron Devices Society

The IEEE Journal of the Electron Devices Society (J-EDS) is a peer-reviewed, open-access, fully electronic scientific journal publishing papers ranging from applied to fundamental research that are scientifically rigorous and relevant to electron devices.

Please submit your manuscripts for consideration of publication in J-EDS at http://mc.manuscriptcentral.com/jeds.

The J-EDS publishes original and significant contributions relating to the theory, modelling, design, performance, and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nano-devices, optoelectronics, photovoltaics, power IC's, and micro-sensors. Tutorial and review papers on these subjects are also published.

As an open-access title, J-EDS provides the electron devices community:

- Faster speed of publication
- Free access to readers globally
- World-wide audience
- Increased dissemination
- High impact factor (IF)
- Articles can be cited sooner
- Articles potentially cited more frequently

Electron Devices Society®

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2018 25th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD) Abstract submission deadline: 22 Mar 2018 Full Paper Submission deadline: 22 Mar 2018 Final submission deadline: 06 Jun 2018 Notification of acceptance date: 25 May 2018	03 Jul - 06 Jul 2018	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo Minami-ku Kyoto, Japan
2018 31st International Vacuum Nanoelectronics Conference (IVNC) Abstract submission deadline: 26 Feb 2018 Final submission deadline: 24 May 2018 Notification of acceptance date: 09 Apr 2018	09 Jul - 13 Jul 2018	Kyoto Research Park 134 Chudoji Minami-machi Shimogkyo-ku Kyoto, Japan
2018 International Flexible Electronics Technology Conference (IFETC) Abstract submission deadline: 31 Jan 2018 Full Paper Submission deadline: 07 Feb 2018 Final submission deadline: 15 May 2018 Notification of acceptance date: 31 Mar 2018	07 Aug - 09 Aug 2018	Delta Hotels Ottawa City Centre 101 Lyon St N Ottawa, ON, Canada
ESSDERC 2018 - 48th European Solid-State Device Research Conference (ESSDERC) Abstract submission deadline: 03 Apr 2018 Full Paper Submission deadline: 04 Apr 2018 Final submission deadline: 01 Jun 2018 Notification of acceptance date: 18 May 2018	03 Sep - 06 Sep 2018	Technische Universität Dresden Dresden, Germany
2018 e-Manufacturing & Design Collaboration Symposium (eMDC) Call for Papers Deadline: 1 June 2018	07 Sep 2018	Ambassador Hotel No.188 Chung Hwa Road, Sec.2 , Hsin Chu,Taiwan
2018 22nd International Conference on Ion Implantation Technology (IIT) Abstract submission deadline: 18 May 2018 Full Paper Submission deadline: 14 Sep 2018 Final submission deadline: 02 Nov 2018 Notification of acceptance date: 02 Jul 2018	16 Sep - 21 Sep 2018	Congress Centrum Würzburg Kranenkai 34 Würzburg, Germany
2018 13th European Microwave Integrated Circuits Conference (EuMIC) Abstract submission deadline: 12 Feb 2018 Full Paper Submission deadline: 12 Feb 2018	23 Sep - 25 Sep 2018	IFEMA Feria de Madrid Avenida Partenon 5 Madrid, Spain

Final submission deadline: 11 Jun 2018 Notification of acceptance date: 12 Apr 2018		
2018 XXIIIrd International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED) Abstract submission deadline: 10 Jul 2018 Full Paper Submission deadline: 01 Aug 2018 Final submission deadline: 20 Aug 2018 Notification of acceptance date: 15 Aug 2018	24 Sep - 27 Sep 2018	Tbilisi State University 1, Chavchavadze Ave. Tbilisi, Georgia
2018 International Integrated Reliability Workshop (IIRW) Abstract submission deadline: 16 Jul 2018 Full Paper Submission deadline: 13 Sep 2018 Final submission deadline: 07 Oct 2018 Notification of acceptance date: 13 Aug 2018	07 Oct - 11 Oct 2018	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2018 International Semiconductor Conference (CAS) Full Paper Submission deadline: 25 May 2018 Notification of acceptance date: 13 Jul 2018	10 Oct - 12 Oct 2018	Rina Sinaia Hotel 8 Carol I Street Sinaia, Romania
2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) Abstract submission deadline: 11 May 2018 Final submission deadline: 03 Aug 2018 Notification of acceptance date: 22 Jun 2018	14 Oct - 17 Oct 2018	San Diego, CA, USA
2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) Abstract submission deadline: 25 May 2018 Final submission deadline: 31 Aug 2018 Notification of acceptance date: 01 Jul 2018	15 Oct - 18 Oct 2018	Hyatt Regency 1333 Bayshore Highway Burlingame, CA, USA
2018 Non-Volatile Memory Technology Symposium (NVMTS)	22 Oct – 24 Oct 2018	Sendai, Japan
2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA) Abstract submission deadline: 15 Jun 2018 Full Paper Submission deadline: 15 Jun 2018 Final submission deadline: 24 Aug 2018 Notification of acceptance date: 20 Jul 2018	31 Oct - 02 Nov 2018	Georgia Tech Hotel and Conference Center Atlanta, GA, USA
2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	05 Nov - 08 Nov 2018	Hilton San Diego Resort and Spa 1775 East Mission Bay Drive San Diego, CA, USA
2018 IEEE International Electron Devices Meeting (IEDM)	29 Nov - 07 Dec 2018	Hilton San Francisco San Francisco, CA, USA
2018 IEEE 49th Semiconductor Interface Specialists Conference (SISC) Abstract submission deadline: 09 Aug 2016	05 Dec - 08 Dec 2018	Catamaran Resort Hotel 3999 Mission Boulevard San Diego, CA, USA
2018 International Symposium on Semiconductor Manufacturing (ISSM) Call for Papers Deadline: 30 July 2018	10 Dec – 11 Dec 2018	Tokyo, Japan

Dear EDS Member:

The IEEE Electron Devices Society is a vibrant, prolific organization whose members make vital contributions to the global technical community each year. To ensure that our members' work is properly recognized, we encourage you to nominate fellow members for our annual awards. It is in this vein that we would like to draw your attention to the awards listed to the right.

These highly prestigious awards draw nominations from all over the world. Please visit the EDS awards website. You can find important information about eligibility, deadlines and other details. If you need more information or have a question about preparing a nomination, please contact Laura Riello of the EDS Executive Office, l.riello@ieee.org. We strive to maintain a comprehensive set of awards that reflect our member activities. As the field of electron devices evolves, so too must our awards. If you would like to suggest new awards, we would welcome your comments and suggestions.

Sincerely,
Samar Saha
EDS Awards Committee Chair

Visit the EDS Website

Pasqualina M. Sarro
2018 Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

- Robert Bosch Award
- J.J. Ebers Award
- Distinguished Service Award
- Education Award
- Early Career Award
- William R. Cherry Award
- PhD Student Fellowship
- Masters Student Fellowship
- Region 9 Outstanding Student Paper Award
- Chapter of the Year Award

*Although the IEEE Electron Devices Society (EDS) is pleased to invite all individuals and groups in the OFAC embargoed countries to submit nominations for IEEE EDS Awards, the IEEE EDS cannot provide any award monies to members from such countries at this time.

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.