

---

## TABLE OF CONTENTS

<b>1.0 INTRODUCTION .....</b>	<b>1</b>
<b>2.0 SYSTEM LEVEL ESD .....</b>	<b>1</b>
<b>3.0 BEHAVIORAL MODELS .....</b>	<b>3</b>
<b>4.0 METHODOLOGY SUMMARY .....</b>	<b>6</b>
4.1 BASIC CONCEPT .....	6
4.2 IMPLEMENTATION EXAMPLE .....	7
4.3 I-V MEASUREMENT USING TLP TO BUILD BEHAVIORAL MODEL .....	9
4.4 DEFINITION OF FAILURE CRITERIA.....	11
<b>5.0 BUILD BEHAVIORAL MODEL.....</b>	<b>12</b>
5.1 DIODES .....	12
5.2 SNAPBACK PROTECTION .....	13
5.3 OTHER TRIGGERING CONDITIONS .....	16
5.4 FILE FORMAT FOR INFORMATION EXCHANGE .....	17
<b>6.0 IMPLEMENTATION INTO THE DESIGN FLOW .....</b>	<b>20</b>
6.1 VALIDATION .....	21
<b>7.0 SUMMARY .....</b>	<b>23</b>
<b>8.0 OUTLOOK.....</b>	<b>24</b>
<b>9.0 DEFINITION OF TERMS.....</b>	<b>24</b>
<b>10.0 REFERENCES .....</b>	<b>24</b>
<b>Annexes</b>	
Annex A (Informative): Analysis of IBIS – Advantages and Disadvantages .....	27
Annex B (Informative): Example of Exchange File for ESD Protection For SEED .....	31
Annex C (Informative): Validation Case Study: LIN Component Modelling .....	33
Annex D (Informative): Revision History for ESD TR26.0-01 .....	35
<b>Tables</b>	
Table 1: Keywords Proposal to Provide Exchangeable Information to Build Quasi-Static Model .....	18
Table 2: Examples of Shared Information to Build Protection Device Models Using Proposed Keywords .....	19
Table 3: Summary of IBIS Advantages and Disadvantages and an Overview of Proposed Improvements .....	29

---

**Figures**

Figure 1: Problem of the Interactions Between the Various Elements of a System ..... 2

Figure 2: System Level ESD Interactions ..... 3

Figure 3: Single TLP Pulse and its Data Point on I-V Curve ..... 4

Figure 4: Simple Circuit Used to Explain the Effect of a Parasitic Inductance and Capacitance; Transient Simulation for Different Circuit Configurations ..... 5

Figure 5: Hierarchical Modular Modeling Principle to Address SEED Complexity ..... 6

Figure 6: Summary of the Elements Needed to Build IC Model ..... 7

Figure 7: Example of a PCB Showing the Path from the External Connector to the IC ..... 8

Figure 8: Example of the Analysis of a PCB: Schematic and Block Approach of the Net Involved in the ESD Propagation and Simulation Result ..... 9

Figure 9: Circuit Board Layout with a Circuit Schematic Superimposed Showing the Stress Injection Point and the Voltage Simulation at the IC ..... 9

Figure 10: Measurement and Simulation of a Sample 100 ns TLP Pulse using a Time Domain Reflection (TDR) Configuration ..... 10

Figure 11: Piecewise-Linear Description of I-V TLP Measurements ..... 11

Figure 12: Time to Failure Measured, Fitted Equation, and Simulated of a Snapback Protection Device ..... 12

Figure 13: Piecewise Linear Diode Implementation into State-Machine Diagram for VHDL ..... 13

Figure 14: Snapback Device Philosophy - from Analog Measurements to Digital States Machine ..... 14

Figure 15: Modified VHDL AMS Model of the SCR I/V Characteristic from Figure 14 ..... 15

Figure 16: TVS Statement Entity for I,V, and Simulation Result for the Positive Voltage Part of the SC17R in Figure 14 ..... 16

Figure 17: Example of Power Clamp Device Implementation into State-Machine for VHDL-AMS Coding ..... 17

Figure 18: Reconstructed Schematic Obtained from Component Description Between Three Pins ..... 20

Figure 19: Implementation of IC Model from Component Description File into the Design Flow to Achieve System Level Simulation ..... 21

Figure 20: Modular PCBs Which can be Combined for the Validation of Different Simulation Set-ups ..... 22

Figure 21: Parasitic Elements of the Device and Measurement Set-up ..... 23

Figure 22: Information Related to the Inputs and Outputs Provided by IBIS ..... 27

Figure 23: IBIS Compared to 100 ns TLP Measurement of ESD Protection of a Digital Component ..... 28

Figure 24: Schematic Overview of the IC Modeling Showing the New ESD Structures ..... 30

Figure 25: Equivalent Schematic of the LIN Component ..... 33

Figure 26: Schematic of the Whole System to Reproduce TLP Injection ..... 34

Figure 27: Simulation Result Showing the Mismatch ..... 34