EOS/ESD ASSOCIATION, INC. SEMINAR

March 14-15, 2018

SYSTEM ESD PROTECTION DESIGN ADRESSING PCB AND IC ASPECTS

March 16, 2018

MEASUREMENT TECHNIQUES

Fraunhofer Institution for Modular Solid State Technologies EMFT
Hansastr. 27d, 80686 Munich, Germany • Lunch and refreshments provided.

Register Online at www.esda.org/events/calendar/

Be proactive! Get engaged! Learn from industry professionals to experience device protection technologies and limitations.

SYSTEM ESD PROTECTION DESIGN ADDRESSING PCB AND IC ASPECTS

MARCH 14-15, 2018 • 9:00 AM - 6:00 PM

Instructors: Jeffrey Dunnihoo, Pragma Design
Harald Gossner, Intel Corporation

Jeff Dunnhoo

Harald Gossner

An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. The tutorial is a hands-on training course for performing a simulation based optimization of PCB ESD protection design and provides deep understanding of the relevant performance criteria both of TVS diodes and IO circuit. This tutorial presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection, with minimum impact on the system performance. All categories of system failures ranging from 'hard' to 'soft' types are considered to review simulation and tool applications that can be used.

By examining the ESD Industry Council's "SEED" (System Efficient ESD Design) approach as recommended by Industry Council on Target Levels and JEDEC (JEP172), the tutorial will establish the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements and, therefore, a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance.

The method allows to achieve first time right PCB builts and reduces the respin effort for boards and ICs. Based on a TLP characterization of SoC interface circuits and TVS diodes, simulation models for impedance and clamping behavior as well as failure threshold are extracted. These are used to assess design solutions by transient simulations. This is showcased by real world examples.

In addition to SEED simulation "First Time Right" design methodologies, the course will review advanced lab analysis and characterization techniques (and limitations), including current reconstruction scanning, susceptibility scanning, resonance scanning, and embedded ESD detector techologies and tools. With the authors of the comprehensive textbook on the subject "System Level ESD Co-Design", Mr. Dunnihoo and Mr. Gossner will discuss hands-on experience and in-depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD-robust systems that include mobile and automotive applications.

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Instructors: Horst A. Gieser and Heinrich Wolf, Fraunhofer EMFT


Horst A. Gieser


Heinrich Wolf

Advanced ESD Characterization

How to gain accurate insight in the electrical behavior of protection elements and of elements to be protected. The seminar covers the following topics: Accuracy aspects of transmission line testing, characterization and parameter extraction from DC to very fast transmission line pulsing including electro thermal aspects, how to choose the failure criteria (leakage and RF-degradation), how to gain accurate transient device behavior applying repetitive ps-pulsing, high bandwidth system level measurements applying a current sensor.

ESD Failure Reproduction and Alternative Models

How to look at a failure and how to reproduce it. CDM-Pitfalls; Capacitively Coupled TLP; Cable Discharge; Charged Board Model; ESD from Outside - straight through passivation ESD on LEDs.

Lab Experience

Learn to know your structures in the ATIS test lab and discuss the results with the speakers and your colleagues. Learn to know characterization equipment and methods.

Please contact heinrich.wolf@emft.fraunhofer.de to discuss your individual test wishes at least before March 1st, 2018 and send some devices to be tested during a demonstration at the workshop. The speakers reserve the right to prioritize projects in view of interest to the audience.

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ABOUT THE INSTRUCTORS

Jeffrey Dunnihoo is the founder of Pragma Design in Austin, Texas; specializing in interface design architecture and ESD, EOS, and other transient analysis. Pragma's engineering services are based on decades of experience in I/O ASIC and serial bus interface protection and design. Pragma Design's current PESTO online ESD simulation tool implements the Industry Council's system efficient ESD design methodology which is used in Littelfuse's iDesign simulation tool. Jeff has presented at IEEE EMC, ESDA, ISTFA, and has recently co-authored a new textbook with other ESD experts on ESD co-design fundamentals. He has also been a contributor to industry groups and standards bodies such as USB, IEEE 802.11, VESA/DisplayPort, and ESD Industry Council; and has served in EOS/ESD Association, Inc. systems and testing working groups.

Harald Gossner is Senior Principal Engineer at Intel. He received his degree in physics (Dipl. Phys.) from the Ludwig-Maximilians-University, Munich in 1990 and his Ph. D. in electrical engineering from the Universität der Bundeswehr, Munich in 1995. For 15 years he has worked on the development of ESD protection concepts with Siemens and Infineon Technologies. In 2010 he has joined Intel Mobile Communications overseeing the development of robust mobile systems. Harald has authored and co-authored more than 100 technical papers and two books in the field of ESD and device physics. He holds 50 patents on the same topic. He received the best paper award of EOSESD 2005 and 2012. Regularly he is lecturing tutorials at ESREF, IRPS and EOSESD symposium. He has served in technical program committees of IEDM, EOSESD Symposium and International ESD Workshop and is member of the board of directors of ESD Association. In 2006 he became cofounder and co-chair of the Industry Council on ESD Target Levels.

Horst A. Gieser is head of the ATIS (Analysis and Test of Integrated Systems) team at the Fraunhofer-Institution for Modular Solid State Technologies EMFT (the former Munich branch of Fraunhofer-Institute for Reliability and Microintegration until June 30, 2010). He received his diploma in Electrical Engineering and his Ph.D. from the Technical University in Munich. He has authored and contributed to more than 55 publications. Four papers in the field of electrostatic discharge (ESD) won awards at international conferences. Currently, he is chairing the ESD FORUM e.V. www.esdforum.de, the German non-profit ESD association furthering the exchange of scientific and professional experience. He has been serving in organizing several international conferences and workshops. Further interests are in the field of reliability and failure analysis of devices, circuits, and systems as well as characterization techniques with ultra-short transients. For lateral and vertical integration of modules and systems his team has been working on Aerosol Jet Printing, through silicon vias, and polymer electronics.

Heinrich Wolf received his diploma degree in Electrical Engineering from the Technical University of Munich (TUM) and his PhD from the Technical University of Berlin, Germany. He joined the Chair of Integrated Circuits at the TUM as a member of the scientific staff working on Electrostatic Discharge (ESD) related issues. This involved modeling of ESD-protection elements, parameter extraction techniques and test chip design. In 1999 he joined Munich branch of the Fraunhofer Institute for Reliability and Microintegration (IZM) which became the Institution for Solid State Technologies EMFT in 2010. He was involved in the investigation of ESD phenomena for CMOS and Smart Power Technologies. Furthermore he published on the development of ESD test methods and tester characterization. Currently he is coordinating the ESD related activities at the EMFT and is also working in the field of RF transmission line design which includes simulation and characterization up to 110 GHz. Furthermore, he serves for the TPC of the EOS/ESD Symposium and the IEW.

EOS/ESD ASSOCIATION, INC. SEMINAR

March 14-15, 2018 - System ESD Protection Design Addressing PCB and IC Aspects
March 16, 2018 - Measurement Techniques

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Address is (please circle the one that applies) Home or Company

Phone: _____ Fax: _____ E-mail: _____

	Cost
ESD System Level	$1,710
Measurement Techniques	$ 710

Register online at www.esda.org

Discount before Feb. 2nd, 2018: ESD System Level - members $ 1,510 / non-Members $1,610
Measurement Techniques - members $ 510 / non-Members $ 610

Register 5 or more people from one company at the same time and save 10%. Please contact the ESD Association prior to registering.

Cancellation & refund requests will be honored only if received in writing no later than Feb. 2nd, 2018 and are subject to a $50 fee. Any other approved dispositions will also be assessed a $50 fee.

Payment Information

Payment is required at time of registration. Only checks drawn in U.S. currency on a U.S. bank that is a member of the Federal Reserve will be accepted; make checks payable to ESD Association. Visa®, Mastercard®, and American Express® and Discover® are accepted.

Amount enclosed $ _____ ☐ Check ☐ Credit Card

Credit card type: Visa® Mastercard® American Express® Discover®

Credit card number: _____ Expiration date: _____

Name on card: _____ Security code: _____

Cardholder's signature: _____

Accomodations: Be sure to make your reservations early to guarentee room availability.

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