

ESD Open Forum

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Q: We have experienced a significant amount of unexplained "component on board" failures that resemble ESD at times and EOS at other times, but we have not been able to duplicate these failures using any of the existing ESD Models. There is literature that suggests that these are CBM failures. Is the ESDA doing any work to produce a standard method/procedure for the industry?

A: This is a very good and direct question. In an attempt to bring awareness for the need to develop a universal procedure to test for component failures on printed circuits boards (PCBs), the ESDA standards body has had three adhoc meetings to explore the possibilities.

In reviewing existing publications, such as the ESDA white paper [1] and others [2, 3, 4], it is found that only anecdotal evidence existed up to 1983 for ESD failures of Integrated Circuits (ICs) that are mounted on PCBs. These failures had occurred after improperly grounded personnel handled the IC-populated PCBs during the many stages of manufacturing up to and including actual placement in the completed electronic equipment/system. Between 1984 [4] and 1987 [7], it was reported that most components which reportedly failed for the ESD transients on the printed circuit board (PCB), had failed functional testing (that is, the board was inoperable). Failure Analysis (which included SEM analysis) of the ICs removed from the PCB, showed that the physical damage type was dielectric/silicon punch-through.

From 1985 [5], this PCB ESD discharging event was referred to as a Charged Board Model (CBM) ESD event, and CBM ESD testing was initiated. The measured PCB capacitance ($> 125\text{pF}$) was always larger than that (25 pF) for IC devices being built at that time. In 1986, Enoch and Shaw [6], in their study of board-mounted ICs, used the field induced method to charge the board (PCB), then grounded the PCB via one of the input connectors. Koyler et al in 1987 [7] regarded the PCB to be an extended device package, but with higher capacitance. They suggested two modes by which the board-mounted IC can fail: (i) during the insertion of the device into the board, and (ii) when the PCB discharges into the device, an external to internal mechanism. Paasi 2003 [8] found board mounted IC failures after they were charged by transportation on conveyor belts. Olney et al [9] in 2003 used a regular CDM tester to perform the field-induced stress testing of the components on the board.

Conceptually, the Charged Board Model (CBM) is similar to the Charged Device Model (CDM). During a CDM event, the charge stored by a packaged IC discharges (typically $< 100\text{picoseconds}$) just before contact is made with a conductive object at or near ground potential. During a CBM event, the charge stored by an entire PCB discharges ($100\text{s of picoseconds}$) just before contact is made with a conductive object at or near ground potential. Thus, the Charged Board Model can be thought of as an extension of the Charged Device Model where the PCB is the "device" that stores the charge. It is suggested that CBM be renamed CBE (Charged Board Event) because CBE does not actually represent a new model, it is just a more severe CDM event – so severe that the failure can be mistaken for electrical overstress (EOS) damage.

Yes, we need a document that the industry can rely on. The question is: which industries need this? At the WG, we have discussed the PCB industry, the Cell phone industry, the “board stuffing” industry”, the automotive industry, and the medical industry. CBE is not as well known as other ESD models but it represents a major real-world ESD threat. Even if all the individual components used for a given PCB have high device/component-level ESD robustness, one or more of these components could be very susceptible to ESD damage after mounting to a PCB since a PCB in general has much higher capacitance than an individual device [10-16]. CBE damage can be much more severe than CDM damage. Therefore, before attributing an IC failure on a PCB to EOS, the possibility of CBE ESD damage should be explored.

It is true that no industry standard currently exists for CBE testing, but a Technical Report (TR) or Standard Practice (SP) document is being considered by the Device Testing Working Group members. An SP document by definition contains a procedure for performing one or more operations or functions that may or may not yield a test result. However, if a test result is obtained, it is not reproducible. Trying to standardize the CBE stress testing procedure will be very challenging because PCB designs and layouts vary significantly and each PCB may have several tens to hundreds of potential discharge points, and so specifying specific discharge points in a standardized test method (STM) is not easy. However, an SP document, which is just the best practices that are being used, can easily be developed.

References

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