SEARCH and RETRIEVAL INDEX
to
EOS/ESD SYMPOSIUM PROCEEDINGS
1979 to 2017

(A GUIDE TO THE KNOWLEDGE BASE OF THE EOS/ESD SYMPOSIUM PROCEEDINGS)

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INTRODUCTION

The EOS/ESD Symposium annual proceedings are a major source of information on electrostatic discharge. The proceedings also cover electrical overstress in general and, to a lesser extent, EMI. The first symposium was held in 1979 in Denver, Colorado. It was sponsored by ITT Research Institute and managed by a Steering Committee of individuals from industry and government organizations interested in EOS/ESD. The Symposium has been held every year since 1979. In 1983, EOS/ESD Association, Inc. became a cosponsor with IITRI until 1989.

Starting in 1990 the EOS/ESD Symposium became sponsored by the EOS/ESD Association in cooperation with the IEEE Electron Devices Society.

In 1994, ESD Association expanded its area of interest to non-electronic concerns of ESD and started to be known as the EOS/ESD Association, Inc. The symposium started to publish a few papers from other fields.

Paper number references for this index consist of 5 digit numbers. The first two digits are the proceeding’s year where the paper can be found. The last three digits are the proceedings page number on which the paper starts or the assigned paper number.

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There are some workshop reports and summaries at the back of the proceedings. The workshop information was not included in this index.

Starting in 1991 the proceedings was handed out at the Symposium. This is discernible by the paper awards photographs, since the awards for 1989 appear in both the 1990 and 1991 proceedings. So before 1991, to look at award photos for papers given a certain year you looked in the next year’s proceedings. For the awards from 1990 on, you look in the second year’s proceedings after the paper was given.
**AVAILABILITY**

The proceedings are generally available from EOS/ESD Association, Inc. Headquarters. (Some earlier years are no longer available.)

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99043  A Study of ESD Induced Lockups in a Semiconductor Photolithography Area

Barnum, J.R.
81229  Electrical Overstress Damage in Silicon Solar Cells
91026  Sandia’s Severe Human-Body Electrostatic Discharge Tester (SSET)

Barrett, R.
2004141  Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
Barth, J.E.

96167 Charged Device Model (CDM) Metrology: Limitations and Problems
96211 Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics toward Creating a More Repeatable Simulation or;
98029 Metrology and Methodology of System Level ESD Testing
98290 Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
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99203 Issues Concerning CDM ESD Verification Modules-The Need to Move to Alumina

2000072 The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation
2000085 TLP Calibration, Correlation, Standards, and New Techniques
2001453 Correlation Considerations: Real HBM to TLP and HBM Testers
2002155 Correlation Considerations II: Real HBM to HBM testers
2003179 Real HBM & MM - The dv/dt Threat
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2005141 Voltages Before and After Current in HBM Testers and Real HBM
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
2009040 VF-TLP Round Robin Study, Analysis and Results
2009286 Using VFTLP Data to Design for CDM Robustness
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2012060 HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform
2013140 On-Chip System Level ESD Protection for Class G Audio Power Amplifiers
20163B3 HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document?
20164A1 Improving CDM Measurements with Frequency Domain Specifications

Baruah, A.

79126 An Electrothermal Model for Current Filamentation in Second Breakdown of Silicon-on Sapphire Diodes

Batchelder, J.S.

91038 Technique for Generating Contamination-Free Ionized Air Using Focused Laser Light

Batra, J.

20171B3 An ESD Case Study with High Speed Interface in Electronics Manufacturing and its Future Challenge

Batra, V.

20159A2 EOS Characterization Methodology Applied to Disable Feature of ESD Power Clamps

Bauduin, B.

94301 A Comparative Study of "Low Cost" 1.3 µm Laser Diodes: ESD Performance

Baum, K.

91151 Detection of ESD-Induced Non-Catastrophic Damage in P-Channel Power MOSFETs

Baumann, C.

2010049 Triggering of Transient Latch-up (TLU) by System Level ESD

Baumgartner, G.

84025 Electrostatic Measurement for Process Control
84097 Testing of Electrostatic Materials Fed. Std. 101C, Method 4046.1
85124 ESD Analysis of Masking Tape Operations
87018 A Method to Improve Measurements of ESD Dissipative Materials
90097 Electrostatic Discharge Protective Bag Test - Analysis of EIA Standard 541
92009 The Misconceptions of Air Flow as a Tribocharging Source
95262 Electrostatic Decay Measurement Theory and Applications
96156 ESD Demonstrations to Increase Engineering & Manufacturing Awareness
97068 Analysis of ESD Glove Use
98224 EOS Analysis of Soldering Iron Tip Voltage
2001281 A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots
Bayer, M.J.  
2003017  Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies

Baynes, C.C.  
90151  Failure Analysis of Electrostatic Sensitive ECL Gate Arrays

Bazarian, A.  
80044  Gas Tube Surge Arresters for Control of Transient Voltages

Beall, J.R.  
83198  A Study of ESD Latent Defects in Semiconductors

Beamer, B.  
91210  A New Permanent ESD and Corrosion Resistant Material [BPR]

Beaudoin, F.  
2004174  ESD Induced Latent Defects in CMOS ICs and Reliability Impact

Beckrich-Ros, H.  
2008067  A Physics-Based Compact Model for ESD Protection Diodes under Very Fast Transients
2008088  A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology
2010021  A Novel Physical Model for the SCR ESD Protection Device
2011179  Scalable Modeling Studies on the SCR ESD Protection Device
2012015  ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

Beebe, S.G.  
96265  Methodology for Layout Design and Optimization of ESD Protection Transistors
98259  Simulation of Complete CMOS I/O Circuit Response to CDM Stress
2004248  ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure
2005421  SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies
2007185  Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI
2008235  ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2009101  Metal and Silicon Burnout Failures from CDM ESD Testing
2010203  Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Beetner, D.  
20178A1  On-Chip Sensors to Measure Level of Transient Events

Bèges, R.  
20154B1  TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators

Belisle, D.  
2002163  A New ESD Model: The Charged Strip Model

Bell, D.A.  
2010097  Hierarchical Verification of Chip-Level ESD Design Rules

Bellens, R.  
97240  Study of the ESD Behaviour of Different Clamp Configurations in a 0.35 µm CMOS Technology

Bellew, P.  
2000041  Optimizing the Performance of a Composite ESD Circuit Protection Device
2000111  TLP Measurements for Verification of ESD Protection Device Response

Bellmore, D.G.  
2001141  Anodized Aluminum Alloys, Insulator or Not?
2002223  Controlling ESD in Automated Handling Equipment
2004200  CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2004219  Characterizing Automated Handling Equipment Using Discharge Current Measurements
2005195  Characterizing Automated Handling Equipment Using Discharge Current Measurements II
2006240  Trends in External Ionizer Monitoring and Control
Beloni, E.
2010325  ESD Stimulated Ignition of Metal Powders

Beltman, R.A.M.
90157  Simulation of Thermal Runaway during ESD Events
91098  Physics of Electro-Thermal Effects in ESD Protection Devices

Bendix, P.
2000456  Chip-Level Simulation for CDM Failures in Multi-Power ICs
2005100  Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies

Bennett, D.
2003372  Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004141  Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

Benoist, T.
2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration
2012015  ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

Berbeco, G.R.
80001  Passive Static Protection:  Theory and Practice
82124  Characterization of ESD Safe Requirements for Floor Surfaces

Berkowitz, M.B.
89032  Modular ESD Certification Training Program
90027  ESD Controls in Hazardous High Voltage Environments

Berndt, H.
2001267  A Study of the Variables of Electrodes Used in the Measurement of Table and Floor Materials and How They Affect the Test Results

Bernett, M.K.
82115  Electroactive Polymers as Alternate ESD Protective Materials

Bernier, J.C.
94214  CDM Events in Automated Test Handlers and Environmental Testing - A Case History
95110  ESD Improvements for Familiar Automated Handlers
96117  Die Level CDM Testing Duplicates Assembly Operation Failures
97083  ESD Sources Pinpointed by Analysis of Radio Wave Emissions
99168  Test Methodologies for Detecting ESD Events in Automated Processing Equipment
2000097  A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods
2003372  Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2005195  Characterizing Automated Handling Equipment Using Discharge Current Measurements II

Berning, D.W.
79116  Reverse-Bias Second Breakdown in Power Transistors

Berthet, F.
2014393  Electrical Overstress Robustness and Test Method for ICs

Bertonnaud, Stephane
2012388  IEC System Level ESD Challenges and Effective Protection Strategy for USB2 Interface

Bertrand, G.
2002281  Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN
<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Besse, P.</td>
<td>2002</td>
<td>Investigations for a Smart Power and Self-Protected Device under ESD Stress through Geometry and Design Considerations</td>
</tr>
<tr>
<td></td>
<td>2006</td>
<td>Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology</td>
</tr>
<tr>
<td></td>
<td>2010</td>
<td>Correlation between System Level and TLP Tests Applied to Stand-Alone ESD Protections and Commercial Products</td>
</tr>
<tr>
<td></td>
<td>2011</td>
<td>ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver</td>
</tr>
<tr>
<td></td>
<td>2012</td>
<td>Impact of Snapback Behavior on System Level ESD Performance with Single and Double Stack of Bipolar ESD Structures</td>
</tr>
<tr>
<td></td>
<td>2015</td>
<td>TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators</td>
</tr>
<tr>
<td></td>
<td>2017</td>
<td>High-Performance Bi-Directional SCR Developed on a 0.13 um SOI-Based Smart Power Technology for Automotive Applications</td>
</tr>
<tr>
<td>Beyne, E.</td>
<td>2015</td>
<td>ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package</td>
</tr>
<tr>
<td>Bhar, T.N.</td>
<td>7902</td>
<td>Proposed MIL-STD and MIL-HDBK for an Electrostatic Discharge Control Program -- Background and Status --</td>
</tr>
<tr>
<td>Bhat, N.</td>
<td>2017</td>
<td>On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism</td>
</tr>
<tr>
<td>Bhatia, K.</td>
<td>2007</td>
<td>Layout Guidelines for Optimized ESD Protection Diodes</td>
</tr>
<tr>
<td></td>
<td>2007</td>
<td>A Kelvin Transmission Line Pulsing System with Optimized Oscilloscope Ranging</td>
</tr>
<tr>
<td>Bhooshan, R.</td>
<td>2015</td>
<td>A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures</td>
</tr>
<tr>
<td>Biegel, M.G.</td>
<td>9408</td>
<td>Charged Device Damage of PLCCs inside an Antistatic Shipping Tube - A Case History</td>
</tr>
<tr>
<td>Biermann, G.</td>
<td>9314</td>
<td>A Statistical Method for the Detection of Gate Oxide Breakdowns Due To Fast EOS Events, Such As ESD, On Power DIMOS Devices</td>
</tr>
<tr>
<td></td>
<td>9717</td>
<td>Grounding Personnel via the Floor/Footwear System</td>
</tr>
<tr>
<td>Bigaouette, R.J.</td>
<td>9016</td>
<td>Degraded Device Detection</td>
</tr>
<tr>
<td>Billy, S.</td>
<td>2015</td>
<td>A Comprehensive ESD Verification Flow at Transistor Level for Large SoC Designs</td>
</tr>
<tr>
<td>Bilodeau, T.M.</td>
<td>8814</td>
<td>A Novel High Fidelity Technique to View In-Situ ESD Stress Voltage Waveforms</td>
</tr>
<tr>
<td></td>
<td>8904</td>
<td>Theoretical and Empirical Analyses of the Effects of Circuit Parasitics on the Calibration of HBM ESD</td>
</tr>
<tr>
<td></td>
<td>9013</td>
<td>The Electrostatic Discharge Sensitivity of GaAs MMIC Amplifiers</td>
</tr>
<tr>
<td>Bin, L.</td>
<td>9813</td>
<td>Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor</td>
</tr>
<tr>
<td>Bingold, B.</td>
<td>9114</td>
<td>Package Effects on Human Body and Charged Device ESD Tests</td>
</tr>
<tr>
<td>Birk, M.</td>
<td>9702</td>
<td>Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs</td>
</tr>
<tr>
<td>Black, E.P.</td>
<td>9101</td>
<td>Real Circuit Performance of ESD Protection Devices</td>
</tr>
<tr>
<td>Blackburn, D.L.</td>
<td>7911</td>
<td>Reverse-Bias Second Breakdown in Power Transistors</td>
</tr>
</tbody>
</table>
Blanc, D.  
2013105  Power-to-Failure Investigation for PNP-based ESD Protections: From ns to ms

Blanc, F.  
2001110  Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test  
2006077  ESD Protection for the High-Voltage CMOS Technologies  
2007047  Designing HV Active Clamps for HBM Robustness  
2008099  A Methodology for the ESD Test Reduction for Complex Devices

Blankenagel, J.  
89050  A High Voltage Pulse Generator for ESD Simulation

Blankstein, S.  
98124  Outgassing, Volatile Organic Content, and Contamination Content of Materials Used in Today’s Electronics Workplace

Blinde, D.R.  
81009  Quantitative Effects of Relative & Absolute Humidity on ESD Generation/Supression  
83067  The Room Air Ionization System, a Better Alternative than 40% Relative Humidity [BPR]

Blitshteyn, M.  
83076  Measuring Effectiveness of Air Ionizers

Blore, R.A.  
79041  Reliability of EOS Screened Gold Doped 4002 CMOS Devices

Bobde, M.  
2008083  Potential Barrier Based Clamp: A New Device Structure For Low Voltage Triggering

Bock, K.H.  
90193  Improved ESD-Protection of GaAs-FET Microwave Devices by New Metallization Strategy  
92168  Field emitter-Based ESD-Protection Circuits for High Frequency Devices and IC’s [BPP]  
96302  A Compact Model for the Grounded-Gate NMOS Behaviour under CDM ESD Stress  
97001  ESD Issues in Compound Semiconductor High-Frequency Devices and Circuits  
97308  Influence of Well Profile and Gate Length on the ESD Performance of a Fully Silicided 0.25 um CMOS Technology  
98177  Non-Uniform Triggering of gg-nMOST Investigated by Combined Emission Microscopy and Transmission Line Testing  
98290  Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations  
98301  Investigation into Socketed CDM (SDM) Taster Parasitics  
99095  Influence of gate length on ESD-performance for deep sub-micron CMOS technology  
2009135  Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM

Boday, D  
2012120  ESD Protection of MR Sensors Using a Dissipative Shunt

Boehm, D.  
98233  Magneto Optical Static Event Detector  
99168  Test Methodologies for Detecting ESD Events in Automated Processing Equipment  
2000193  Advances in Magneto Optical Static Event Detector Technology

Bogani, A.  
2013164  HBM ESD EDA Check Method Applied to Complete Smart Power IC’s – Functional Initialization and Implementation  
20153A2  Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC’s – Initialization and Implementation  
20173B2  EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC’s

Bolasny, R.E.  
80213  Static Control Systems

Bonfert, D.  
99178  Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bönisch, S.</td>
<td>2001373</td>
<td>Broadband Measurement of ESD Risetimes to Distinguish between Different Discharge Mechanisms</td>
</tr>
<tr>
<td>Bontekoe, F.</td>
<td>90119</td>
<td>Standard ESD Testing of Integrated Circuits</td>
</tr>
<tr>
<td>Bookin, W.</td>
<td>2007138</td>
<td>ESD Damage and Solutions in Tape Head Manufacturing</td>
</tr>
<tr>
<td>Boone, W.</td>
<td>98010</td>
<td>Evaluation of Cleanroom/ESD Garment Fabrics: Test methods and Results</td>
</tr>
<tr>
<td></td>
<td>98328</td>
<td>Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing</td>
</tr>
<tr>
<td></td>
<td>99361</td>
<td>Using HGA Antennas to Measure EMI; Establishing and Correlating Damage Thresholds of GMR Heads</td>
</tr>
<tr>
<td></td>
<td>99373</td>
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</tr>
<tr>
<td></td>
<td>2002326</td>
<td>Impact of Insulating “Conductive” Materials on Disk Drive ESD Robustness</td>
</tr>
<tr>
<td></td>
<td>2004008</td>
<td>Wire Bonding Tip Study for Extremely ESD Sensitive Devices</td>
</tr>
<tr>
<td>Bordeos, R.</td>
<td>2000184</td>
<td>A Case Study on Hidden ESD Events of GMR HGA Dynamic Test Fixture</td>
</tr>
<tr>
<td></td>
<td>2000485</td>
<td>Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach</td>
</tr>
<tr>
<td></td>
<td>2001175</td>
<td>A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)</td>
</tr>
<tr>
<td></td>
<td>2002147</td>
<td>Magnetoresistive Sensitivity Mapping (MSM) and Dynamic Electrical Test (DET) Correlation Study on GMR Sensor Induced by Low</td>
</tr>
<tr>
<td></td>
<td>2002321</td>
<td>The Practical Approach of ESD Control Solution in Headstack Assembly (HSA) Manufacturing</td>
</tr>
<tr>
<td>Bordoloi, B.K.</td>
<td>88113</td>
<td>Characterization of Corrosivity of Antistatic Packaging Materials</td>
</tr>
<tr>
<td>Borgmans, C.</td>
<td>93177</td>
<td>Selecting Materials for Protection against ESD Using an ESD Shielding Effectiveness Meter</td>
</tr>
<tr>
<td>Borjesson, A.</td>
<td>95253</td>
<td>A Method for Measurement of Triboelectric Charging</td>
</tr>
<tr>
<td>Borlongan, M.A.</td>
<td>2007222</td>
<td>Preventing Arcing Damage on Radio Frequency Device Wafer by Controlling ESD Resistively Level of Water for Saw and Wash</td>
</tr>
<tr>
<td>Boroni, A.</td>
<td>20158A3</td>
<td>Practical HBM Testing with Statistical Pin Combinations</td>
</tr>
<tr>
<td>Borremans, J.</td>
<td>2007242</td>
<td>T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology</td>
</tr>
<tr>
<td></td>
<td>2009352</td>
<td>A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS</td>
</tr>
<tr>
<td>Bos, P.</td>
<td>90119</td>
<td>Standard ESD Testing of Integrated Circuits</td>
</tr>
<tr>
<td>Bosch, W.</td>
<td>2013191</td>
<td>Powered System-Level Conductive TLP Probing Method for ESD/EMI Hard Fail and Soft Fail Threshold Evaluation</td>
</tr>
<tr>
<td>Boschke, R.</td>
<td>20151A3</td>
<td>VFTLP Characteristics of ESD Protection Diodes in Advanced Bulk FinFET Technology</td>
</tr>
<tr>
<td></td>
<td>20151A4</td>
<td>ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies</td>
</tr>
<tr>
<td></td>
<td>20161A1</td>
<td>ESD Protection Design in a-IGZO TFT Technologies</td>
</tr>
<tr>
<td></td>
<td>20166A2</td>
<td>VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires</td>
</tr>
<tr>
<td></td>
<td>20176B1</td>
<td>VFTLP Characteristics of ESD Diodes in Bulk Si Gate-all-Around Vertically Stacked Horizontal Nanowire Technology</td>
</tr>
<tr>
<td>Author</td>
<td>Publication Year</td>
<td>Title</td>
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<td>-----------------</td>
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<td>-------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Boselli, G.</td>
<td>199011</td>
<td>Investigations on Double-Diffused MOS (DMOS) transistors under ESD zap conditions</td>
</tr>
<tr>
<td></td>
<td>2001071</td>
<td>Modeling Substrate Diodes under Ultra High ESD Injection Conditions</td>
</tr>
<tr>
<td></td>
<td>2002257</td>
<td>Efficient PnP Characteristics of pMOS Transistors in Sub-0.13 µm ESD Protection Circuits</td>
</tr>
<tr>
<td></td>
<td>2003008</td>
<td>A MOSFET Power Supply Clamp with Feedback Enhanced Triggering for ESD Protection in Advanced CMOS Technologies</td>
</tr>
<tr>
<td></td>
<td>2004132</td>
<td>Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers</td>
</tr>
<tr>
<td></td>
<td>2004146</td>
<td>The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps</td>
</tr>
<tr>
<td></td>
<td>2005043</td>
<td>Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window</td>
</tr>
<tr>
<td></td>
<td>2005298</td>
<td>A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65nm CMOS Technologies</td>
</tr>
<tr>
<td></td>
<td>2010031</td>
<td>The Relevance of Long-Duration TLP Stress on System Level ESD Design</td>
</tr>
<tr>
<td></td>
<td>2010103</td>
<td>An Automated ESD Verification Tool for Analog Design</td>
</tr>
<tr>
<td></td>
<td>2010309</td>
<td>Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies</td>
</tr>
<tr>
<td></td>
<td>2011069</td>
<td>Novel Technologies to Modulate the Holding Voltage in High Voltage ESD Protections</td>
</tr>
<tr>
<td></td>
<td>2012373</td>
<td>A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting</td>
</tr>
<tr>
<td></td>
<td>2013133</td>
<td>Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications</td>
</tr>
<tr>
<td></td>
<td>2013292</td>
<td>The Very Unusual Case of the IEC-Robust IC with Low HBM Performance</td>
</tr>
<tr>
<td></td>
<td>2013383</td>
<td>Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components</td>
</tr>
<tr>
<td></td>
<td>20157A1</td>
<td>Design and Optimization on ESD Self-Protection Schemes for 700V LDMOS in High Voltage Power IC</td>
</tr>
<tr>
<td></td>
<td>20163B2</td>
<td>Case Study of DPI Robustness of a MOS-SCR Structure for Automotive Applications</td>
</tr>
<tr>
<td></td>
<td>20176B3</td>
<td>A Novel, SCR-Based, Distributed Power Supply ESD Network for Advanced CMOS Technologies</td>
</tr>
<tr>
<td>Bossard, P.R.</td>
<td>80017</td>
<td>ESD Damage from Triboelectrically Charged IC Pins</td>
</tr>
<tr>
<td></td>
<td>81057</td>
<td>Evaluation of Integrated Circuit Shipping Tubes [BPP]</td>
</tr>
<tr>
<td></td>
<td>83029</td>
<td>ESD by Static Induction</td>
</tr>
<tr>
<td></td>
<td>84040</td>
<td>A Room Ionization System for Electrostatic Charge and Dust Control</td>
</tr>
<tr>
<td></td>
<td>87214</td>
<td>Room Ionization: Can It Significantly Reduce Particle Contamination?</td>
</tr>
<tr>
<td>Bossche, M.V.</td>
<td>2009158</td>
<td>The Application of Large-Signal Calibration Techniques Yields Unprecedented Insight during TLP and ESD Testing</td>
</tr>
<tr>
<td>Botula, A.</td>
<td>2001326</td>
<td>Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit</td>
</tr>
<tr>
<td>Bouangeune, D.</td>
<td>2012396</td>
<td>Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based</td>
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<tr>
<td>Bouchard, S.</td>
<td>92039</td>
<td>ESD - A Problem beyond the Discrete Component</td>
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<tr>
<td>Boujarra, W.</td>
<td>20153A3</td>
<td>A Comprehensive ESD Verification Flow at Transistor Level for Large SoC Designs</td>
</tr>
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<td>Bourgeat, J.</td>
<td>2009314</td>
<td>Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage</td>
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<td>TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior</td>
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<td>$β$ Matrix Concept for ESD Power Devices, Demonstrators in C45 nm &amp; C32 nm CMOS Technology</td>
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<tr>
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<td>2013199</td>
<td>Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology</td>
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<tr>
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<td>Self-ESD-Protected Transmission Line Broadband in CMOS28nm UTBB-FDSOI</td>
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<tr>
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<td>ESD Protection Structure Enhancement Against Latch-up Issue using TCAD Simulation</td>
</tr>
<tr>
<td>Bouyssou, E.</td>
<td>2011241</td>
<td>Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection</td>
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<td>Coupling of ESD-Generated EMP to Electronics</td>
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<tr>
<td></td>
<td>Simulation of the EMP from ESD</td>
<td></td>
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<td>Bowers, J.S.</td>
<td>A Study of ESD Latent Defects in Semiconductors</td>
<td></td>
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<tr>
<td>Boxleitner, W.</td>
<td>ESD Stress on PCB Mounted ICs Caused by Charged Boards and Personnel</td>
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<tr>
<td></td>
<td>Coaxial Probe to Measure ESD Voltage Waveforms with One Nanosecond Risetimes</td>
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<tr>
<td>Bradford, J.</td>
<td>ESD Packaging: An Environmental Perspective</td>
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<td>Grounding Personnel via the Floor/Footwear System</td>
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<tr>
<td>Branberg, G.A.</td>
<td>Electro-Static Discharge and CMOS Logic</td>
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<td>Brandt, M.T.</td>
<td>A Proposed Test Methodology for Evaluating the ESD Control Characteristics of Floor Materials</td>
<td></td>
</tr>
<tr>
<td>Brankov, A.</td>
<td>Failure Detection With HMM Waveforms</td>
<td></td>
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<tr>
<td>Braude, R.</td>
<td>Setting Up an Effective Corporate ESD Program</td>
<td></td>
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<tr>
<td>Bravaix, A.</td>
<td>Ultra-thin Gate Oxide Reliability in the ESD Time Domain</td>
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<tr>
<td></td>
<td>Reliability Aspects of Gate Oxide under ESD Pulse Stress</td>
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<tr>
<td>Brennan, C.J.</td>
<td>Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors</td>
<td></td>
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<td></td>
<td>Design Automation to Suppress Cable Discharge Event (CDE) Induced Latchup in 90nm CMOS ASICs</td>
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<td></td>
<td>Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90nm CMOS ASICs</td>
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<tr>
<td>Brennan, T.F.</td>
<td>Invisible EOS/ESD Damage: How to find it?</td>
<td></td>
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<td>Brennanv, C.</td>
<td>ESD Design Automation for a 90nm ASIC Design System</td>
<td></td>
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<tr>
<td>Bridgwood, M.A.</td>
<td>Modeling the Effects of Narrow Impulsive Overstress on Capacitive Test Structures</td>
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<tr>
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<td>Breakdown Mechanisms in MOS Capacitors Following Electrical Overstress</td>
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<td></td>
<td>A Comparison of Threshold Damage Processes in Thick Field Oxide Protection Devices Following Square Pulse and Human Body</td>
<td></td>
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<tr>
<td>Briggs Jr., C.</td>
<td>Electrostatic Conductivity Characteristics of Workbench-Top Surface Materials</td>
<td></td>
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<tr>
<td>Brin, R.A.</td>
<td>You've Implemented an ESD Program - What's next?</td>
<td></td>
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<tr>
<td></td>
<td>ESD Program Auditing: The Auditor's Perspective</td>
<td></td>
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<td>Brodbeck, J.</td>
<td>Humidity Effects on Laminated ESD Worksurface Resistance and Charge Dissipation Properties</td>
<td></td>
</tr>
</tbody>
</table>
Brobeck, T.
98290 Characterization and Optimization of a Bipolar ESD – Device by Measurements and Simulations
98301 Investigation into Socketed CDM (SDM) Tester Parasitics
98320 Influence of the Device Package on the Results of CDM Tests – Consequences for Tester Characterization and Test Procedure
2000066 Influence of the Charging Effect on HBM ESD Device Testing
2004067 From the ESD Robustness of Products to the System ESD Robustness
2005178 Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices
2005184 Experience in HBM ESD Testing of High Pin Count Devices
2006136 Relations between System Level ESD and (vf-) TLP
2006144 Cable Discharges into Communication Interfaces
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
2007001 CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress
2008106 Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests
2009419 Characterization and Simulation of Real-World Cable Discharge Events
2010049 Triggering of Transient Latch-up (TLU) by System Level ESD

Brodsky, J.S.
2003098 Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2010031 The Relevance of Long-Duration TLP Stress on System Level ESD Design
2010103 An Automated ESD Verification Tool for Analog Design
2010309 Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies
2011197 Capturing Real World ESD Stress with Event Detector
2013292 The Very Unusual Case of the IEC-Robust IC with Low HBM Performance
2014289 Identification of Two-Probe TLP Contact Resistance Issues and Proposed Solutions

Brooke, L.C.
86188 Design and Test Results for a Robust CMOS VLSI Input Protection Network

Brossier, J.
85100 A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models with Experimental Measurements

Brown, D.
20171B1 EMI Generated EOS in a Wire-Bonder

Bruin, P.
2003051 Transmission Line Pulsed Photo Emission Microscopy as an ESD Troubleshooting Method

Bruines, J.
90143 An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes
93117 Suppression of Soft Failures in a Submicron CMOS Process

Bryant, N.
2012186 Carbon Nanotube Based Thermoplastic Lightning Strike Isolators

Bucha, R.M.
2001262 The Purity, Wetting, and Electrical Properties of Static-Dissipative Surfactant Coatings Versus Inherently-Dissipative Polymer Alloys

Buden, B.N.
83056 Power Failure Modeling of Integrated Circuits

Budenstein, P.P.
79126 An Electrothermal Model for Current Filamentation in Second Breakdown of-Silicon-on Sapphire Diodes
80122 Effect of Junction Spikes and Doping Level on the Second Breakdown Susceptibility of Silicon-On-Sapphire Diodes
Buhler, C.  
2005212  Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Bui, A.  
97346  Unique ESD Failure Mechanisms During Negative to Vcc HBM Tests

Buj, C.  
2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Bulach, S.  
96193  Non-invasive Detection and Characterization of ESD Induced Phenomena in Electronic Systems

Burgess, K.  
2010417  Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing  
2011197  Capturing Real World ESD Stress with Event Detector  
2011379  Two New Unexplained and Unresolved HBM Tester Related Failures

Burke, J.J.  
90010  The Effect of Lightning on the Utility Distribution System

Burnett, E.S.  
82131  ESD & Contamination from Clean Room Garments - Problems and Solutions

Burroughs, J.E.  
82185  Electrostatic Discharge Immunity in Computer Systems

Burton, R  
2016A2  ESD Robust 800V SCR-JFET with p+ Ballast Structure

Büyüktas, K.  
20158A4  A Low-Impedance TLP Measurement System for Power Semiconductor Characterization up to 700V and 400A in the Microsecond Range

Bychikhin, S.  
2002387  Investigation of ESD Protection Elements under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry  
2003116  Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness  
2006274  Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices  
2009358  IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements  
2011059  ESD Robust DeMOS Devices in Advanced CMOS Technologies  
2011147  HBM ESD Robustness of GaN-on-Si Schottky Diodes

Cabayan, H.S.  
79198  Statistical Failure Analysis of Military Systems for High Altitude EMP

Cadjan, M.  
2013367  EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level  
20156A2  A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures  
20156A4  P2P and RMAP - New Software Tool for Quick and Easy Verification of Power Nets

Caignet, F.  
2007304  Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester  
2010127  Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation  
2010137  Impact of the Power Supply on the ESD System Level Robustness  
2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver  
2011343  Investigating the Probability of Susceptibility Failure within ESD System Level Consideration  
2013155  20GHz On-Chip Measurement of ESD Waveform for System Level Analysis  
2014053  Novel 3D Back-to-Back Diodes ESD Protection  
20154B1  TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators  
20167A3  From Quasi-Static to Transient System Level ESD Simulation: Extraction of Turn-on Elements
Caikang, S.
98135 Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Caillard, B.
2003233 STMSCR: A New Multi-Finger SCR-Based Protection Structure against ESD

Calabrese, G.M.
94315 Root Cause Analysis and Packaging Enhancements to Improve Processor ESD Susceptibility

Calcaterra, M.C.
79147 Microwave Nanosecond Pulse Burnout Properties of One Micron MESFETS

Calderbank, J.M.
80012 The Effects of High Humidity Environments on Electrostatic Generation and Discharge

Calle, C.
2005212 Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Calvin, H.
80225 Measurement of Fast Transients and Application to Human ESD
81001 A Closer Look at the Human ESD Event

Cambieri, J.
2012298 ESD Induced Leakage Current Increase of Diffused Diodes

Camp,D
2012402 A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 6100-4-2 Robustness Without on Board Suppressors

Campbell, D.S.
86208 ESD Pulse and Continuous Voltage Breakdown in MOS Capacitor Structures
90162 Experimental & Theoretical Studies of EOS/ESD Oxide Breakdown in Unprotected MOS Structures
92112 Parametric Drift in Electrostatically Damaged MOS Transistors

Campbell, R.W.
95218 Use of Static-Safe Polymers in Automated Handling Equipment

Campi, J.
2012319 Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers

Cao, J.
2013056 Design and Verification of a Novel Multi-RC-Triggered Power Clamp Circuit for On-Chip ESD Protection
2013248 Photon Accelerated Turn-on of High-Voltage ESD Diode Breakdown
20163A3 Novel Insights into the Power-off and Power-on Transient Performance of Power-Rail ESD Clamp Circuit

Cao, S.
2008235 ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Cao, Y.
2008221 ESD Concept for High-Frequency Circuits
2010239 A TLP-Based Characterization Method for Transient Gate Biasing of MOS Devices in High-Voltage Technologies
2010283 On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD
2011187 ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology
2012353 Statically Triggered Active ESD Clamps for High-Voltage Applications
2014268 TLP Failure Level Extraction Despite Reflected Waves
2014318 ESD Troubleshooting Using Multi-level TLP
20157A4 Active Clamp Design for On-Chip GUN Protection
20174A3 How to Build a Generic Model of Complete ICs for System ESD and Electrical Stress Simulation
Capano, P.J.  
90224  The Application of “Zelec ECP” in Static Dissipative Systems  
91182  Development of Highly Efficient, Static Dissipative Systems Based On Electroconductive Powders

Cappa, V.  
97018  Influence of the Device Geometry and Inhomogeneity on the Electrostatic Discharge Sensitivity of InGaAs/InP Avalanche Photodetectors

Carabajal III, B.  
92234  A Successful HBM ESD Protection Circuit for Micron and Sub-Micron Level CMOS

Carchon, G.  
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Carey, R.  
98040  An Experimental and Theoretical Consideration of Physical Design Parameters in Field-Induced Charged Device Model ESD Simulators and Their Impact upon Measured Withstand Voltages

Carlton, R.M.  
84034  Effects of Air Ions and Electric Fields on Health and Productivity

Carn, B.  
2012254  Sampling Pin Approaches for ESD Test Applications  
20164A2  JS-002 Module and Product CDM Result Comparison to JEDEC and ESDA CDM Methods

Carol, S.C.T.  
2002382  Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD

Carradero, D.  
2000212  Evaluation of Tribocharging and ESD Protection Schemes on GMR Magnetic Recording Heads during CO2 Jet Cleaning

Carter, G.  
91050  Streaming Potential ESD Shifts during Post Dicing High Pressure Spray Rinse Operations

Carter, J.  
2000505  Effect of 1nS to 250 mS ESD Transients on GMR Heads

Casselman, W.  
2001281  A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

Castiglione, C.  
2013105  Power-to-Failure Investigation for PNP-based ESD Protections: From ns to ms

Castle, G.  
80067  Analysis of ESD Damage in JFET Preamplifiers

Catrysse, J.  
93177  Selecting Materials for Protection against ESD Using an ESD Shielding Effectiveness Meter

Cavone, M.  
94292  A Method for the Characterization and Evaluation of ESD Protection Structures and Networks

Cecchetto, L.  
2006032  Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies  
2007058  CDM Circuit Simulation of a HV Operational Amplifier Realized in 0.35µm Smart Power Technology  
2008211  Novel 190V LIGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate

Cenusa, M.  
20158A4  A Low-Impedance TLP Measurement System for Power Semiconductor Characterization up to 700V and 400A in the Microsecond Range
<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
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<tr>
<td>Cerati, L.</td>
<td>2006</td>
<td>Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies</td>
</tr>
<tr>
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<td>2006</td>
<td>Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices</td>
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<td>2007</td>
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<tr>
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<tr>
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<td></td>
<td>2013</td>
<td>HBM ESD EDA Check Method Applied to Complete Smart Power IC’s – Functional Initialization and Implementation</td>
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<tr>
<td></td>
<td>2015</td>
<td>Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC’s – Initialization and Implementation</td>
</tr>
<tr>
<td></td>
<td>2016</td>
<td>HV ESD Diodes Investigation under vf-TLP Stresses: TCAD Approach</td>
</tr>
<tr>
<td></td>
<td>2017</td>
<td>EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC’s</td>
</tr>
<tr>
<td>Cermak, R.</td>
<td>2000</td>
<td>Floating Gate EEPROM as EOS Indicators during Wafer-Level GMR Processing</td>
</tr>
<tr>
<td>Cha, S-Y</td>
<td>2013</td>
<td>Electrostatic Control and its Analysis of Roller Transferring Processes in FPD Manufacturing</td>
</tr>
<tr>
<td>Chadwick, A.</td>
<td>2009</td>
<td>Protecting Circuits from the Transient Voltage Suppressor's Residual Pulse During IEC 61000-4-2 Stress</td>
</tr>
<tr>
<td>Chaikin, S.</td>
<td>2008</td>
<td>The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)</td>
</tr>
<tr>
<td>Chaine, M.</td>
<td>9213</td>
<td>ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers</td>
</tr>
<tr>
<td></td>
<td>9406</td>
<td>A Correlation Study between Different Types of CDM Testers and “Real” Manufacturing In-Line Leakage Failures [BPR]</td>
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<td></td>
<td>9734</td>
<td>Unique ESD Failure Mechanisms during Negative to Vcc HBM Tests</td>
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<td>Investigation into Socketed CDM (SDM) Tester Parasitics</td>
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<td>Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits</td>
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<tr>
<td></td>
<td>9921</td>
<td>A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies</td>
</tr>
<tr>
<td></td>
<td>2003</td>
<td>TLP Analysis of 0.125µm CMOS ESD Input Protection Circuit</td>
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<tr>
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<td>2003</td>
<td>Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)</td>
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<tr>
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<td>2006</td>
<td>HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins</td>
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<td>2009</td>
<td>VF-TLP Round Robin Study, Analysis and Results</td>
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<tr>
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<td>2009</td>
<td>A Novel Low Voltage Base-Modulated SCR ESD Device with Low Latch-up Risk</td>
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<td>2009</td>
<td>HBM Cross Power Domain Failure Due to Secondary Tester Pulse</td>
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<td>2010</td>
<td>ESD Protection Circuit Schemes for DDR3 DQ Drivers</td>
</tr>
<tr>
<td></td>
<td>2012</td>
<td>Sampling Pin Approaches for ESD Test Applications</td>
</tr>
<tr>
<td>Chakraborty, P.</td>
<td>2006</td>
<td>HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed</td>
</tr>
<tr>
<td></td>
<td>2007</td>
<td>Modeling CDM Failures in High-Voltage Drain-Extended ESD Cells</td>
</tr>
<tr>
<td>Chakravarthy, S.</td>
<td>2013</td>
<td>Optimized Netlist Checks – Full Chip ESD Verification</td>
</tr>
<tr>
<td></td>
<td>2013</td>
<td>CDM Single Power Domain Failures in 90 nm</td>
</tr>
<tr>
<td>Chan, D.</td>
<td>2009</td>
<td>Using VFTLP Data to Design for CDM Robustness</td>
</tr>
<tr>
<td>Chandler, C.</td>
<td>9624</td>
<td>A Hybrid Technology: Static Dissipative/VCI Films</td>
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<tr>
<td>Chang, C.</td>
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<tr>
<td>97373</td>
<td>Decay-Time Characterization of ESD Materials for Use with Magnetoresistive Recording Heads</td>
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<td>Three-Dimensional Transient Simulation of Magnetoresistive Head Temperature during an ESD Event</td>
<td></td>
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<tr>
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<td>Ion Milling Induced ESD Damage during MR Head Fabrication</td>
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<tr>
<td>98360</td>
<td>A Study of ESD Sensitivity of AMR and GMR Recording Heads</td>
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<tr>
<td>99391</td>
<td>ESD Sensitivity Study of GMR Recording Heads with a Flex-On-Suspension Head-Gimbal Assembly</td>
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<tr>
<td>2001187</td>
<td>Effect of Low-Level ESD on the Lifetime of GMR Heads</td>
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<th>Chang, C.Y.</th>
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<tr>
<td>2014349</td>
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<tr>
<td>20176B2</td>
</tr>
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</table>
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97337 An Attempt to Explain Thermally Induced Soft Failures during Low Level ESD Stresses: Study of the Differences between Soft and Hard
98187 Investigations on the Thermal Behavior of Interconnects Under ESD Transients Using a Simplified Thermal RC Network
2001110 Human Body Model Test of a Low Voltage Threshold SCR Device: Simulation and Comparison with the Transmission Line Pulse Test
2005170 Impact of the CDM Tester Ground Plane Capacitance on the DUT Stress Level

Chao, C.
2010191 Engineering Fully Silicided Large MOSFET Driver for Maximum It1 Performance

Chao, C.J.
2004160 Latch-up Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

Chao, R.
2013357 An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs

Chase, E.W.
81236 Evaluation of Electrostatic Discharge (ESD) Damage to 16K EPROMS
82013 Electrostatic Discharge (ESD) Damage Susceptibility of Thin Film Resistors and Capacitors
86127 Triboelectric Charging of Personnel from Walking on Tile Floors
87205 Electrostatic Discharge Effects in GaAs FETs and MODFETS
88065 Theoretical Study of Expected EOS/ESD Sensitivity of III-V Compound Semiconductor Devices
94206 Charge Generation from Floor Materials Using a Rolling Friction Tester
96032 A Low Cost Visual Indicator for Detecting Ground Connection Failure of CRT Filter Screens
2001281 A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

Chatterjee, A.
89167 Improving the ESD Failure Threshold of Silicided NMOS Output Transistors by Ensuring Uniform Current Flow
92265 An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies

Chatty, K.
2005126 Design Automation to Suppress Cable Discharge Event (CDE) Induced Latch-up in 90nm CMOS ASICs
2005380 Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90nm CMOS ASICs
2005413 PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latch-up Robustness
2006179 Design and Characterization of a Multi-RC-Triggered MOSFET-based Power Clamp for On-Chip ESD Protection
2007028 Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology
2007250 Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies
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2007385 Process and Design Optimization of a Protection Scheme Based on NMOSFETs with ESD Implant in 65nm and 45nm CMOS
2008228 Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies
2008304 Investigation of ESD Performance of Silicide-Blocked Stacked NMOSFETs in a 45nm Bulk CMOS Technology
2009069 Technology Scaling of Advanced Bulk CMOS On-Chip ESD Protection
2009196 ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology
2009334 Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line
2010091 An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies
2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations

Chaudhary, N.
2005280 ESD Evaluation of the Emerging MuGFET Technology
Chaudhry, I.
20152A4 Robust ESD Clamp for Envelop Tracking Power Supply
20165A3 ESD Power Clamp with Adjustable Trigger Voltage for RF Power Amplifier Integrated Circuit

Cheaib, M.
2003161 A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach

Chemelli, R.G.
80017 ESD Damage from Triboelectrically Charged IC Pins
81057 Evaluation of Integrated Circuit Shipping Tubes [BPP]
83029 ESD by Static Induction
84040 A Room Ionization System for Electrostatic Charge and Dust Control
85155 The Characterization and Control of Leading Edge Transients from Human Body Model ESD Simulators
86059 Sheet Resistance Measurement of Buried Shielding Layers
94200 Controlling the Variables in a Rolling Friction Triboelectricity Test Set
94206 Charge Generation from Floor Materials Using a Rolling Friction Tester

Chen, B.
96291 CMOS-ON-SOI ESD Protection Networks

Chen, C-K
2012336 Schottky Emitter High Holding Voltage ESD Clamp in BCD Power Technology

Chen, G.
20161A1 ESD Protection Design in a-IGZO TFT Technologies

Chen, J.W.
2000456 Chip-Level Simulation for CDM Failures in Multi-Power ICs
2005100 Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-InducedLatch-up and Inter-Power SupplyLatch-up in Advanced CMOS Technologies
2012076 ESD Dynamic Methodology for Diagnosis and Predictive Simulation of HBM/CDM Events

Chen, J.Z.
97230 Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes

Chen, K.
88212 Effects of Interconnect Process and Snapback Voltage on the ESD Failure Threshold of NMOS Transistors

Chen, K-C.
2012342 PMOS-Triggered PMLSCR for High Voltage Application
2014336 A Non-Typical Latch-up Event on HV ESD Protection

Chen, K-J.
2014354 A High-Reliable Self-Isolation Current-Mode Transmitter (CM-Tx) Design for +/-60V Automotive Interface with Bulk-BCD Technology
20157A3 Investigation and Solution to the Early Failure of Parasitic NPN Triggered by the Adjacent PNP ESD Clamps
20163A2 An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology
20171A2 Deep N-well Induced Latch-up Challenges in Bulk FinFET Technology
20176B2 Novel SCR Structure for Power Supply Protection in FinFET Technology

Chen, L.C.
2005316 On-Chip System ESD Protection Design for STN LCD Drivers

Chen, S-H.
2010425 HBM Parameter Extraction and Transient Safe Operating Area
2011027 On Gated Diodes for ESD Protection in Bulk FinFET CMOS Technology
2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes
2012001 ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling
2012007 ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon Via (TSV) in 3D Stacked Integrated Circuits
Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester

Mixed-Mode Simulations for Power-on ESD Analysis

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An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs

Behavior of RF MEMS Switches under ESD Stress

Invited Paper: Plasma-charging damage and ESD, help each other?

Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads I

Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads II

An Investigation of ESD Protection for Magnetoresistive Heads

`“Direct Charging” Charge Device Model Testing of Magnetoresistive Recording Heads

A CMOS VLSI ESD Input Protection Device, DIFIDW

Design and Test Results for a Robust CMOS VLSI Input Protection Network
Chi, X.  
2003280  Flue Gas Cleaning Using Wet-Type Electrostatic Precipitator

Chiang, Y.M.  
2000413  ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors

Chim, S.  
97386  Characterization of ESD Damaged Magnetoresistive Recording Heads

Ching, D.  
2005238  EOS from Soldering Irons Connected to Faulty 120VAC Receptacles

Ching, L.Y.  
99095  Influence of gate length on ESD-performance for deep sub-micron CMOS technology

Chini, A.  
2001249  Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

Cho, D.H.  
2001398  Improving the Balanced Coaxial Differential Probe for High-Voltage Pulse Measurements
2012396  Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Cho, H.  
2002123  Effects of ESD Transients on the Properties of GMR Heads

Cho, W-H.  
2010279  Static Charge Induced Orientation of Liquid Crystals in LCD Panels

Choi, C-J.  
2012396  Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Choi, E.  
2010203  Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Choi, S-S.  
2012396  Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Chou, B.C.  
2008115  Wafer-Level Charged Device Model Testing

Chou, J.T.  
2000105  Comparison and Correlation of ESD HBM (Human Body Model) Obtained Between TLP, Wafer-Level, and Package-Level Tests

Chou, S.  
2004346  Breakdown Behavior of TMR Head in ESD Transients
2006108  Breakdown Evaluation of Ultrathin Barrier Magnetic Tunnel Junctions with V-Ramp Testing
2007111  Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions
2011323  Machine Model Evaluation and Interconnect Effect Study for TMR HGA

Christoforou, Y.  
2008014  On the Relevance of IC ESD Performance to Product Quality
2008317  Active ESD Protection Design Methodology for DC/DC Converters
2011120  Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment
2014384  Characterization Methods to Replicate EOS Fails
Chu, C.
98311 Ultra Low Impedance Transmission Line Tester
99235 ESD Performance Optimization of Ballast Resistor on Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology
2000413 ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors
2009286 Using VFTLP Data to Design for CDM Robustness

Chu, L.W.
2012331 Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process
2013015 High CDM Resistant Low-Cap SCR for 0.9 V Advanced CMOS Technology
20176B1 VFTLP Characteristics of ESD Diodes in Bulk Si Gate-all-Around Vertically Stacked Horizontal Nanowire Technology

Chua, E.C.
2002382 Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD

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2001032 ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device

Chubb, J.N.
92203 Experimental Comparison of Methods of Charge Decay Measurements for a Variety of Materials
99049 Electrostatic Test Methods Compared
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Chum, K.W.K.
91163 Investigation of Latent Failures Due To ESD in CMOS Integrated Circuits
92106 The Integrity of Gate Oxide Related to Latent Failures under EOS/ESD Conditions

Chun, J.H.
2005033 RF ESD Protection Strategies: Co-design vs. Low-C Protection
2008235 ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Chundru, R.
2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)

Chung, Y.
2002348 Investigations for a Smart Power and Self-Protected Device under ESD Stress through Geometry and Design Considerations for

Chwastek, E.J.
89149 A New Method for Assessing the Susceptibility of CMOS Integrated Circuits to Latch-Up: The System Transient Technique

Ciappa, M.
2001249 Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes
2005060 SCR Operation Mode of Diode Strings for ESD Protection

Claeys, C.
2008059 Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques

Clark, L.T.
2003027 Methods for Designing Low-leakage Power Supply Clamps

Clark, N.K.
95295 Melt Filaments in n+p+n Lateral Bipolar ESD Protection Devices
97246 Protection of High Voltage Power and Programming Pins

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79193 Electrostatic Discharge Protection Using Silicon Transient Suppressors
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Effect of Large Device Capacitance on FICDM Peak Current

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96227 Vanadium Pentoxide Based Antistatic Coatings

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2005280 ESD Evaluation of the Emerging MuGFET Technology

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2005212 Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Cline, R.A.

92234 A Successful HBM ESD Protection Circuit for Micron and Sub-Micron Level CMOS

2001192 Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

2004132 Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers

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2005298 A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65nm CMOS Technologies

2006222 High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies

Cohen, L.

98124 Outgassing, Volatile Organic Content, and Contamination Content of Materials Used in Today’s Electronics Workplace

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2000041 Optimizing the Performance of a Composite ESD Circuit Protection Device

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94257 The Effect of Oxidation of the Poly Gate on the ESD Performance of CMOs ICs

Cole, Jr., E.I.

2001238 Human Body Model, Machine Model, and Charged Device Model ESD Testing of Surface Micromachined Microelectromechanical

Colinge, J.P.

93215 The ESD Protection Capability of SOI Snapback NMOSFETs: Mechanisms and Failure Modes

Collaert, N.

2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications

2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets

2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness

2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design

20151A4 ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies

20166A2 VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires

Collins, G.

2007068 Modeling CDM Failures in High-Voltage Drain-Extended ESD Cells

Colombo, P.

2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

Colvin, J.B.

90173 A New Technique to Rapidly Identify Low Level Gate Oxide Leakage in Field Effect Semiconductors Using a Scanning Electron

93109 The Identification and Analysis of Latent ESD Damage On CMOS Input Gates [BPR]

Concannon, A.

2002101 Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway

2010157 SCCF-System to Component Level Correlation Factor

2010293 Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays

2010425 HBM Parameter Extraction and Transient Safe Operating Area

2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes

2012051 Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester
2012402  A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 61000-4-2 Robustness Without on Board Suppressors
2013133  Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications
2014289  Identification of Two-Probe TLP Contact Resistance Issues and Proposed Solutions
20153B1  HBM Failures Induced by ESD Cell Turn-Off and Circuit Interaction with ESD Protection
20165A2  Impact of Sub-Threshold SOA on ESD Protection Schemes

Condon, G.P.
85118  Simplified Methods for Checking ESD Bags and Handling Packages

Connerney, D.
2011285  A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal ICs

Connor, J.
2010111  Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation

Consiglio, R.J.
88155  A Method of Calibration for Human Body Model ESD Testers to Establish Correlatable Results
93093  AC and Transient Latch-up Characteristics of a Twin-Well CMOS Inverter with Load Capacitance
95199  ESD Reliability Impact of P+ Pocket Implant on Double Implanted NLDD MOSFET

Contiero, C.
2001102  Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology

Cook, C.
92149  Characterization and Failure Analysis of Advanced CMOS Sub-Micron ESD Protection Structures
93149  Characterization of New Failure Mechanisms Arising From Power-Pin ESD Stressing

Coolbaugh, D.
2005090  The Influence of High Resistivity Substrates on CMOS Latch-up Robustness

Coonce, H.E.
87093  Electrostatic Discharge Testing of Circuit Packs

Cooper, D.W.
97271  Measurement of Cleanroom Fabric Surface Resistivities

Cooper, E.
2002163  A New ESD Model: The Charged Strip Model

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99268  Processable ESD Control Materials Filled With Tunable Intrinsically Conductive Polymer Nanocomposites

Cooray, S.
2013037  Basic Characteristics of the Field Assisted Air Ionizer

Cordoni, M.
2013313  Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

Cordova, W.H.
85100  A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models with

Cormier, B.
93139  Coaxial Probe to Measure ESD Voltage Waveforms with One Nanosecond Risetimes

Corsi, M.
93209  ESD Protection of BICMOS Integrated Circuits Which Need To Operate in the Harsh Environments of Automotive Or Industrial

Cottrell, P.E.
90218  Electrostatic Discharge Protection for a 4-Mbit DRAM [BPR]
<table>
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<tr>
<th>Author</th>
<th>Publication Year</th>
<th>Title</th>
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<tbody>
<tr>
<td>Courau, L.</td>
<td>2016</td>
<td>An Automated Tool for Chip-Scale ESD Network Exploration and Verification</td>
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<tr>
<td>Courbeau, C.</td>
<td>2004</td>
<td>Wire Bonding Tip Study for Extremely ESD Sensitive Devices</td>
</tr>
<tr>
<td>Courivaud, B.</td>
<td>2014</td>
<td>Novel 3D Back-to-Back Diodes ESD Protection</td>
</tr>
<tr>
<td>Cowden, B.</td>
<td>2011</td>
<td>New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications</td>
</tr>
<tr>
<td>Coyle, R.</td>
<td>99287</td>
<td>Electrostatic Discharge (ESD) Mechanism for Battery Charge Contact Failure in Cordless Phones</td>
</tr>
<tr>
<td>Creto, G.</td>
<td>2015</td>
<td>A Low-Impedance TLP Measurement System for Power Semiconductor Characterization up to 700V and 400A in the Microsecond Range</td>
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<tr>
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<td>98187</td>
<td>Investigations on the Thermal Behavior of Interconnects Under ESD Transients Using a Simplified Thermal RC Network</td>
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<tr>
<td>Cristofoi, A.</td>
<td>2013</td>
<td>Thyristor Compact Model for ESD, DC and RF Simulation</td>
</tr>
<tr>
<td>Cristoleaneau, S.</td>
<td>2010</td>
<td>Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration</td>
</tr>
<tr>
<td>Crockett, R.G.</td>
<td>84196</td>
<td>ESD Sensitivity and Latency Effects of Some HCMOS Integrated Circuits</td>
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<tr>
<td>Croft, G.D.</td>
<td>92243</td>
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<td>94135</td>
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<td>96276</td>
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<td>97083</td>
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<td>2000097</td>
<td>A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods</td>
</tr>
<tr>
<td>Crosby, J.M.</td>
<td>87028</td>
<td>Thermoplastic Composites for ESD Protection</td>
</tr>
<tr>
<td>Crouch, K.E.</td>
<td>80167</td>
<td>Lightning Protection Design for a Photovoltaic Concentrator</td>
</tr>
<tr>
<td>Crovato, R.</td>
<td>97018</td>
<td>Influence of the Device Geometry and Inhomogeneity on the Electrostatic Discharge Sensitivity of InGaAs/InP Avalanche Photodetectors</td>
</tr>
<tr>
<td>Crowe, D.</td>
<td>99160</td>
<td>Latent ESD Failures in Schottky Barrier Diodes</td>
</tr>
<tr>
<td></td>
<td>2000387</td>
<td>Random GaAs IC’s ESD Failures Caused by RF Test Handler</td>
</tr>
<tr>
<td>Crowley, J.M.</td>
<td>88084</td>
<td>Resistance Testing of Static Dissipative Worksurfaces</td>
</tr>
<tr>
<td></td>
<td>2003285</td>
<td>Biased-Plate Characterization of Pulsed DC Ionizers</td>
</tr>
<tr>
<td>Crown, E.M.</td>
<td>97153</td>
<td>Mathematical Modeling of Electrostatic Propensity of Protective Clothing Systems</td>
</tr>
</tbody>
</table>
Cui, Q.  
2009204 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses

Cullop, D.M.  
86111 Methodology for Evaluation of Static-Limiting Floor Finishes  
89023 Controlling Voltage on Personnel

Currence, R.  
89175 A "Waffle" Layout Technique Strengthens the ESD Hardness of the NMOS Output Transistor

Czarnecki, P.  
2010443 Behavior of RF MEMS Switches under ESD Stress

Czarnecki, S.  
2007117 Tunable Diode Protection for GMR and TMR Sensors  
2007136 ESD Damage and Solutions in Tape Head Manufacturing  
2010473 The Effect of ESD on the Performance of Magnetic Storage Drives

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93239 Designing On-Chip Power Supply Coupling Diodes for ESD Protection and Noise Immunity  
94141 Core Clamps for Low Voltage Technologies  
95001 Novel Clamp Circuits for IC Power Supply Protection

Dacio, M.S.  
2007222 Preventing Arcing Damage on Radio Frequency Device Wafer by Controlling ESD Resistively Level of Water for Saw and Wash

Daenen, T.  
2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node  
2004040 ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions  
2004316 Multilevel Transmission Line Pulse (MTLP) Tester

Dahl, R.  
2012402 A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 6100-4-2 Robustness Without on Board Suppressors

Dahman, S.J.  
99268 Processable ESD Control Materials Filled With Tunable Intrinsically Conductive Polymer Nanocomposites  
2001255 Recent Innovations of Inherently Conducting Polymers for Optimal (106 – 109 OHM/SQ) ESD Protection Materials  
2003306 All Polymeric Compounds: Conductive and Dissipative Polymers in ESD Control Materials

Dahn, J.  
98139 Electrostatic Hazards of Explosive, Propellant and Pyrotechnic Powders

Daily, W.  
86069 Reversible Charge Induced Failure Mode of CMOS Matrix Switch

Dale, D.  
96211 Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics toward Creating a More Repeatable Simulation

Danesin, F.  
2007264 ESD Robustness of AlGaN/GaN HEMT Devices

Dangelmayer, G.T.  
83001 ESD - How often does it Happen?  
84001 A Realistic and Systematic ESD Control Plan [BPR]  
85020 Employee Training for Successful ESD Control  
92001 A Systematic ESD Program Revisited (invited)  
94001 A Successful ESD Training Program

Daniel, A.  
2011386 Filter Models of CDM Measurement Channels and TLP Device Transients
Daniel, S.
90206 Process and Design Optimization for Advanced CMOS I/O ESD Protection Devices
92149 Characterization and Failure Analysis of Advanced CMOS Sub-Micron ESD Protection Structures
93149 Characterization of New Failure Mechanisms Arising From Power-Pin ESD Stressing

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97246 Protection of High Voltage Power and Programming Pins

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98118 Electrostatic Discharges from Charged Particles Approaching a Grounded Surface

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84112 Designing to Avoid Static - ESD Testing of Digital Devices
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88190 Standards and Regulations for Evaluating ESD Immunity at the Systems Level -- An Update

Daughton, J.
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

Davenport, D.E.
82110 Metalloplastics

David, F.
20172B3 ESD Protection Structure Enhancement Against Latch-up Issue using TCAD Simulation

Davies, D.K.
96322 The ESD Threat
99054 Charging and Ignition of Sprayed Fuel

Davis, J.
2003070 TLP Analysis of 0.125µm CMOS ESD Input Protection Circuit
2009301 HBM Cross Power Domain Failure Due to Secondary Tester Pulse

Davis, M.
2001187 Effect of Low-Level ESD on the Lifetime of GMR Heads

Day, D.
99235 ESD Performance Optimization of Ballast Resistor on Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology

de Boet, J.
2005001 Selecting an Appropriate ESD Protection for Discrete RF Power LDMOSTs

De Coster, J.
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors
2009265 A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response under EOS-ESD Stress
2010443 Behavior of RF MEMS Switches under ESD Stress
2011130 A SCR-Based ESD Protection for MEMS-Merits and Challenges

De Heyn, V.
99095 Influence of gate length on ESD-performance for deep sub-micron CMOS technology
2001461 Contributions to Standardization of Transmission Line Pulse Testing Methodology
2002274 Effect of the n+Sinker in Self-Triggering Bipolar ESD Protection Structures
2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2004316 Multilevel Transmission Line Pulse (MTLP) Tester

de Jong, P.C.
98170 Pitfalls When Correlating TLP, HBM, and MM Testing
2002354 The Impact of Substrate Resistivity on ESD Protection Devices
2007047 Designing HV Active Clamps for HBM Robustness
2008006 Gate Oxide Protection and ggNMOSTs in 65 nm
<table>
<thead>
<tr>
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<tr>
<td>2009</td>
<td>A DRC-Based Check Tool for ESD Layout Verification</td>
<td>de Kort, C.G.C.M.</td>
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<tr>
<td>2015</td>
<td>A Study of the Effect of Remote CDM Clamps in Integrated Circuits</td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>Dynamic Aspects to Current Spreading in GgNMOSTs during Current Ramp-up</td>
<td>De Raad, G.</td>
</tr>
<tr>
<td>2017</td>
<td>DNW-Controllable Triggered Voltage of the Integrated Diode Triggered SCR (IDT-SCR) ESD Protection Device</td>
<td>De Ranter, F</td>
</tr>
<tr>
<td>2003</td>
<td>Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design</td>
<td>de Vreede, P.W.H.</td>
</tr>
<tr>
<td>2005</td>
<td>Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies Avoiding Competitive</td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>Diode Network Used as ESD Protection in RF Applications</td>
<td>De Wolf, I.</td>
</tr>
<tr>
<td>2009</td>
<td>ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors</td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response under EOS-ESD Stress</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>Behavior of RF MEMS Switches under ESD Stress</td>
<td>De Zutter, D.</td>
</tr>
<tr>
<td>2001</td>
<td>ESD Entry Points: Coaxial Cables vs. Shielding Apertures</td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td>Statistical Failure Analysis of Military Systems for High Altitude EMP</td>
<td></td>
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<tr>
<td>2002</td>
<td>An Automated Test of Tribocharging for Automotive Seating Fabric</td>
<td>DeAngelis, A.</td>
</tr>
<tr>
<td>2005</td>
<td>Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor</td>
<td>Deepak, G.</td>
</tr>
<tr>
<td>2011</td>
<td>HBM ESD Robustness of GaN-on-Si Schottky Diodes</td>
<td>Deferm, L.</td>
</tr>
<tr>
<td>2008</td>
<td>Device ESD Susceptibility Testing and Design Hardening [BPP]</td>
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<tr>
<td>2009</td>
<td>The Characterization and Control of Leading Edge Transients from Human Body Model ESD Simulators</td>
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<tr>
<td>2011</td>
<td>Degradation in InGaAsP Semiconductor Lasers Resulting From Human Body Model ESD</td>
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<td>2009</td>
<td>A Robust ESD Event Locator System with Event Characterization</td>
<td></td>
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<tr>
<td>2010</td>
<td>An Experimental and Theoretical Consideration of Physical Design Parameters in Field-Induced Charged Device Model ESD Simulators and Their Impact upon Measured Withstand Voltages</td>
<td></td>
</tr>
<tr>
<td>2005</td>
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<tr>
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<td>HBM ESD Robustness of GaN-on-Si Schottky Diodes</td>
<td></td>
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<tr>
<td>2008</td>
<td>Active ESD Protection Design Methodology for DC/DC Converters</td>
<td></td>
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<tr>
<td>2007</td>
<td>Influence of Well Profile and Gate Length on the ESD Performance of a Fully Silicided 0.25 um CMOS Technology</td>
<td></td>
</tr>
<tr>
<td>2004</td>
<td>ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions</td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology</td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS</td>
<td></td>
</tr>
</tbody>
</table>
Dehan, P.
20153A3 A Comprehensive ESD Verification Flow at Transistor Level for Large SoC Designs

DeHeyn, V.
2003088 Characterization and Modeling of Transient Device Behavior under CDM ESD Stress

Dekker, M.
2010341 Pitfalls for CDM Calibration Procedures
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
20163B3 HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document?

Dekkers, D.J.
87129 An ESD Expert System

Dela Cruz, W.A.
2007222 Preventing Arcing Damage on Radio Frequency Device Wafer by Controlling ESD Resistively Level of Water for Saw and Wash

Delage, J.
95124 ESD Measurements and Corrective Actions for Integrated Circuits (IC) Lead Inspection/Handling Systems

Delecki, J.
92277 Shallow Trench isolation Double-Diode Electrostatic Discharge Circuit and Interaction with DRAM Output Circuitry

Della Giovampaola, C.
2012240 A μ-TLP System Realized in MEMS Technology

Delmas, A.
2009165 Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
2012409 Impact of Snapback Behavior on System Level ESD Performance with Single and Double Stack of Bipolar ESD Structures
2013258 Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement

Demmler, M.
97027 Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs

den Dekker, A.
2001228 Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection

Deng, F.
2001295 A Study of GMR Breakdown Damage in Cleaning

Deng, Q.
2001415 Electromagnetic Field Generated by Transient Electrostatic Discharges (ESD) from Person Charged with Low Electrostatic Voltage

Denison, M.
2003313 Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications

Denson, W.K.
82001 ESD Susceptibility Testing of Advanced Schottky TTL
88007 A Review of EOS/ESD Field Failures in Military Equipment

Denton, L.R.
87036 Contaminated Antistatic Polyethylene

Depetro, R.
2001102 Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology
Derikx, R.
2011267 A Contribution to the Evaluation of HMM for IO Design
20163B3 HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document?

DerMarderosian, A.
79022 The Generation of Electrostatic Charges in Silicone Encapsulants during Cyclic Gaseous Pressure Tests

Desai, G.G.
99124 Measurement of Ionizer Performance - a New Approach

Desai, S.
92136 ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Detalle, M.
20155A1 ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package

Devoldere, P.
94301 A Comparative Study of "Low Cost" 1.3 µm Laser Diodes: ESD Performance

Dey, K.A.
82001 ESD Susceptibility Testing of Advanced Schottky TTL

Dhakad, H.
2011307 An Automated Approach for Verification of On-Chip Interconnect Resistance for Electrostatic Discharge Paths
2012135 Chasing a Latent CDM ESD Failure by Unconventional FA Methodology

Di Biccari, L.
2013105 Power-to-Failure Investigation for PNP-based ESD Protections: From ns to ms
20153A2 Schematic-Level and Layout-Level ESD EDA Check Methodology Applied to Smart Power IC’s – Initialization and Implementation
20162A1 HV ESD Diodes Investigation under vf-TLP Stresses: TCAD Approach
20173B2 EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC’s

Diatta, M.
2011241 Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection

Diaz, C.H.
92088 Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices
93083 Studies of EOS Susceptibility in 0.6 mm nMOS ESD I/O Protection Structures
94106 Bi-Modal Triggering for LVSCR ESD Protection Devices

Dibra, D.
20152B2 ESD Induced Functional Upset in Magnetic Sensor ICs

Dickson, N.
95043 Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors

Diep, J.
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry

Diep, T.
88162 A Microwave-Bandwidth Waveform Monitor for Charged-Device Model Simulators [BPP]
89059 A Field-induced Charged-Device Model Simulator [BPP]
92159 PIN Photodetectors-The ESD Bottleneck in Laser Packages
95175 A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices
96167 Charged Device Model (CDM) Metrology: Limitations and Problems
99203 Issues Concerning CDM ESD Verification Modules-The Need to Move to Alumina
2000072 The Importance of Standardizing CDM ESD Test Head Parameters to Obtain Data Correlation
2001445 Integration of TLP Analysis for ESD Troubleshooting
2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
Dietz, F.
2003116 Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness

Dinger, III, F.B.
88024 Developing and Maintaining an Effective ESD Training Program

DiSarro, J.
2008242 A Dual-Base Triggered SCR with Very Low Leakage Current and Adjustable Trigger Voltage
2009196 ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology
2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations
2012312 Design and Optimization of SCR Devices for On-Chip ESD Protection in Advanced SOI CMOS Technologies
2012319 Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers
2013009 Investigation of SOI SCR Triggering and Current Sustaining under DC and TLP Conditions
2013224 Maximizing ESD Robustness of Current-Mode-Logic (CML) Driver with Internal Gate Bias Network
2013391 Influence of Package Parasite Elements on CDM Stress

Dissegna, M.
2004107 Study of CDM Specific Effects for a Smart Power Input Protection Structure
2006032 Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies
2006274 Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
2007058 CDM Circuit Simulation of a HV Operational Amplifier Realized in 0.35µm Smart Power Technology
2008211 Novel 190V LiGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate
2013383 Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components
20166B2 Case Study of DPI Robustness of a MOS-SCR Structure for Automotive Applications
20165A2 Impact of Sub-Threshold SOA on ESD Protection Schemes

Djobava, R.
95095 Calculation and Measurement of Transient Fields of Voluminous Objects

Dobbin, A.
2011076 When Good Trigger Circuits Go Bad: A Case History
2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

Dobbs, B.
83021 Air Force Maintenance Program for Electrical Overstress/Electrostatic Discharge (EOS/ESD) Control

Dobson, J.
2012254 Sampling Pin Approaches for ESD Test Applications

Dodson, G.A.
79188 The Phantom Emitter - an ESD-Resistant Bipolar Transistor Design and its Applications to Linear Integrated Circuits

Dolby, D.
92136 ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Domanski, K.
2003080 Transient Latch-up: Experimental Analysis and Device Simulation
2004299 Development Strategy for TLU-Robust Products
2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
2005060 SCR Operation Mode of Diode Strings for ESD Protection
2005245 SoC-A Real Challenge for ESD Protection?
2007347 External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique
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2012085 Topology-Aware ESD Checking: A New Approach to ESD Protection
2013268 Activities Towards a New Transient Latch-up Standard
20152B4 A Passive Coupling Circuit for Injecting TLP-Like Stress Pulses into only one End of a Driver/Receiver System
20153B2 Soft Fails Due to LU Stress of Virtual Power Domains
20165B3 EDA Approaches in Identifying Latch-up Risks
20168A3 TLP IV Characterization of a 40 nm CMOS IO Protection Concept in the Powered State
Domengès, B.
2014393 Electrical Overstress Robustness and Test Method for ICs

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79140 Square Pulse and RF Pulse Overstressing of UHF Transistors
80206 Basic Considerations in Electro-Thermal Overstress in Electronic Components
82169 Circuit Design for EOS/ESD Protection
85024 A Design Methodology for ESD Protection Networks
86173 Thick Oxide Device ESD Performance under Process Variations [BPR]
87265 Electrical Overstress in NMOS Silicided Devices
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Dong, L.
2003280 Flue Gas Cleaning Using Wet-Type Electrostatic Precipitator

Donner, J.C.
91059 Reducing Field Failure Rate with Improved EOS/ESD Design

Doucette, R.E.
85055 The Elimination of Electrostatic Discharge Failures from Silicon Gate Logic Technologies

Dournelle, S.
2003233 STMSCR: A New Multi-Finger SCR-Based Protection Structure against ESD

Downing, M.H.
83006 ESD Control Implementation and Cost Avoidance Analysis

Drab, K.
20156B2 How Six Sigma Brought Saving and Improved Manufacturing Process by 98.9%

Dray, A.
2011082 β Matrix Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology
2012015 ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process
2013199 Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology
20159A2 EOS Characterization Methodology Applied to Disable Feature of ESD Power Clamps

Dreibelbis, D.H.
83154 EOS or ESD: Can Failure Analysis Tell the Difference?

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2010325 ESD Stimulated Ignition of Metal Powders

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2000029 Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

Drew, B.
2009091 CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps

Drüen, S.
2003122 High Abstraction Level Permutational ESD Concept Analysis
2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
2005245 SoC-A Real Challenge for ESD Protection?

Dubec, V.
2002387 Investigation of ESD Protection Elements under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry
2006274 Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
Dudek, V.  
2003116 Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness

Dugan, M.P.  
86182 Design and Characterization of Input Protection Networks for CMOS/SOS Applications

Duncan, W.  
92175 Shrink Film Packaging Evaluation

Dundigal, S.  
2010381 CDM Effect on a 65 nm SOC LNA

Dunn, C.  
92136 ESD Improvement Using Low Concentrations of Arsenic Implantation in CMOS Output Buffers

Dunn, P.  
2005126 Design Automation to Suppress Cable Discharge Event (CDE) Induced Latch-up in 90nm CMOS ASICs

Dunnihoo, J.  
2009396 Failure Detection With HMM Waveforms  
2010145 Effects of TVS Integration on System Level ESD Robustness

Durgin, D.L.  
80154 An Overview of the Sources and Effects of Electrical Overstress  
81120 An Overview of Electrical Overstress Effects on Semiconductor Devices  
82049 A Survey of EOS/ESD Data Sources

Dutton, R.W.  
2001355 Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF Applications  
2005033 RF ESD Protection Strategies: Co-design vs. Low-C Protection  
2006317 A Frequency-Domain VFTLP Pulse Characterization Methodology and its Application to CDM ESD Modeling  
2007102 Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System  
2008235 ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology  
2008258 Ultra-Fast Transmission Line Pulse Testing of Tunneling and Giant Magnetoresistive Recording Heads  
2010203 Investigation on Output Driver with Stacked Devices for ESD Design Window Engineering

Duvanaud, C.  
98118 Electrostatic Discharges from Charged Particles Approaching a Grounded Surface

Duvvury, C.  
83181 A Summary of Most Effective Electrostatic Discharge Protection Circuits for MOS Memories and their Observed Failure Modes  
85045 ESD Design Considerations for ULSI  
86173 Thick Oxide Device ESD Performance under Process Variations [BPR]  
88053 Photoemission Testing for ESD Failures Advantages and Limitations  
88201 A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes [BPR]  
88206 Output ESD Protection Techniques for Advanced CMOS Processes [BPP]  
89190 Input Protection Design for Overall Chip Reliability  
91088 A Synthesis of ESD Input Protection Scheme  
92088 Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices  
93083 Studies of EOS Susceptibility in 0.6 mm nMOS ESD I/O Protection Structures  
94237 The Impact of Technology Scaling On ESD Robustness and Protection Circuit Design [BPP]  
95162 Advanced CMOS Protection Device Trigger Mechanisms during CDM [BPR]  
96285 EOS/ESD Analysis of High-Density Logic Chips  
97230 Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes  
98104 A Simulation Study of HBM Failure in an Internal Clock Buffer and the Design Issues for Efficient Power Pin Protection Strategy  
98208 An Automated Tool for Detecting ESD Design Errors  
99212 A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies  
2001012 5-V Tolerant Fail-Safe ESD Solutions for a 0.18μm Logic CMOS Process
Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology
Integration of TLP Analysis for ESD Troubleshooting
Efficient PnP Characteristics of pMOS Transistors in Sub-0.13 µm ESD Protection Circuits
Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers
Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps
Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window
ESD Evaluation of the Emerging MuGFET Technology
Problems with IO to all Other IOs ESD Stress Test: Two Case Studies
HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies
CDM Peak Current Variations and Impact upon CDM Performance Thresholds
Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications
Single Pulse CDM Testing and its Relevance to IC Reliability
Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests
The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
Electrical and Thermal Scaling Trends for SOI FinFET ESD Design
Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM
Influence of CDM Tester Plate Size on Discharge Current
Diode Isolation Concept for Low Voltage and High Voltage Protection Applications
Protecting Circuits from the Transient Voltage Suppressor's Residual Pulse during IEC 61000-4-2 Stress
SPICE Simulation Methodology for System Level ESD Design
TLP Characterization for Testing System Level ESD Performance
Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing
Capturing Real World ESD Stress with Event Detector
Two New Unexplained and Unresolved HBM Tester Related Failures
Sampling Pin Approaches for ESD Test Applications
IEC System Level ESD Challenges and Effective Protection Strategy for USB2 Interface
Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components

Dwyer, V.M.
Experimental & Theoretical Studies of EOS/ESD Oxide Breakdown in Unprotected MOS Structures
Parametric Drift in Electrostatically Damaged MOS Transistors

Dyer, M.J.D.
The Antistatic Performance of Cleanroom Clothing - Do Tests on the Fabric Relate to the Performance of the Garment
Test Procedures for Predicting Surface Voltages on Inhabited Garments

Eatmon, R.
An Automated ESD Verification Tool for Analog Design

Eaton, J.
Tribocharging of Materials Used In Tape Heads and Associated ESD Damage

Eberhardt, E.P.
Nondestructive Failure Analysis of VLSI Zener Diodes

Edgington, G.
On-Chip Sensors to Measure Level of Transient Events

Edwards, H
Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications
Egger, P.
93129 Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model [BPP]
94049 Influence of Tester, Test Method and Device Type on CDM ESD Testing
94069 Influence of Tester Parasitics on "Charged Device Model" Failure Thresholds
97366 Does the ESD-Failure Current Obtained by Transmission Line Pulsing Always Correlate to Human Body Model Tests?

Ehrmaier, B.
96259 Some Results in Measuring Static Decay

Eklof, P.
86081 Studies and Revelation of Latent ESD-Failures

Elder, R.A.
90251 Resistivity Measurements on Buried Conductive Layers

Ellis, D.
2009017 Transient Safe Operating Area (TSOA) Definition for ESD Applications
2010399 A New Method to Evaluate Effectiveness of CDM ESD Protection

Ellis, E.B.
82179 Electrostatic Discharge at the Product Level

Enders, J.
81106 Susceptibility of IC's in Electrostatic Damage Step-Stress Tests

Eng, D.C.
95304 Quantifying ESD/EOS Latent Damage and Integrated Circuit Leakage Currents

Englisch, A.
2000394 A Study of the Mechanisms for ESD Damage to Reticles

Enlow, E.W.
80059 Failure Threshold Distributions in Bipolar Transistors
81145 Determining an Emitter-Base Failure Threshold Distribution of NPN Transistors
83056 Power Failure Modeling of Integrated Circuits

Enoch, D.R.
83048 A Programmable Equipment for Electrostatic Discharge Testing to Human Body Models
83185 ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics [BPP]
84165 Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
85132 An Experimental Investigation of ESD-Induced Damage to Integrated Circuits on Printed Circuit Boards
86224 An Experimental Validation of the Field-Induced ESD Model

Enokizono, M.
2010273 Neutralizing Current Sensor for AC Corona Ionizer

Entringer, C.
2005053 Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology
2006166 Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection
2009314 Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage
2010011 TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior

Eppes, D.
2009101 Metal and Silicon Burnout Failures from CDM ESD Testing
Ershov, M.

2009204 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses
2010301 Study of Power Arrays in ESD Operation Regimes
2013367 EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level
20156A2 A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures
20156A4 P2P and RMAP - New Software Tool for Quick and Easy Verification of Power Nets

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2010375  ESD Protection Circuit Schemes for DDR3 DQ Drivers

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92019 An Evaluation of Air Ionizers for Static Charge Reduction and Particle Emission

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2013367 EDA Software for Verification of Metal Interconnects in ESD Protection Networks at Chip, Block, and Cell Level  
20156A2 A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures  
20156A4 P2P and RMAP - New Software Tool for Quick and Easy Verification of Power Nets

Felder, G.  
2006240 Trends in External Ionizer Monitoring and Control

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83095 Coplanar Triboelectrification of Selected Materials

Fenouillet-Beranger, C.  
2010185 Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration  
2012015 ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process  
20151A1 Innovative High-Density ESD Protection Device in State of the Art FDSOI UTB Technologies

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2000446 ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior  
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Fledderman, C.B.
94257  The Effect of Oxidation of the Poly Gate on the ESD Performance of CMOs ICs

Fleurimont, J.
2009292  A DRC-Based Check Tool for ESD Layout Verification

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87252  The Effects of High Electric Field Transients on Thin Gate Oxide MOSFETs [BPP]

Fonteneau, P.
2007165  Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain
2008067  A Physics-Based Compact Model for ESD Protection Diodes under Very Fast Transients
2008088  A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology
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20151A1  Scalable Modeling Studies on the SCR ESD Protection Device

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89084  Electrostatic-Discharge Detectors

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99043  A Study of ESD Induced Lockups in a Semiconductor Photolithography Area

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84136  Protection of Components against Electrical Overstress (EOS) and Transients in Monitors

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2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

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20166A1 Ultra-Low Standby Current ESD Clamp MOSFET with P/N Hybrid Gate

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86193 ESD Protection Network Evaluation by HBM and CDM (Charged Package Method)
88228 VLSI ESD Phenomenon and Protection
96076 ESD and Latch up Phenomena on Advanced Technology LSI
2001419 Invited Paper: ESD Evaluation by TLP Method on Advanced Semiconductor Devices
2004125 ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices
2009038 ESD Parameter Extraction by TLP Measurement

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2013299 System Level EOS Case Studies not due to Excessive Voltages
20171B3 An ESD Case Study with High Speed Interface in Electronics Manufacturing and its Future Challenge
20173A2 Charged Device ESD Threats with High Speed RF Interfaces

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86019 A 'Tailorable' ESD Control Program for the Manufacturing Environment
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2009419 Characterization and Simulation of Real-World Cable Discharge Events
2010211 ESD Protection Program at Electronics Industry - Areas for Improvement
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2012198 Is There Correlation Between ESD Qualification Values and the Voltages Measured in the Field?
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- Study of Gated PNP as an ESD Protection Device for Mixed-Voltage and Hot-Pluggable Circuit Applications
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Gebreselasie, E.G.

- Low-Voltage Diode-Configured SiGe: C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (ITf/MAX)
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**Gefter, P.**
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- 2006: Ionization Applications and Pitfalls for Charge Neutralization in Substrate Handling

**Geissler, S.**
- 98151: Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon – Bound Source/Drain Diodes

**Gelorme, J.D.**
- 94226: Electrically Conducting Polyanilines for Electrostatic Dissipation

**Gendron, A.**
- 2006069: Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology
- 2009165: Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
- 2011035: New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications

**Gendron, R.P.**
- 89162: Designing High Performance Bipolar Devices for High ESD Robustness

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**Georgieva, K.**
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- 2008059: Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques

**Gerdemann, A.**
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- 2007289: A Novel Testing Approach for Full-Chip CDM Characterization
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- 2014232: A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry

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2008211 Novel 190V LIGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate  
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2001390 Comparison of Solutions to Minimize Voltages Induced by ESD Events on Adjacent Microstrips

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2011197 Capturing Real World ESD Stress with Event Detector

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79168 Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature
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2014223 Device Interactions between ESD Diodes and NMOS Clamps in CMOS Processes

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90193 Improved ESD-Protection of GaAs-FET Microwave Devices by New Metallization Strategy
92168 Field Emitter-Based ESD-Protection Circuits for High Frequency Devices and IC's [BPP]

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<td>2010</td>
<td>Anomalous ESD Failures in MLDMOS during Reverse Recovery</td>
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<tr>
<td>Hasebe, T.</td>
<td>2005</td>
<td>Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor</td>
</tr>
<tr>
<td></td>
<td>2006</td>
<td>Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications</td>
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<td></td>
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<td>Voltage Overshoot Study in 20V DeMOS-SCR Devices</td>
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<td></td>
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<tr>
<td></td>
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<td>2009</td>
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<td></td>
<td>2009</td>
<td>On-Wafer Human Metal Model Measurements for System-Level ESD Analysis</td>
</tr>
<tr>
<td>Hasegawa, K.</td>
<td>2014</td>
<td>CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus</td>
</tr>
<tr>
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<td></td>
<td>A Study of Relation between a Power Supply ESD and Parasitic Capacitance</td>
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<tr>
<td></td>
<td>2007</td>
<td>A Study for ESD Robustness of Cascoded NMOS Driver</td>
</tr>
<tr>
<td></td>
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</tr>
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<td></td>
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<td></td>
<td>2010</td>
<td>Impact of Difference between Discharging Methods on CDM Testing</td>
</tr>
<tr>
<td>Haspeslagh, L.</td>
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</tr>
<tr>
<td></td>
<td>8912</td>
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</tr>
<tr>
<td>Hatanaka, N.</td>
<td>2001</td>
<td>Field Emission Noise Caused by Capacitance Coupling ESD in AMR/GMR Heads</td>
</tr>
<tr>
<td>Hatchard, C.</td>
<td></td>
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<tr>
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</tr>
<tr>
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</tr>
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<td>Havermann, R.L.</td>
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</tr>
<tr>
<td>Hawkins, C.</td>
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</tr>
<tr>
<td>Hayano, K.</td>
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<td>A Simulation Analysis of Quarter-Micron CMOS LSI Input Circuit Behavior under CDM-ESD for Protection Device Improvement</td>
</tr>
<tr>
<td>Hayashi, H.</td>
<td>2004</td>
<td>ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices</td>
</tr>
</tbody>
</table>
Haynes, R.
99282  Development of Accelerated Aging Test for ESD/EMI Protective Materials and Electrical Discontinuity at Seams and Interconnections

Hays, R.A.
81202  EOS Threshold Determination of Electro-Explosive Devices
82034  Electrical Overstress Threshold Testing

He, C-W
2012342  PMOS-Triggered PMLSCR for High Voltage Application
2014336  A Non-Typical Latch-up Event on HV ESD Protection

He, Y-H
2012342  PMOS-Triggered PMLSCR for High Voltage Application

Head, G.O.
81040  A Low-Cost Program for Evaluation of ESD Protective Materials and Equipment
81225  Time-Related Improvements of Electrical Characteristics in Electrostatically Damaged Operational Amplifiers
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Hébert, F.
2008083  Potential Barrier Based Clamp: A New Device Structure for Low Voltage Triggering

Hee Lee, T.
2008191  Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer

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2006274  Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
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20159A1  Debug and Prediction of EOS Events Using Long Duration Transmission Line Pulse (TLP) Measurement

Hein, K.
2005238  EOS from Soldering Irons Connected to Faulty 120VAC Receptacles

Heinecke, H.
97027  Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs

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20152A2  Self-ESD-Protected Transmission Line Broadband in CMOS28nm UTBB-FDSOI

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Helling, K.H.
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2012001  ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling
2012007  ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon via (TSV) in 3D Stacked Integrated Circuits
2012051  Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester
2013001  Exploring ESD Challenges in Sub-20-nm Bulk FinFET CMOS Technology Nodes
2013022  ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices
2013148  Impact of the On-Chip and Off-Chip ESD Protection Network on Transient-Induced Latch-up in CMOS IC
2014282 Anti-Series GgNMOS ESD Clamp for Space Application IC’s
20151A3 VFTLP Characteristics of ESD Protection Diodes in Advanced Bulk FinFET Technology
20151A4 ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies
20155A1 ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package
20166A2 VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires
20176B1 VFTLP Characteristics of ESD Diodes in Bulk Si Gate-All-Around Vertically Stacked Horizontal Nanowire Technology

Hellstrom, S.
86081 Studies and Revelation of Latent ESD-Failures

Henderson, K.
2010091 An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies

Henry, L.G.
94324 Failure Analysis of CMOS PALs Exhibiting ESD-Type Polygate Short to Substrate Using a State-Of-The-Art IC Diagnostic uProber
96167 Charged Device Model (CDM) Metrology: Limitations and Problems
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2013268 Activities Towards a New Transient Latch-up Standard
20164A1 Improving CDM Measurements with Frequency Domain Specifications

Hensel, W.A.
91041 Avoiding Costly Pitfalls in Establishing an ESD Control Program

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2007117 Tunable Diode Protection for GMR and TMR Sensors

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2002354 The Impact of Substrate Resistivity on ESD Protection Devices
2007047 Designing HV Active Clamps for HBM Robustness

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2014258 Reflection Control in VF-TLP Systems

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2006334 Methods to Remove Anomalies from Human Body Model Pulse Generators
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2011076  When Good Trigger Circuits Go Bad: A Case History

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80067  Analysis of ESD Damage in JFET Preamplifiers

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99097  Electrostatic Failure of X-Band Silicon Schottky Barrier Diodes

Higashi, N.  
80161  Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Hijzen, E.A.  
2001228  Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection

Hilbricht, O.  
2014215  Do Devices on PCBs Really See a Higher CDM-like ESD Risk?  
20158A3  Practical HBM Testing with Statistical Pin Combinations

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85006  ESD in Semiconductor Wafer Processing - An Example

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2009414  ESD Event Receiver for System Level Testing  
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92175  Shrink Film Packaging Evaluation  
93173  Expanded Evaluation of Static Protective Shrink Wrap Film

Hiramoto, T.  
98018  Controlling ESD and Absorbing and Shielding EMW by Using Conductive Fiber in Aircraft

Hirano, T.  
2010369  Anomalous ESD Failures in MLDMOS during Reverse Recovery  
2011053  Source Engineering for ESD Robust NLDMS
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2008332 New Protection Techniques and Test Chip Design for Achieving High CDM Robustness  
2009119 An Investigation of Input Protection for CDM Robustness in 40 nm CMOS Technology  
2010353 Impact of Difference between Discharging Methods on CDM Testing  

Hirata, M.  
2010119 Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation  

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20164B1 An ESD Control Method Considering the Semiconductor Device Charged Voltage  

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2008083 Potential Barrier Based Clamp: A New Device Structure for Low Voltage Triggering  

Ho, W.J.  
99235 ESD Performance Optimization of Ballist Resistor on Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology  

Ho, W-H.  
2005316 On-Chip System ESD Protection Design for STN LCD Drivers  

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2009286 Using VFTLP Data to Design for CDM Robustness  

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2005033 RF ESD Protection Strategies: Co-design vs. Low-C Protection  

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96110 Immediate Elimination of Gross ESD Failures in PLCC MECL Product Line through Innovative Techniques  

Hoffman, T.  
2011027 On Gated Diodes for ESD Protection in Bulk FinFET CMOS Technology  

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2006014 ESD Damage due to HBM Stressing of Non-Connected Pins  
2013361 Using Static Voltage Analysis and Voltage-Aware DRC to Identify EOS and Oxide Breakdown Reliability Issues  

Hogan, M  
2013361 Using Static Voltage Analysis and Voltage-Aware DRC to Identify EOS and Oxide Breakdown Reliability Issues  

Hogle, N.  
2017A3 Enhanced nFinFET ESD Performance
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   2001385 The EMI/ESD Environment of Large Server Installations
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   2008076 Discrete ESD Protection Diode during a System Level Pulse: Comparison of Simulation with Measurements
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   84078 An Experimental Study of the ESD Screening Effectiveness of Anti-Static Bags [BPR]
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   96101 Linewidth Control Effects on MOSFET ESD Robustness

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   83017 Analysis of Electrostatic Charge Propensity of Floor Finishes

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   91074 A New ESD Protection Concept for VLSI CMOS Circuits Avoiding Circuit Stress

Honda, M.
   84124 EMI Characteristics of ESD in a Small Air Gap--ARP Governs the EMI--
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   2012263 System Failures due to an Induced ESD within the System

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Hong, C
2011035 New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications
2013232 High-Voltage Asymmetrical Bi-Directional Device for System-Level ESD Protection of Automotive Applications on a BiCMOS Technology

Hong, S.
93157 Two-Dimensional Electrothermal Simulations and Design of Electrostatic Discharge (ESD) Protection Circuit

Hong, W-K
2012396 Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Hongmei, Li
2008228 Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies

Hopkins, D.C.
80035 Protective Level Comparisons for Voltage Transient Suppressors (120 V, AC Type)

Hopkins, M.
98029 Metrology and Methodology of System Level ESD Testing
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004141 Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

Hopper, P.J.
2002101 Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway
2004117 Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application
2005387 Implementation of High VT Turn-on in Low-Voltage SCR Devices
2006064 Dual-Direction Isolated NMOS-SCR Device for System Level ESD Protection
2007053 Voltage Overshoot Study in 20V DeMOS-SCR Devices
2007075 Implementation of Dual-Direction SCR Devices in Analog CMOS Process
2008196 Small Footprint Trigger Voltage Control Circuit for Mixed-Voltage Applications
2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD Stress
2008242 A Dual-Base Triggered SCR with Very Low Leakage Current and Adjustable Trigger Voltage
2009364 Self-Protection Capability of Power Arrays
2009405 On-Wafer Human Metal Model Measurements for System-Level ESD Analysis
2010157 SCCF-System to Component Level Correlation Factor
2010293 Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays
2010301 Study of Power Arrays in ESD Operation Regimes
2010425 HBM Parameter Extraction and Transient Safe Operating Area
2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes

Hoque, M.
2000097 A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods

Horgan, E.L.
80140 Assessing Electrical Overstress Effects on Electronic Systems
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82019 Limitations in Modeling Electrical Overstress Failure in Semiconductor Devices
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88033 Resolving ESD Incidents in Spacecraft Production Systems

Horiguchi, N.
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20176B1 VFTLP Characteristics of ESD Diodes in Bulk Si Gate-all-Around Vertically Stacked Horizontal Nanowire Technology

Horiguchi, Y.
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<tr>
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<tr>
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<tr>
<td>Hsu, Y-Y.</td>
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<tr>
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<tr>
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<tr>
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<td>The Effects of High Electric Field Transients on Thin Gate Oxide MOSFETs [BPP]</td>
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</tr>
<tr>
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<td>Effect of Substrate Contact on ESD Failure of Advanced CMOS Integrated Circuits</td>
</tr>
</tbody>
</table>
Hu, J.  2001192 Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

Hu, Y.  87179 High Density Input Protection Circuit Design in 1.2 Micrometer CMOS Technology

Hua, C.  99235 ESD Performance Optimization of Ballast Resistor on Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology

Hua, R.  20173A3 Characterizing ESD Stress Currents in Human Wearable Devices

Huang, C-F.  2012336 Schottky Emitter High Holding Voltage ESD Clamp in BCD Power Technology

Huang, C-Y.  20163A2 An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology

Huang, H-C.  2014336 A Non-Typical Latch-up Event on HV ESD Protection

Huang, J.  97132 Measurements of Body Impedance for ESD

Huang, J.B.  2003098 Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor

Huang, R.W.  2004160 Latch-up Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

Huang, T.Y.  95199 ESD Reliability Impact of P+ Pocket Implant on Double Implanted NLDD MOSFET

Hudock, M.S.  81057 Evaluation of Integrated Circuit Shipping Tubes [BPP]

Hudson, S.  2010317 Problematic Natural Gas Power Plant Pumping/Irrigation

Huff, P.J.  84078 An Experimental Study of the ESD Screening Effectiveness of Anti-Static Bags [BPR]

Huffman, T.R.  87214 Room Ionization: Can It Significantly Reduce Particle Contamination?

Hughbanks, T.S.  94273 Capacitive Coupling Effects in Spark-Gap Devices

Hughes, A.  93173 Expanded Evaluation of Static Protective Shrink Wrap Film

Hughes, J.F.  84196 ESD Sensitivity and Latency Effects of Some HCMOS Integrated Circuits
Huguenin, J-L.  
2010185  Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Huh, Y.  
2000456  Chip-Level Simulation for CDM Failures in Multi-Power ICs  
2005100  Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies  
2006342  Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators Meet the

Hui, D.T.  
99105  Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips  
2000029  Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry  
2001326  Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit

Hui, J.  
2014171  HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation

Huiskamp, P.  
20154A2  An Off-Chip ESD Protection for High-Speed Interfaces

Huitsing, A.J.  
2001426  The Application of Transmission Line Pulse Testing for the ESD Analysis of Integrated Circuits  
2009292  A DRC-Based Check Tool for ESD Layout Verification  
2011163  Predictive CDM Simulation Approach Based on Tester, Package and Full Integrated Circuit Modeling

Hulett, T.V.  
81090  On Chip Protection of High Density NMOS Devices

Hull, R.E.  
87200  Analysis of High-Voltage ESD Pulse Testing on CMOS Gate Array Technology  
88039  Stress-Hardening of Damage Thresholds Due to Cumulative ESD Pulse Testing

Hulog, J.  
96095  Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures

Hulse, B.  
2010091  An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies

Hung, P-F  
2012331  Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process

Hung, S.T.  
2000485  Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach  
2001175  A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)  
2002147  Magnetoresistive Sensitivity Mapping (MSM) and Dynamic Electrical Test (DET) Correlation Study on GMR Sensor Induced by Low

Huntsman, J.R.  
79045  The Deficiencies in Military Specification MIL-B-81705: Considerations and a Simple Model for Static Protection  
82094  Test Methods for Static Control Products  
84064  Triboelectric Charge: Its ESD Ability and a Measurement Method for its Propensity on Packaging Materials

Hurkx, G.A.M.  
2001228  Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection

Huynh, P.  
86069  Reversible Charge Induced Failure Mode of CMOS Matrix Switch
<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Hyatt, H.M.</td>
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</tr>
<tr>
<td></td>
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</tr>
<tr>
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<tr>
<td></td>
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<tr>
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</tr>
<tr>
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</tr>
<tr>
<td>Hyman, M.</td>
<td>Carbon Nanotube Plastic - Packaging Materials for Class 0 Device ESD Protection</td>
</tr>
<tr>
<td>Hyslop, A.E.</td>
<td>ESD Design Considerations for ULSI</td>
</tr>
<tr>
<td>Hyvonen, S.</td>
<td>Comprehensive ESD Protection for RF Inputs</td>
</tr>
<tr>
<td></td>
<td>Combined TLP/RF Testing System for Detection of ESD Failures in RF Circuits</td>
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<tr>
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</tr>
<tr>
<td>Iannacci, J.</td>
<td>A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts</td>
</tr>
<tr>
<td>Ibarreta, R.S.</td>
<td>A Novel Ionizer Design with Both DC and AC High Voltage Bias</td>
</tr>
<tr>
<td>Iben, I.E.T.</td>
<td>Dynamic Temperature Rise of Shielded MR Sensors during Simulated Electrostatic Discharge Pulses of Variable Pulse Width</td>
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<tr>
<td></td>
<td>Amplitude and Asymmetry Study using Magnetoresistive Sensitivity Mapping (MSM) on Manufacturing ESD Failures and ESD</td>
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<tr>
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</tr>
<tr>
<td></td>
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</tr>
<tr>
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<td>A Study of Cable Discharge Events and Other Short Time Pulses of Cabled MR Sensors</td>
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<tr>
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<td>A Thermodynamic Study of ESD and EOS Induced Pinned Layer Reversal in GMR Sensors</td>
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<tr>
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</tr>
<tr>
<td></td>
<td>The Effect of ESD on the Performance of Magnetic Storage Drives</td>
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<td>Diode Protection of GMR Sensors</td>
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<tr>
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<td>FET Protection of GMR and TMR Sensors</td>
</tr>
<tr>
<td></td>
<td>Dielectric Breakdown of TMR Sensors and the Role of Joule Heating</td>
</tr>
<tr>
<td></td>
<td>EM Generated EOS in a Wire Bond</td>
</tr>
</tbody>
</table>
Ichihara, T.
2002119 Invited Paper: Analysis of Barkhausen Noise Failure Caused by ESD in a GMR Head

Ichino, S.
2005290 A Study of Relation between a Power Supply ESD and Parasitic Capacitance

Ida, R.
2000465 Verify ESD: A Tool for Efficient Circuit Level ESD Simulations of Mixed-Signal ICs
2003224 A Study of Vertical SiGe Thyristor Design and Optimization
2011035 New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications
2012285 A Physically-Based Behavioral Snapback Model

Ignatenko, A.
2003285 Biased-Plate Characterization of Pulsed DC Ionizers

Ikeda, H.
2001306 Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group
2008290 A Study of Advanced Technique on RC-Triggered NMOSFET Power Clamp
2014061 CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus

Ikehashi, T.
99225 Design Methodology of a Robust ESD Protection Circuit for STI Process 256Mb NAND Flash Memory

Ikehata, T.
2009055 Space Charge Balance Sensing for Static Control
2010273 Neutralizing Current Sensor for AC Corona Ionizer

Ille, A.
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
2007328 Reliability Aspects of Gate Oxide under ESD Pulse Stress
2009196 ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology
2012085 Topology-Aware ESD Checking: A New Approach to ESD Protection
2013115 Thyristor Compact Model for ESD, DC and RF Simulation
20165B4 Spice Modeling Flow for ESD Simulation of CMOS ICs

Imai, S.
2011338 Characteristic of Radiated Electromagnetic Wave by ON/OFF Discharge on Sub-Micron Gap

Imamiya, K.
99225 Design Methodology of a Robust ESD Protection Circuit for STI Process 256Mb NAND Flash Memory

Imholte, J
2012402 A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 61000-4-2 Robustness Without on Board Suppressors

in't Zandt, M.A.A.
2001228 Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection

Ioannou, D.
2009196 ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology
2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations

Isachar, O.
2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)

Ishiguro, S.
86193 ESD Protection Network Evaluation by HBM and CDM (Charged Package Method)

Ishii, H.
2006196 An Active ESD Protection Technique for the Power Domain Boundary in a Deep Submicron IC
Ishizuka, H.
97255  A Study of ESD Protection Devices for Input Pins: Discharge Characteristics of Diode, Lateral-Bipolar and Thyristor under MM and HBM Tests
2008290  A Study of Advanced Technique on RC-Triggered NMOSFET Power Clamp
2009119  An Investigation of Input Protection for CDM Robustness in 40 nm CMOS Technology
2010353  Impact of Difference between Discharging Methods on CDM Testing

Isofuku, S.
2006266  Voltage Dependence of Spark Resistance at Low Voltage ESD in Air and Reed Switch
2012263  System Failures due to an Induced ESD within the System

Isoird, K.
20152A1  An Electrostatic-Discharge-Protection Solution for Silicon-Carbide MESFET

Isomura, N.
2007403  A Study for ESD Robustness of Cascoded NMOS Driver
2008325  CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between IO Test Chips and Product Level

Issakov, V.
2008221  ESD Concept for High-Frequency Circuits

Issaq, E.
93233  ESD Design Methodology

Ito, C.
2001355  Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF Applications
2005033  RF ESD Protection Strategies: Co-design vs. Low-C Protection
2006008  A New Mechanism for Core Device Failure during CDM ESD Events
2006317  A Frequency-Domain VFTLP Pulse Characterization Methodology and its Application to CDM ESD Modeling
2007102  Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System

Ito, S.
2011338  Characteristic of Radiated Electromagnetic Wave by ON/OFF Discharge on Sub-Micron Gap
98199  ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate
99078  Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Ito, Y.
2006112  A Resistive Ferrite Substrate for the GMR Head in Helical-scan Tape Systems

Itoh, T
2013091  Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate

Itou, Y.
2006104  Study on EMI Phenomena for GMR/TMR Head

Ivanova, K.
2014359  Over-Voltage Protection Strategies for LED Based Light Source Systems and other Applications

Iverson, C.
2007257  A Novel On-Chip Protection Circuit for RFICs Implemented in D-Mode pHEMT Technology

Iwahori, J.
2005290  A Study of Relation between a Power Supply ESD and Parasitic Capacitance
2007403  A Study for ESD Robustness of Cascoded NMOS Driver

Iwasaki, A.
97163  Control of Static Charge on Personnel in an Electronics Working Area
<table>
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<tr>
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<td>Contributions to Standardization of Transmission Line Pulse Testing Methodology</td>
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<td>Effect of the n+Sinker in Self-Triggering Bipolar ESD Protection Structures</td>
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<tr>
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</tr>
<tr>
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<tr>
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<tr>
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<tr>
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<tr>
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</tr>
</tbody>
</table>
Jahanzeb, A.
2006024  HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2006222  High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies
2007282  CDM Peak Current Variations and Impact upon CDM Performance Thresholds
2009135  Capacitive Coupled TLP (CC-TLP) and the Correlation with the CDM
2009183  Influence of CDM Tester Plate Size on Discharge Current
2009322  Diode Isolation Concept for Low Voltage and High Voltage Protection Applications
2009377  Protecting Circuits from the Transient Voltage Suppressor's Residual Pulse during IEC 61000-4-2 Stress
2010065  SPICE Simulation Methodology for System Level ESD Design
2010075  TLP Characterization for Testing System Level ESD Performance
2011197  Capturing Real World ESD Stress with Event Detector
2012388  IEC System Level ESD Challenges and Effective Protection Strategy for USB2 Interface

Jahn, S.
20152B2  ESD Induced Functional Upset in Magnetic Sensor ICs

Jainsompron, Y.
2001149  DC Transient Monitoring and Analysis to Prevent EOS in Burn-in Systems

Jain, R.
2009221  IGBT Plugged in SCR Device for ESD Protection in Advanced CMOS Technology
2016A3  Predictive High Voltage ESD Device Design Methodology
20175B1  Shottky LDNMOS for HV ESD Protection

Jalilzeinali, R.
2010381  CDM Effect on a 65 nm SOC LNA

Jang, E.
2007144  HDD-level Electrostatic Discharge (ESD) Failure Voltage of Tunneling Magnetoresistive (TMR) Heads

Jansen, P.H.
2004098  Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies
2006039  Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications
2007053  Voltage Overshoot Study in 20V DeMOS-SCR Devices
2008204  Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD Stress
2010157  SCCF-System to Component Level Correlation Factor
2010293  Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays
2010425  HBM Parameter Extraction and Transient Safe Operating Area

Jaouen, H.
2005170  Impact of the CDM Tester Ground Plane Capacitance on the DUT Stress Level

Jarrett, T.
96123   Interconnects for Device ESD Protection
2001281  A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots
2004200  CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2006240  Trends in External Ionizer Monitoring and Control

Jeamsaksiri, W.
2003242  Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Jeffry, A.
2016A4   Design of ESD Protection for Fault Tolerant Interface Applications with EMC Immunity

Jenei, S.
2002111  Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices
Jenicot, G.  
2009358 IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements

Jensen, M.C.  
81101 Diagnosis and Analysis of Emitter-Base Junction Overstress Damage

Jensen, N.  
2003313 Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications  
2004067 From the ESD Robustness of Products to the System ESD Robustness

Jeon, B.C.  
2002191 ESD Degradation Analysis of Poly-Si N-type TFT Employing TLP (Transmission Line Pulser) Test  
2002362 ESD Characterization of Grounded-Gate NMOS with 0.35 µm/18 V Technology Employing Transmission Line Pulser (TLP) Test

Jeon, C.H.  
2000407 A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process  
2011315 System-Level ESD On-Chip Protection for Mobile Display Driver IC

Jeon, J-S.  
2011315 System-Level ESD On-Chip Protection for Mobile Display Driver IC  
2013240 Gate Bounded Diode Triggered High Holding Voltage SCR Clamp for On-Chip ESD Protection in HV ICs

Jeong, J-Y  
2012091 Minimizing Electrostatic Charge Generation and ESD Event in TFT-LCD Production Equipment  
2012105 Comparing Room Ionization Technologies in FPD Manufacturing

Jeong, S.  
2009211 Effect of Delay in Package Traces on CDM Stress and Peak Current

Jesby, E.S.  
85020 Employee Training for Successful ESD Control

Jezequel, F.  
2010011 TCAD Study of the Impact of Trigger Element and Topology on Silicon Controlled Rectifier Turn-on Behavior

Jiaa, C.  
2005270 Cell Phone GaAs Power Amplifiers: ESD, TLP, and PVS Devices

Jian, S.  
98135 Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Jiang, C.F.  
2006108 Breakdown Evaluation of Ultrathin Barrier Magnetic Tunnel Junctions with V-Ramp Testing  
2007111 Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions

Jiang, H.C.  
2001032 ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device

Jiang, R.  
20168A2 Application Level Investigation of System-Level ESD-Induced Soft Failures

Jianping, F.  
98135 Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Jimenez, J.  
2011082 β Matrix Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology  
2013199 Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology  
20152A2 Self-ESD-Protected Transmission Line Broadband in CMOS28nm UTBB-FDSOI
Jin, J.  
95021 A Novel ESD Protection Technique for Submicron CMOS/BiCMOS Technologies

Jo, C.  
2011274 A Study of a Measurement and Simulation Method on ESD Noise Causing Soft-Errors by Disturbing Signals  
20163B1 Measurement of Discharging Currents through an IC due to the Charged Board Event Using a Shielded Rogowski Coil

Jobava, R.G.  
96203 Numerical Calculation of ESD

Jochum, T.  
20156A4 P2P and RMAP - New Software Tool for Quick and Easy Verification of Power Nets

Johari, P.  
2011300 Efficient Multi-Domain ESD Analysis and Verification of Large SoC Designs

Johnson, C.  
93225 Two Unusual HBM ESD Failure Mechanisms on a Mature CMOS Process

Johnson, C.  
20173B1 An Automated Tool for Minimizing Product Failures Due to Parasitic BJTs and SCRs

Johnson, G.L.  
90263 A Study on the Effectiveness of ESD Smocks

Johnson, L.D.  
2005100 Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies  
2006342 Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators  
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins

Johnson, M.  
2009188 FCDM Measurements of Small Devices  
2009286 Using VFTLP Data to Design for CDM Robustness  
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results  
2012042 Considerations for CDM Standards Alignment: Analysis of a Common Hardware Solution across Different CDM Tester Models  
2012402 A Design Strategy for 8 kV/Contact 15 kV/Air Gap IEC 61000-4-2 Robustness Without on Board Suppressors  
20164A2 JS-002 Module and Product CDM Result Comparison to JEDEC and ESDA CDM Methods

Johnson, M.A.  
81044 An Analysis of Antistatic Cushioning Materials

Johnson, R.A.  
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors  
2001364 Influence of Process and Device Design on ESD Sensitivity of a Silicon Germanium Heterojunction Bipolar Transistor

Johnson, R.L.  
84078 An Experimental Study of the ESD Screening Effectiveness of Anti-Static Bags [BPR]  
91224 Development of a Corporate Standardization Program for ESD Control Materials and Products at Hughes Aircraft Company and Delco

Johnsson, D.  
2008221 ESD Concept for High-Frequency Circuits  
2010239 A TLP-Based Characterization Method for Transient Gate Biasing of MOS Devices in High-Voltage Technologies  
2011360 Study of System ESD Co-design of a Realistic Mobile Board  
2012051 Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester  
2012304 ESD Characterization of Atomically-Thin Graphene  
20152B4 A Passive Coupling Circuit for Injecting TLP-Like Stress Pulses into only one End of a Driver/Receiver System

Jokinen, V.  
20174B1 Qualification Challenges of Footwear and Flooring Systems
Jon, M.B.
99287 Electrostatic Discharge (ESD) Mechanism for Battery Charge Contact Failure in Cordless Phones

Jon, M.C.
87078 The Metallurgical Study of ESD Damage in 256K DRAM Devices
88015 Tape and Reel Packaging - An ESD Concern
88162 A Microwave-Bandwidth Waveform Monitor for Charged-Device Model Simulators [BPP]
89059 A Field-induced Charged-Device Model Simulator [BPP]
94279 Off-Chip Protection: Shunting of ESD Current by Metal Fingers on Integrated Circuits and Printed Circuit Boards
97088 A Robust ESD Event Locator System with Event Characterization
97139 Mitigating Electrostatic Discharge (ESD) in Solid CO: Pellet Cleaning of Printed Wiring Boards and Assemblies

Jonassen, N.
84045 Static-Electric Characterization of Semi-Insulating Materials
85059 The Physics of Air Ionization
86035 The Physics of Charge Neutralization by Air Ions
87209 Ions, Space Charge and Fields
90001 Atmospheric Electricity - Nature's Own ESD
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94221 Do Gases Charge?
95331 Explosions and Static Electricity
98111 Human Body Capacitance: Static or Dynamic Concept?
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry

Jones, A.B.
95013 Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junctions

Jones, C.
2000387 Random GaAs IC's ESD Failures Caused by RF Test Handler

Jordan, D.
2002296 An Automated Electrostatic Discharge Computer-Aided Design System with the Incorporation of Hierarchical Parameterized Cells in BiCMOS Analog and RF Technology For Mixed Signal Applications

Joseph, A.
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors
2005090 The Influence of High Resistivity Substrates on CMOS Latch-up Robustness

Joshi, A.
2010091 An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies
2010111 Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation

Joshi, C.
20156A1 A Full-Chip ESD Simulation Flow

Joshi, S.
2000430 Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies
2002289 Compact Modeling of Vertical ESD Protection NPN Transistors for RF Circuits
2003188 Comprehensive ESD Protection for RF Inputs
2003224 A Study of Vertical SiGe Thyristor Design and Optimization
2003346 Combined TLP/RF Testing System for Detection of ESD Failures in RF Circuits
2003364 Transmission Line Pulsed Waveform Shaping with Microwave Filters

Jou, C-P
2012331 Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process

Joyce, J.L.
91224 Development of a Corporate Standardization Program for ESD Control Materials and Products at Hughes Aircraft Company and Delco
Jozwiak, P.C.
2001001 Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling
2001022 GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes
2002010 High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
2003250 Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

Ju, JH.
2010279 Static Charge Induced Orientation of Liquid Crystals in LCD Panels

Juge, A.
2000251 Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 µm CMOS Process

Juliano, P.A.
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors
2000287 Breakdown and Latent Damage of Ultra-Thin Gate Oxides under ESD Stress Conditions
2000430 Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies
2001326 Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit
2003059 ESD Protection Design Challenges for a High Pin-Count Alpha Microprocessor in a 0.13µm CMOS SOI Technology
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

Jung Kim, W.
2008191 Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer

Jung, S-W
2013323 Electrostatic Control and its Analysis of Roller Transferring Processes in FPD Manufacturing

Jung, Y.I.
2002362 ESD Characterization of Grounded-Gate NMOS with 0.35 µm/18 V Technology Employing Transmission Line Pulser (TLP) Test

Jurczak, M.
2003242 Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets

Kadamati, G.
98208 An Automated Tool for Detecting ESD Design Errors

Kagaoan, J.
2000184 A Case Study on Hidden ESD Events of GMR HGA Dynamic Test Fixture
2001175 A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)

Kagerer, A.
98320 Influence of the Device Package on the Results of CDM Tests – Consequences for Tester Characterization and Test Procedure

Kaku, F.
20164B1 An ESD Control Method Considering the Semiconductor Device Charged Voltage

Kakuda, K.
2006152 Radiated ESD Noise of 5GHz-band from Walkers

Kakuta, S.
2001306 Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group
2002342 Study for Recovery Process of Damaged Al2O3 during Ion Milling to Increase Tolerance to ESD

Kalkner, W.
2001373 Broadband Measurement of ESD Risetimes to Distinguish between Different Discharge Mechanisms

Kalliohaka, T.
2002250 ESD Control Tools for Surface Mount Technology and Final Assembly Lines
<table>
<thead>
<tr>
<th>Author</th>
<th>Publication Year</th>
<th>Title</th>
</tr>
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<tbody>
<tr>
<td>Kallman, R.</td>
<td>94034</td>
<td>Realities of Wrist Strap Monitoring Systems</td>
</tr>
<tr>
<td>Kamat, V.G.</td>
<td>2003017</td>
<td>Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies</td>
</tr>
<tr>
<td>Kamdem, A.</td>
<td>2014393</td>
<td>Electrical Overstress Robustness and Test Method for ICs</td>
</tr>
<tr>
<td>Kamvar, P.</td>
<td>2001216</td>
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</tr>
<tr>
<td>Kan, W.</td>
<td>99070</td>
<td>Stacked PMOS Clamps for High Voltage Power Supply Protection</td>
</tr>
<tr>
<td>Kaneko, M.</td>
<td>96186</td>
<td>One of the Methods of Observing ESD Around Electronic Equipment</td>
</tr>
<tr>
<td>Kaneshiro, M.</td>
<td>2011035</td>
<td>New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications</td>
</tr>
<tr>
<td></td>
<td>2013232</td>
<td>High-Voltage Asymmetrical Bi-Directional Device for System-Level ESD Protection of Automotive Applications on a BICMOS Technology</td>
</tr>
<tr>
<td>Kang, D.G.</td>
<td>2000407</td>
<td>A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process</td>
</tr>
<tr>
<td>Kang, S.M.</td>
<td>92088</td>
<td>Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices</td>
</tr>
<tr>
<td></td>
<td>93083</td>
<td>Studies of EOS Susceptibility in 0.6 mm nMOS ESD I/O Protection Structures</td>
</tr>
<tr>
<td></td>
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<td>96316</td>
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</tr>
<tr>
<td></td>
<td>98281</td>
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<tr>
<td></td>
<td>2000456</td>
<td>Chip-Level Simulation for CDM Failures in Multi-Power ICs</td>
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<tr>
<td>Kang, T.</td>
<td>2011285</td>
<td>A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal ICs</td>
</tr>
<tr>
<td>Kanno, M.</td>
<td>2011088</td>
<td>Origin of It2 Drop Depending on Process and Layout with Fully Silicided ggMOS</td>
</tr>
<tr>
<td>Kao, T.M.</td>
<td>99235</td>
<td>ESD Performance Optimization of Ballast Resistor on Power AlGaAs/GaAs Heterojunction Bipolar Transistor Technology</td>
</tr>
<tr>
<td>Karaskiewicz, R.J.</td>
<td>80059</td>
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</tr>
<tr>
<td></td>
<td>81114</td>
<td>Electrical Overstress Investigations in Modern Integrated Circuit Technologies</td>
</tr>
<tr>
<td>Kärjä, E.</td>
<td>2013084</td>
<td>Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials</td>
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<tr>
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<td>2014206</td>
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<td>20162B3</td>
<td>Charge Relaxation of Slowly Dissipative Polymers</td>
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<tr>
<td></td>
<td>20174B3</td>
<td>Electrostatic Discharge Characteristics of Conductive Polymers</td>
</tr>
<tr>
<td>Karkashadze, D.D.</td>
<td>95095</td>
<td>Calculation and Measurement of Transient Fields of Voluminous Objects</td>
</tr>
<tr>
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<td>96203</td>
<td>Numerical Calculation of ESD</td>
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<tr>
<td>Karp, J.</td>
<td>2008001 Effect of Flip-Chip Package Parameters on CDM Discharge</td>
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<td>2009211 Effect of Delay in Package Traces on CDM Stress and Peak Current</td>
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<td></td>
<td>2011100 Small Footprint ESD Protection of Hot-Swappable I/Os</td>
<td></td>
</tr>
<tr>
<td>Kaschani, K.T.</td>
<td>2006014 ESD Damage due to HBM Stressing of Non-Connected Pins</td>
<td></td>
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<tr>
<td></td>
<td>2011220 The Impact of Electrical Overstress on the Design, Handling, and Application of Integrated Circuits</td>
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<td></td>
<td>20175A3 Correlation Study of Different CDM Testers and CCTL P</td>
<td></td>
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<tr>
<td>Kashani, A.</td>
<td>98139 Electrostatic Hazards of Explosive, Propellant and Pyrotechnic Powders</td>
<td></td>
</tr>
<tr>
<td>Kasuga, K.</td>
<td>2002138 A Study of Electrostatic Discharge on MR Heads in Digital Tape Systems</td>
<td></td>
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<tr>
<td>Kataoka, K.</td>
<td>2003402 Study on Magnetic Instability of GMR Heads Using Quasi-Static Tester with Laser Heating Function</td>
<td></td>
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<td></td>
<td>2004380 Improvement of ESD Robustness and Magnetic Stability by Structure of GMR Head</td>
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<td>2006100 ESD Induced Instability of Pinned Layer in GMR Head</td>
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<td>2007107 Study on High Field Transfer Curves of GMR Heads with Damaged Pinned Layer by ESD</td>
<td></td>
</tr>
<tr>
<td>Katimi, R.</td>
<td>98360 A Study of ESD Sensitivity of AMR and GMR Recording Heads</td>
<td></td>
</tr>
<tr>
<td>Kato, K.</td>
<td>88228 VLSI ESD Phenomenon and Protection</td>
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<td>2004125 ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices</td>
<td></td>
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<tr>
<td>Kato, T.</td>
<td>2010119 Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation</td>
<td></td>
</tr>
<tr>
<td>Katrak, K.K.</td>
<td>95073 Human Body Electrostatic Charge (ESC) Levels: Are They Limited By Corona Bleed Off or Environmental Conditions?</td>
<td></td>
</tr>
<tr>
<td>Katz, J.</td>
<td>2014258 Reflection Control in VF-TLP Systems</td>
<td></td>
</tr>
<tr>
<td>Kaully, E.</td>
<td>2001133 Preparing a Microelectronics Assembly and Test Area for More Sensitive Product</td>
<td></td>
</tr>
<tr>
<td>Kawabe, K</td>
<td>2014197 Visualization Technology to Capture an ESD Event</td>
<td></td>
</tr>
<tr>
<td>Kawamata, K.</td>
<td>2003173 4.5GHz Measurement of Transition Duration and Frequency Spectra Due to Small Gap Discharge as Low Voltage ESD</td>
<td></td>
</tr>
<tr>
<td>Kawamura, T.</td>
<td>84124 EMI Characteristics of ESD in a Small Air Gap--ARP Governs the EMI--</td>
<td></td>
</tr>
<tr>
<td>Kawata, S.</td>
<td>2003389 A Consideration about Ionizer Balance in HGA Process</td>
<td></td>
</tr>
<tr>
<td>Kazmi, S.</td>
<td>96095 Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures</td>
<td></td>
</tr>
<tr>
<td>Kearney, A.</td>
<td>2003070 TLP Analysis of 0.125µm CMOS ESD Input Protection Circuit</td>
<td></td>
</tr>
</tbody>
</table>
Kearney, M.  
2009091 CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps  
2011007 A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction  

Keel, M.-S.  
2013036 ESD-Resilient Active Biasing Scheme for High-Speed SSTL I/Os  
20152A3 CDM-Reliable T-coil Techniques for High-Speed Wireline Receivers

Kelaidis, M.J.  
83021 Air Force Maintenance Program for Electrical Overstress/Electrostatic Discharge (EOS/ESD) Control  

Keller, J.K.  
80073 Protection of MOS Integrated Circuits from Destruction by Electrostatic Discharge [BPP]  

Keller, T.  
2007047 Designing HV Active Clamps for HBM Robustness  
2008099 A Methodology for the ESD Test Reduction for Complex Devices

Kelley, R.H.  
85084 Modeling the Effects of Narrow Impulsive Overstress on Capacitive Test Structures  

Kelly, M.A.  
95175 A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices  
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2003179 Real HBM & MM - The dV/dt Threat  
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins

Kemper, W.  
2003051 Transmission Line Pulsed Photo Emission Microscopy as an ESD Troubleshooting Method  
2006001 System Event Triggered Latch-up in IC Chips: Test Issues and Chip Level Protection Design  
2012414 Characterizing Devices Using the IEC 6100-4-5 Surge Stress

Keough, A.H.  
87142 Static Controlled Thermoformable Sheets from Electron Beam Curing  
90231 The Versatility of Electron Beam Processing, and the Conversion of Medium and High Performance Polymeric Films for ESD Protection

Keppens, B.  
99095 Influence of gate length on ESD-performance for deep sub-micron CMOS technology  
2001461 Contributions to Standardization of Transmission Line Pulse Testing Methodology  
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2005372 SCR Based ESD Protection in Nanometer SOI Technologies  
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2006172 Concept for Bulk Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering  
2008325 CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between IO Test Chips and Product Level  
2010167 On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8 kV Contact System Level  
20175B Low Impedance Dual Bipolar ESD Protection

Ker, M.-D.  
92258 A Novel CMOS ESD/EOS Protection Circuit with Full-SCR Structures  
98072 How to Safely Apply the LVTSCR for CMOS Whole-Chip Protection without being Accidentally Triggered On  
99352 Hardware/Firmware Co-Design in an 8-Bits Microcontroller to Solve the System-Level ESD Issue on Keyboard  
2000266 On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Applications
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<tr>
<td>2001</td>
<td>ESD Protection Design for CMOS RF Integrated Circuits</td>
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<tr>
<td>2003</td>
<td>ESD Protection Design for Giga-Hz RF CMOS LNA with Novel Impedance-Isolation Technique</td>
</tr>
<tr>
<td>2004</td>
<td>Optimization of Broadband RF Performance and ESD Robustness by model Distributed ESD Protection Scheme</td>
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<tr>
<td>2004</td>
<td>Latch-up Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product</td>
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<tr>
<td>2004</td>
<td>Design on Latch-up-Free Power-Rail ESD Clamp Circuit in High-Voltage CMOS ICs</td>
</tr>
<tr>
<td>2005</td>
<td>ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process</td>
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<tr>
<td>2005</td>
<td>Dependences of Damping Frequency and Damping Factor of Bi-Polar Trigger Waveforms on Transient-Induced Latch-up</td>
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<tr>
<td>2005</td>
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<tr>
<td>2009</td>
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<td>2011</td>
<td>PMOS-Based Power-Rail ESD Clamp Circuit with Adjustable Holding Voltage Controlled by ESD Detection Circuit</td>
</tr>
<tr>
<td>2012</td>
<td>Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process</td>
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<tr>
<td>2013</td>
<td>ESD-Transient Detection Circuit with Equivalent Capacitance-Coupling Detection Mechanism and High Efficiency of Layout</td>
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<tr>
<td>2006</td>
<td>Ultra-thin Gate Oxide Reliability in the ESD Time Domain</td>
</tr>
<tr>
<td>2006</td>
<td>Standard ESD Testing of Integrated Circuits</td>
</tr>
<tr>
<td>2011</td>
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<tr>
<td>8310</td>
<td>Modeling and Testing for Second Breakdown Phenomena</td>
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<td>8604</td>
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<tr>
<td>8714</td>
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<td>2000</td>
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</tr>
<tr>
<td>2001</td>
<td>Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies</td>
</tr>
<tr>
<td>2003</td>
<td>Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies</td>
</tr>
<tr>
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</tr>
<tr>
<td>2005</td>
<td>ESD Protection for Advanced CMOS SOI Technologies</td>
</tr>
<tr>
<td>2006</td>
<td>Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology</td>
</tr>
<tr>
<td>2012</td>
<td>Latch-up Characterization and Checking of a 55 nm CMOS Mixed Voltage Design</td>
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<tr>
<td>2016</td>
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<tr>
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<tr>
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2009119  An Investigation of Input Protection for CDM Robustness in 40 nm CMOS Technology
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2001012  5-V Tolerant Fail-Safe ESD Solutions for a 0.18µm Logic CMOS Process

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2007075 Implementation of Dual-Direction SCR Devices in Analog CMOS Process

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2016A4 PNP-eSCR ESD Protection Device with Tunable Trigger and Holding Voltage for High Voltage Applications
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89175 A "Waffle" Layout Technique Strengthens the ESD Hardness of the NMOS Output Transistor

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2003204 ESD Protection Design for Giga-Hz RF CMOS LNA with Novel Impedance-Isolation Technique

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2003291 Exploring a Clean ESD Laminate & Ionic Contamination Methodology

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2010473 The Effect of ESD on the Performance of Magnetic Storage Drives

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2006116  Effect of Electrostatic Discharge on Tunneling Magnetoresistive Sensor

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2000355  Baseline Popping of Spin-Valve Recording Heads Induced by ESD

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2010465 A Study on the Application of On-Chip EOS/ESD Full-Protection Device for TMR Heads

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2000322 ESD Sensitivity of GMR Heads at Variable Pulse Length

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2002183 A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology

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96095 Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures

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2013278  Novel Isolation Ring Structure for Latch-up and Power Efficiency Improvement of Smart Power ICs
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Lin, Y.Y.  
2005307  Problems with IO to all Other IOs ESD Stress Test: Two Case Studies
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89190  Input Protection Design for Overall Chip Reliability

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85010  Font ROS Product an ESD Case History

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90224 | The Application of “Zelec ECP” in Static Dissipative Systems |
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2000097 | A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods |
2009017 | Transient Safe Operating Area (TSOA) Definition for ESD Applications |
2009204 | 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses |
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2014342 | Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting |

Lipka, K.M.

97027 | Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs |
Lisenker, B.
2001398 Improving the Balanced Coaxial Differential Probe for High-Voltage Pulse Measurements
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Lisiak, K.P.
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81192 Prediction of Thin-Film Resistor Burnout

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2001216 Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric Thermal Mapping
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2001415 Electromagnetic Field Generated by Transient Electrostatic Discharges (ESD) from Person Charged with Low Electrostatic Voltage

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20177A2 Analysis and Solution to the ESD Failure Caused by Plasma Protection Diodes for MIM Capacitors

Liu, P.
2001415 Electromagnetic Field Generated by Transient Electrostatic Discharges (ESD) from Person Charged with Low Electrostatic Voltage

Liu, Q.
2011285 A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal Ics
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Liu, R.
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2011323 Machine Model Evaluation and Interconnect Effect Study for TMR HGA

Liu, S.
97132 Measurements of Body Impedance for ESD
97135 Why the Human Body Capacitance is So Large

Liu, W.
2012304 ESD Characterization of Atomically-Thin Graphene

Liu, X.F.
2005090 The Influence of High Resistivity Substrates on CMOS Latchup Robustness

Liu, Y.
2012076 ESD Dynamic Methodology for Diagnosis and Predictive Simulation of HBM/CDM Events

Lizenberger, M.
99241 Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices

Lo, K.F.
2002183 A Study of High Current Characteristics of Devices in a 0.13μm CMOS technology
Lo, T.L.  
97107  Fast Fourier Transform Analysis of Published ESD Waveforms and Narrowband Frequency Domain Measurement of Human ESD

Loayza, J.  
20159A2  EOS Characterization Methodology Applied to Disable Feature of ESD Power Clamps

Lockwood, L.  
89050  A High Voltage Pulse Generator for ESD Simulation

Loh, W.  
2006008  A New Mechanism for Core Device Failure during CDM ESD Events  
2006317  A Frequency-Domain VFTLP Pulse Characterization Methodology and its Application to CDM ESD Modeling  
2007102  Gate Oxide Reliability Characterization in the 100ps Regime with Ultra-fast Transmission Line Pulsing System

Loh, Y.  
92143  MOSFET Drain Engineering for ESD Performance  
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2001062  Analysis and Improved Compact Modeling of the Breakdown Behavior of Sub-0.25 Micron ESD Protection ggNMOS Devices  
2004098  Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies

Lou, L.  
2010065  SPICE Simulation Methodology for System Level ESD Design  
2010075  TLP Characterization for Testing System Level ESD Performance

Lowe, K.D.  
88047  ESD Latency: A Failure Analysis Investigation

Lowe, T.  
2004166  ESD Design Automation for a 90nm ASIC Design System

Lowther, R.  
97083  ESD Sources Pinpointed by Analysis of Radio Wave Emissions

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2013056  Design and Verification of a Novel Multi-RC-Triggered Power Clamp Circuit for On-Chip ESD Protection  
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<td>20164B1</td>
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<td>Maki, T.</td>
<td>88201</td>
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</table>
Maksimovic, D.
2008006 Gate Oxide Protection and ggNMOSTs in 65 nm
2008099 A Methodology for the ESD Test Reduction for Complex Devices
2010083 On-Chip System ESD Protection of FM Antenna Pin

Malberti, P.
2001249 Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

Malec, D.
2003161 A Physical Model to Explain Electrostatic Charging in an Automotive Environment; Correlation with Experimental Approach

Malik, R.J.
93103 Electrostatic Failure of GaAs Planar Doped Barrier Diodes

Malinaric, P.
81049 Cho-Trap, a Novel Voltage Transient Protection Packaging Material

Malinverni, P.
92203 Experimental Comparison of Methods of Charge Decay Measurements for a Variety of Materials

Mallikarjunaswamy, S.
2008083 Potential Barrier Based Clamp: A New Device Structure for Low Voltage Triggering

Malobabic, S.
2009017 Transient Safe Operating Area (TSOA) Definition for ESD Applications
2010249 A New ESD Design Methodology for High Voltage DMOS Applications
20162A4 Low Voltage SCR Clamp with High-VT Reference

Maloney, T.J.
85049 Transmission Line Pulsing Techniques for Circuit Modeling
86166 Contact Injection: A Major Cause of ESD Failure in Integrated Circuits [BPP]
88220 Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model
89078 High Current ESD Damage to MOS I/O Structures Caused by Charged Video Monitor Surfaces and Casings
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2002001 New Considerations for MOSFET Power Clamps
2003027 Methods for Designing Low-leakage Power Supply Clamps
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
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94324 Failure Analysis of CMOS PALs Exhibiting ESD-Type Polygate Short to Substrate Using a State-Of-The-Art IC Diagnostic uProber

Marley, J.  
2001120 Controlling ESD Damage of ICs at Various Steps of Back-End Process

Marom, H.  
2008030 HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike

Marquardt, H.  
2012085 Topology-Aware ESD Checking: A New Approach to ESD Protection

Marreiro, D.  
20175A1 Wafer Level Test Methodology for HV Latch-up Spacing Rules Development in BCD Process Technologies

Marshall, A.  
2005280 ESD Evaluation of the Emerging MuGFET Technology

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82076 Modeling of Current and Thermal Mode Second Breakdown Phenomena  
83108 Modeling and Testing for Second Breakdown Phenomena

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2014393 Electrical Overstress Robustness and Test Method for ICs

Martinez, D.  
99391 ESD Sensitivity Study of GMR Recording Heads with a Flex-On-Suspension Head-Gimbal Assembly

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88077 Test Methods to Characterize Triboelectric Properties of Materials

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97013 Gate Burnout of Small Signal MODFETs at TLP Stress  
97330 Electrical Filamentation in GGMOS Protection Structures

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2004132 Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers  
2005307 Problems with IO to all Other IOs ESD Stress Test: Two Case Studies  
2006001 System Event Triggered Latch-up in IC Chips: Test Issues and Chip Level Protection Design  
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed  
2007283 CDM Peak Current Variations and Impact upon CDM Performance Thresholds  
2008094 Single Pulse CDM Testing and its Relevance to IC Reliability  
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2009377 Protecting Circuits from the Transient Voltage Suppressor's Residual Pulse during IEC 61000-4-2 Stress  
2012414 Characterizing Devices Using the IEC 61000-4-5 Surge Stress

Maschietto, A.  
2001249 Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

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95129 Effectiveness of ESD Training Using Multimedia

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82082 A Probabilistic Estimator for Bounding Transistor Emitter-Base Junction Transient-Induced Failures

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2013214 An Active MOSFET Rail Clamp Network for Component and System Level Protection
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Mathews, D.  80117  Some Design Criteria for Avoiding Second Breakdown in Bipolar Devices

Mathur, G.  20157A1  Design and Optimization on ESD Self-Protection Schemes for 700V LDMOS in High Voltage Power IC

Mathurin, J.  81198  Behavior of Thick-Film Power Resistors Subjected to Large Momentary Overloads

Matsil, I.S.  97205  What Every ESD Engineer Needs to Understand About Patents (Invited Paper)

Matsugi, J.  2003382  ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads

Matsumashi, K.  98218  Measures against Electrostatic Destruction of Electronic Devices at Electronic Equipment Assembly Shops

Matsui, J.  2013091  Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate

Matsui, M.  87227  Electromagnetic Wave Generation from Electrostatic Discharge between Charged Human's Body and Earthed Electrode

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Matsuo, Y.  87153  Shield Effect of Electrically Conductive Materials against Electromagnetic Waves Radiated by Electrostatic Discharge

Mauran, N.  2007304  Characterization and Modeling Methodology for IC's ESD Susceptibility at System Level Using VF-TLP Tester

Maurer, L.  2009165  Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System

Mauer, N.  2013155  20GHz On-Chip Measurement of ESD Waveform for System Level Analysis

Mauran, N.  2013258  Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement

Mauran, N.  20154B1  TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators

May, J.E.  83168  Metal Oxide Varistors for Transient Protection of 3 to 5-Volt Integrated Circuits

May, J.T.  94085  Charged Device Damage of PLCCs inside an Antistatic Shipping Tube - A Case History

Mavinkurve, A.  2011210  Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment
Mayerhofer, M.T.
- 2006054 ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive
- 2008221 ESD Concept for High-Frequency Circuits
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McAleer, R.E.
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- 80054 Identification of Latent ESD Failures
- 80189 An Effective ESD Awareness Training Program
- 81014 Analysis of Electrostatic Discharge Failures
- 82041 Latent ESD Failures [BPP]
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- 2008094 Single Pulse CDM Testing and its Relevance to IC Reliability
- 2009183 Influence of CDM Tester Plate Size on Discharge Current

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- 86069 Reversible Charge Induced Failure Mode of CMOS Matrix Switch

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- 79168 Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature

McKenzie, R.
- 98328 Current Transients and the Guzik: A Case Study and Methodology for Qualifying a Spin Stand for GMR Testing
McKinley, W.  
2009247 A Study of ESD Protection Means of Cabled GMR Sensors

McLain, D.  
2006001 System Event Triggered Latch-up in IC Chips: Test Issues and Chip Level Protection Design

McMahon, E.J.  
79027 Proposed MIL-STD and MIL-HDBK for an Electrostatic Discharge Control Program -- Background and Status --

McPhee, R.A.  
85045 ESD Design Considerations for ULSI  
86173 Thick Oxide Device ESD Performance under Process Variations [BPR]

McVittie, J.  
90182 Applications of a New Wafer Surface Charge Monitor

Medhat, D.  
2013361 Using Static Voltage Analysis and Voltage-Aware DRC to Identify EOS and Oxide Breakdown Reliability Issues  
20153A3 A Comprehensive ESD Verification Flow at Transistor Level for Large SoC Designs

Meeks, T.  
20173B3 HV Latch-up - Power Analog ICs Co-Design with Block Level Verification

Meeuwsen, S.  
99011 Investigations on Double-Diffused MOS (DMOS) transistors under ESD zap conditions

Mellberg, H.  
80225 Measurement of Fast Transients and Application to Human ESD  
81001 A Closer Look at the Human ESD Event  
91010 Recent Developments in ESD Waveform Evaluation

Meneghesso, G.  
2001102 Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology  
2001249 Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes  
2006274 Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices  
2007058 CDM Circuit Simulation of a HV Operational Amplifier Realized in 0.35µm Smart Power Technology  
2007264 ESD Robustness of AlGaN/GaN HEMT Devices  
2008059 Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques  
2008211 Novel 190V LIGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate  
2008272 EOS/ESD Sensitivity of Functional RF-MEMS Switches  
2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness  
2009257 EOS/ESD Sensitivity of Phase-Change-Memories  
2010433 A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectic Charging, and Realistic  
2011171 A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts  
2014282 Anti-Series GgNMOS ESD Clamp for Space Application IC's

Meng, K-H  
2012290 The Need for Transient I-V Measurement of Device ESD Response  
2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps  
2014232 A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry  
20156A3 Fast Circuit Simulator for Transient Analysis of CDM ESD

Mensing, R.W.  
79198 Statistical Failure Analysis of Military Systems for High Altitude EMP
Mercha, A.
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Mergens, M.P.J.
98290  Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
99001  Analysis and Compact Modeling of Lateral DMOS Power Devices under ESD Stress Conditions
2000446  ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior
2001001  Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling
2001022  GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes
2002010  High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design
2004289  ESD Protection Solutions for High Voltage Technologies
2006054  ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive

Merlo, L.
20173B2  EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC’s

Merrill, R.
93233  ESD Design Methodology

Mertens, R.
2012373  A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting
2013125  Separating SCR and Trigger Circuit Related Overshoot in SCR-based ESD Protection Circuits
2013319  Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress
2014242  Chip-Level ESD-Induced Noise on Internally and Externally Regulated Power Supplies
2015808  Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit

Mettler, S.
98290  Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
99001  Analysis and Compact Modeling of Lateral DMOS Power Devices Under ESD Stress Conditions
2000446  ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior
2003088  Characterization and Modeling of Transient Device Behavior Under CDM ESD Stress
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2004107  Study of CDM Specific Effects for a Smart Power Input Protection Structure
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Metz, W.J.
2001281  A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

Meuse, T.
98290  Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
98301  Investigation into Socketed CDM (SDM) Tester Parasitics
99178  Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
2004141  Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
2004153  Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps
2006353  HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
2008030  HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike
2008040  VF-TLP Round Robin Study, Analysis and Results
2010359  CDM2 - A New CDM Test Method for Improved Test Repeatability and Reproducibility
2012032  Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2013261  Activities Towards a New Transient Latch-up Standard

Meyer, R.L.
2003414  Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies
Meyerson, B.  
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors

Miao, G  
2013140 On-Chip System Level ESD Protection for Class G Audio Power Amplifiers  
2013209 HBM ESD Protection for Class G Power Amplifiers

Mignoli, F.  
2001102 Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology

Milburn, R.T.  
81101 Diagnosis and Analysis of Emitter-Base Junction Overstress Damage  
90151 Failure Analysis of Electrostatic Sensitive ECL Gate Arrays  
93123 EOS Induced Polysilicon Migration in VLSI Gate Arrays

Mileham, J.R.  
84085 A Material Evaluation Program for Decorative Static Control Table Top Laminates

Millar, S.  
2010217 CDM Damage due to Automated Handling Equipment  
2010233 Comparison of Methods of Evaluation of Charge Dissipation from AHE Soak Boats

Miller, D.  
2010317 Problematic Natural Gas Power Plant Pumping/Irrigation

Miller, J.W.  
97356 Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology  
2000308 Engineering the Cascoded NMOS Output Buffer for Maximum Vt1  
2001082 Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies  
2003017 Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies  
2004255 Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies  
2004280 Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications  
2005070 ESD Protection for Advanced CMOS SOI Technologies  
2006046 Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe  
2006186 Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology  
2008030 HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike  
2009091 CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps  
2011007 A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction  
2011076 When Good Trigger Circuits Go Bad: A Case History  
2012254 Sampling Pin Approaches for ESD Test Applications  
2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps  
2014232 A Co-optimization Methodology on ESD Robustness and Functionality for Pad-Ring Circuitry  
20156A2 A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures

Miller-Lynch, T.  
99019 Wide Range Control of the Sustaining Voltage of ESD Protection Elements Realized in a Smart Power Technology

Min, K.  
2005100 Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies  
2006342 Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators

Minami, T.  
87137 Static Electricity Elimination Using Conductive Fiber by Dyeing

Minear, R.L.  
79188 The Phantom Emitter - an ESD-Resistant Bipolar Transistor Design and its Applications to Linear Integrated Circuits
Minegishi, S. 2003173 4.5GHz Measurement of Transition Duration and Frequency Spectra Due to Small Gap Discharge as Low Voltage ESD

Minixhofer, R. 2011123 Process Variation Aware ESD Design Window Considerations on a 0.18 µm Analog, Mixed-Signal High Voltage Technology 2012298 ESD Induced Leakage Current Increase of Diffused Diodes

Minor, J.L. 94193 Simulation of a System Level Transient-induced Latch-Up Event

Mishra, A. 20162A2 Unique Current Conduction Mechanism through Multi Wall CNT Interconnects under ESD Conditions

Mishra, R. 2009069 Technology Scaling of Advanced Bulk CMOS On-Chip ESD Protection 2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations 2011022 Technology Scaling Effects on the ESD Performance of Silicide-Blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies 2012319 Effect of Embedded-SiGe (eSiGe) on ESD TLP and VFTLP Characteristics of Diode-Triggered Silicon Controlled Rectifiers 2014021 ESD Device Performance Analysis in a 14nm FinFET Soi CMOS Technology: Fin-based versus Planar-based 20151A2 Design and Optimization of ESD Lateral NPN Device in 14nm FinFET Soi CMOS Technology

Mistry, K.R. 89121 On Latency and the Physical Mechanisms Underlying Gate Oxide Damage during ESD Events in N-Channel MOSFETs 90214 Dependence of Input ESD Failure Thresholds on IC Design Style 92250 ESD Protection in a 3.3V Sub-Micron Silicided CMOS Technology [BPR] 94113 Circuit Interactions during Electrostatic Discharge

Mitani, S. 79088 Failure Analysis of Microcircuits Subjected to Electrical Overstress

Mitai, S. 99078 Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Mitard, J. 2012001 ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling 20151A4 ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies

Mitchell, T. 2014342 Overcoming Multi Finger Turn-on in HV DIACs Using Local Poly-Ballasting 20173B3 HV Latch-up - Power Analog ICs Co-Design with Block Level Verification

Mitra, S. 2006179 Design and Characterization of a Multi-RC-Triggered MOSFET-based Power Clamp for On-Chip ESD Protection 2007250 Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies 2008228 Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies 2008312 ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology 2009084 Impact of Stress Engineering on High-k Metal Gate ESD Diodes in 32 nm SOI Technology 2009196 ESD Time-Domain Characterization of High-k Gate Dielectric in a 32 nm CMOS Technology 2009334 Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line 2010091 An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies 2010111 Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation 2010177 Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations 2010197 Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies 2011294 A Current Density Analysis Tool to Identify BEOL Fails Under ESD Stress 2012068 Advanced ESD Tool Flow, Testing, and Design Verification Results
Identification and Verification of BEOL Metal Fails due to ESD Stress using Current Density Analysis Tool

3D Integration ESD Protection Design and Analysis

Miyamoto, K.
New Failure Mechanism Due to Non-Wired Pin ESD Stressing

Miyamoto, Y
Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate

Miyazaki, T.
Ultra-Low Standby Current ESD Clamp MOSFET with P/N Hybrid Gate

Mizoh, Y.
ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads
Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process

Mo, M.
Breakdown Behavior of TMR Head in ESD Transients

Mocuta, A.
VFTLP Characteristics of ESD Diodes in Bulk Si Gate-all-Around Vertically Stacked Horizontal Nanowire Technology

Moens, P.
Effect of the n+Sinker in Self-Triggering Bipolar ESD Protection Structures
Design and Characterization of a High Voltage SCR with High Trigger Current
IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements

Mogami, T.
Impact of Difference between Discharging Methods on CDM Testing

Mohammadnejad, M
Auditing of a Class 0 Facility

Mohan, N.
On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism

Mohan, V.
CDM Effect on a 65 nm SOC LNA

Mohn, R.
High Holding Current SCRs (HHI-SCR) for ESD Protection and Latch-up Immune IC Operation
Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

Money, R.J.
Wire Bonding Tip Study for Extremely ESD Sensitive Devices

Monfray, S.
Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

Monma, H.
ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate
Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices

Monnerau, N.
Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation
ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
Investigating the Probability of Susceptibility Failure within ESD System Level Consideration

Monstream, J.
An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies
Montanaro, J.
98086  Cross Reference ESD Protection for Power Supplies

Montoya, J.A.
96145  Developing an Exit Charge Specification for Production Equipment
2000394  A Study of the Mechanisms for ESD Damage to Reticles
2005229  Unifying Factory ESD Measurements and Component ESD Stress Testing

Montstream, J.
2012068  Advanced ESD Tool Flow, Testing, and Design Verification Results

Moon, H.S.
2002233  ESD Protection Materials Using Conductive Polymers

Moon, K.C.
2002191  ESD Degradation Analysis of Poly-Si N-type TFT Employing TLP (Transmission Line Pulser) Test

Moon, K.S.
2002233  ESD Protection Materials Using Conductive Polymers

Moon, M.G.
79104  ESD Susceptibilities of High Performance Analog Integrated Circuits

Moore, B
2012161  Latch-up Characterization and Checking of a 55 nm CMOS Mixed Voltage Design

Moore, C.
99309  ESD Testing of GMR Heads as a function of Temperature
2000217  Measuring and Specifying Limits on Current Transients and Understanding Their Relationships to MR Head Damage
2000343  A Comparison of Quasi-Static Characteristics and Failure Signatures of GMR Heads subjected to CDM and HBM ESD Events

Moosa, M
2013313  Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps

More, V.
2011250  Interrogation of Damage-State in Lead-free Electronics under Sequential Exposure to Thermal Aging and Thermal Cycling

Morena, E.
2003088  Characterization and Modeling of Transient Device Behavior under CDM ESD Stress
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Morgan, I.H.
88155  A Method of Calibration for Human Body Model ESD Testers to Establish Correlatable Results
95289  The Correlation between Latch-Up Phenomenon and Other Failure Mechanisms
99178  Developing a Transient Induced Latch-up Standard for Testing Integrated Circuits
99190  Transient Latch-Up Using an Improved Bi-polar Trigger

Morimura, H.
2004075  Evaluation of ESD Hardness of Fingerprint Sensor LSIs

Morin, G.
92039  ESD - A Problem beyond the Discrete Component

Morinaga, A.
2003402  Study on Magnetic Instability of GMR Heads Using Quasi-Static Tester with Laser Heating Function

Morishita, Y.
2002006  New ESD Protection Circuits Based on PNP Triggering SCR for Advanced CMOS Device Applications
2005400  A PNP-Triggered SCR with Improved Trigger Techniques for High-Speed I/O ESD Protection in Deep Sub-Micron CMOS LSIs
2007037  Layout Technique to Alleviate Soft Failure for Short Pitch Multi Finger ESD Protection Device
2007376  A Low-Leakage SCR Design Using Trigger-PMOS Modulations for ESD Protection
2009119  An Investigation of Input Protection for CDM Robustness in 40 nm CMOS Technology
Impact of Difference between Discharging Methods on CDM Testing
Area-Efficient ESD Design Using Power Clamps Distributed Outside I/O Cell Ring

Morita, T.
A Study of Relation between a Power Supply ESD and Parasitic Capacitance
A Study for ESD Robustness of Cascoded NMOS Driver

Morris, G.
Electrostatic Failure of X-Band Silicon Schottky Barrier Diodes

Morris, J.
Input Protection Design for Overall Chip Reliability

Morris, S.
Electrostatic Sensitivity of Various Input Protection Networks

Morrison, E.D.
Vanadium Pentoxide Based Antistatic Coatings

Morrison, S.
TLP Characterization for Testing System Level ESD Performance
CDM Events in Automated Test Handlers and Environmental Testing - A Case History

Mortini, P.
Impact of I/O Buffer Configuration on the ESD Performance of a 0.5 µm CMOS Process
Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 µm CMOS Process

Moseley, R.
On-Chip Sensors to Measure Level of Transient Events

Moser, R
Correlation Study of Different CDM Testers and CCTLP

Moss, Ii, R.Y.
Ionization - Science or Magic?
Sources of Error in Resistance Measurements on Conductive Flooring

Motley, G.W.
Bi-Modal Triggering for LVSCR ESD Protection Devices

Motz, M.
ESD Induced Functional Upset in Magnetic Sensor ICs

Mouthaan, A.J.
Simulation of Thermal Runaway during ESD Events

Mouthaan, T.
Physics of Electro-Thermal Effects in ESD Protection Devices
Investigations on Double-Diffused MOS (DMOS) transistors under ESD zap conditions
Modeling Substrate Diodes under Ultra High ESD Injection Conditions

Mrascarica, Z.
ESD Protection for the High-Voltage CMOS Technologies
Designing HV Active Clamps for HBM Robustness
Gate Oxide Protection and ggNMOSTs in 65 nm

Mueller, R.
Grounding Personnel via the Floor/Footwear System

Muhammad, M.
Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13µm CMOS Logic
Design Automation to Suppress Cable Discharge Event (CDE) Induced Latch-up in 90nm CMOS ASICs
PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latch-up Robustness

An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies

Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation

A Current Density Analysis Tool to Identify BEOL Fails Under ESD Stress

Advanced ESD Tool Flow, Testing, and Design Verification Results

Identification and Verification of BEOL Metal Fails due to ESD Stress using Current Density Analysis Tool

Muhonen, K.

2008040 VF-TLP Round Robin Study, Analysis and Results
2008132 Delivering IEC 61000-4-2 Current Pulses through Transmission Lines at 100 and 330 Ohm System Impedances
2009387 Human Metal Model (HMM) Testing, Challenges to Using ESD Guns
2009396 Failure Detection With HMM Waveforms
2009419 Characterization and Simulation of Real-World Cable Discharge Events
2012060 HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform

Mulcahy, B.D.

88137 Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses

Müller, C.

2004067 From the ESD Robustness of Products to the System ESD Robustness

Müller-Lynch, T.

99241 Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices

Muñoz, J.L.

2000060 Detecting ESD Events using a Loop Antenna
2006231 A Novel Ionizer Design with Both DC and AC High Voltage Bias

Murakami, T.

96327 Study of ESD Quench Effects by Air Ionization
96365 Electrostatic Problems in TFT-LCD Production and Solutions Using Ionization
2012191 Test Method Recommendations for the Evaluation of Packaging Materials Used for Small Static Sensitive Electronic Components

Murasaki, N.

87227 Electromagnetic Wave Generation from Electrostatic Discharge between Charged Human's Body and Earthed Electrode

Murata, S.

90111 The ARC Problem and Voltage Scaling in ESD Human Body Model

Murello, A.F.

86156 Study of Antistatically Coated Shipping Tubes Using Static Decay and Triboelectric Tests

Murray, K.D.

88195 Hood Ionization in Semiconductor Wafer Processing: An Evaluation
89018 Ozone and Small Particle Production by Steady State DC Hood Ionization: An Evaluation
90036 Clean Corona Ionization
91038 Technique for Generating Contamination-Free Ionized Air Using Focused Laser Light

Muschitiello, M.

94292 A Method for the Characterization and Evaluation of ESD Protection Structures and Networks

Musshoff, C.

97366 Does the ESD-Failure Current Obtained by Transmission Line Pulsing Always Correlate to Human Body Model Tests?

Muthukrishnan, S.

2007257 A Novel On-Chip Protection Circuit for RFICs Implemented in D-Mode pHEMT Technology

Muto, H.

2007198 Systematic Approach for the Electrification Suppression Using the Effective Work Function
Mykkanen, C.F.
81208   Potential ESD Hazards Associated with Explosive Primers
83067   The Room Air Ionization System, a Better Alternative than 40% Relative Humidity [BPR]

Myny, S.
20161A1  ESD Protection Design in a-IGZO TFT Technologies
Myoung, R.  
2014179  System-Level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation

Naem, A.  
99095  Influence of gate length on ESD-performance for deep sub-micron CMOS technology

Nagata, H.  
2015RCJ  Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply RCJ

Nagata, M.  
2014061  CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus

Nakaei, T.  
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor  
2006039  Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications  
2007053  Voltage Overshoot Study in 20V DeMOS-SCR Devices  
2007089  Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis  
2007158  Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions  
2008295  Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets  
2009364  Self-Protection Capability of Power Arrays  
2009405  On-Wafer Human Metal Model Measurements for System-Level ESD Analysis  
2013091  Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate

Nakagawa, D.  
20166A1  Ultra-Low Standby Current ESD Clamp MOSFET with P/N Hybrid Gate

Nakajima, T.  
2003389  A Consideration about Ionizer Balance in HGA Process

Nakamura, K.  
2003382  ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads  
2004016  Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process

Nakamura, Y.  
87096  Energy Dissipation in Electrostatic Spark Discharge, and its Distance Effects

Nakanishi, C.  
2006260  Solution of Destructive Separation Charge Generation

Nakanishi, K.  
98128  Electrostatic Build Up on Metal Balls Due to Sliding Contact with Insulating Materials and How to Reduce it with Carbon-Fiber Reinforced Plastics - Electrostatic Discharge in Pachinko Parlors

Nakano, T.  
2003382  ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads  
2004016  Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process

Nakauchi, E.  
2000048  ESD Immunity in System Designs, System Field Experiences and Effects of PWB Layout

Nakaya, K.  
2011053  Source Engineering for ESD Robust NLDMOS

Nakos, J.  
98151  Semiconductor Process and Structural Optimization of Shallow Trench Isolation- Defined and Polysilicon – Bound Source/Drain Diodes

Namaguchi, T.  
98245  Wrist Strap Designs and Comparison of Test Results According to MIL-PRF-87893 and ANSI EOS/ESD Association S1.1
Nandy, A.
2011274 A Study of a Measurement and Simulation Method on ESD Noise Causing Soft-Errors by Disturbing Signals

Napombejara, D.
2005344 EOS Exposure of Magnetic Heads and Assemblies in Automated Manufacturing

Narayan, R.
2005100 Chip Level Layout and Bias Considerations for Preventing Neighborhood I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies
2006342 Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins

Narita, K.
99116 A Simulation Analysis of Quarter-Micron CMOS LSI Input Circuit Behavior under CDM-ESD for Protection Device Improvement
20166A4 CDM Protection Design using Internal Power Node for Cross Power Domain in 16nm CMOS Technology

Narkis, M.
98001 New Injection Moldable ESD Compounds Based on Very Low Carbon Black Loadings
99251 Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing
2000139 Controlling ESD and Cleanliness by Using New Thermoplastic Compounds for Injection Molded and Corrugated Packaging Products

Naticchioni, S.M.
88092 Standardized Qualification and Verification Procedures for Electrostatic Discharge (ESD) Protective Materials

Natori, S.
2003402 Improvement of ESD Robustness and Magnetic Stability by Structure of GMR Head
2006104 Study on EMI Phenomena for GMR/TMR Head

Neelakantaswamy, P.S.
85092 Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstressings: A Model
85092 Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Wunsch-Bell Model
87158 A Novel On-Chip ESD Protection Device Using Static Induction Transistor Principle

Neitzert, H.C.
97018 Influence of the Device Geometry and Inhomogeneity on the Electrostatic Discharge Sensitivity of InGaAs/InP Avalanche Photodetectors

Nelsen, D.E.
86188 Design and Test Results for a Robust CMOS VLSI Input Protection Network

Nelsen, L.
2000193 Advances in Magneto Optical Static Event Detector Technology

Neteler, J.G.
97263 Clean Room ESD Packaging Overview
2003291 Exploring a Clean ESD Laminate & Ionic Contamination Methodology

Neve, C R.
20155A1 ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package

Never, J.M.
92277 Shallow Trench isolation Double-Diode Electrostatic Discharge Circuit and Interaction with DRAM Output Circuitry
95273 Failure Analysis of Shallow Trench Isolated ESD Structures
96101 Linewidth Control Effects on MOSFET ESD Robustness

Newberg, C.
2001153 Measurement of Electrostatic Generation in Semiconductor Processing Fluids as a Result of Pumping Through Insulative Pumps
2001281 A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots
CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
Study of "Hot Spots" Arising from Non-Homogeneity in the Micro-Structures of Dissipative Materials
Trends in External Ionizer Monitoring and Control
Carbon Nanotube Plastic - Packaging Materials for Class 0 Device ESD Protection

Newburg, C.
Analysis of the Electrical Field Effects of AC and DC Ionization Systems for MR Head Manufacturing

Ng, K.K.
ESD Concerns in Sawing Wafers with Discrete Semiconductor Devices
Influence of Machine Configuration on EOS Damage during Wafer Cleaning Process

Ngan, P.
Automatic Layout Based Verification of Electrostatic Discharge Paths
Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results

Ngo, S.
CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps
A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction

Nguyen, C.
Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junctions

Nguyen, D.
New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications

Nguyen, K.
CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps

Nguyen, V.
A Miniature Charged Plate for Testing of Charge Accumulation in Hard Disk Drives

Nicholl, H.
Mitigating Electrostatic Discharge (ESD) in Solid CO₂, Pellet Cleaning of Printed Wiring Boards and Assemblies

Nichols, G.
Room Ionization: Can It Significantly Reduce Particle Contamination?

Niemela, S.
Characterizing Slowly Dissipative Materials

Niemesheim, J.
Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
Characterization and Simulation of Real-World Cable Discharge Events
On the Characterization of ESD Properties of JEDEC Trays
Do Devices on PCBs Really See a Higher CDM-like ESD Risk?
Practical HBM Testing with Statistical Pin Combinations
Risk Assessment of Cable Discharge Events

Niggemeier, W.
Grounding Personnel via the Floor/Footwear System

Nikolaidis, T.
Impact of I/O Buffer Configuration on the ESD Performance of a 0.5 µm CMOS Process

Nimmo, R.
ESD Protection of BICMOS Integrated Circuits Which Need To Operate in the Harsh Environments of Automotive Or Industrial

Nishihata, N.
New ESD Control Material Based on Special Carbon

Nishimae, I.
An Advanced ESD Test Method for Charged Device Model
Nishimura, A.
90111 The ARC Problem and Voltage Scaling in ESD Human Body Model

Nishioka, K.
2007107 Study on High Field Transfer Curves of GMR Heads with Damaged Pinned Layer by ESD

Noel, P.H.
83154 EOS or ESD: Can Failure Analysis Tell the Difference?

Nothier, N.
2002281 Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN
2002348 Investigations for a Smart Power and Self-Protected Device under ESD Stress through Geometry and Design Considerations
2006069 Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology
2007304 Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester
2009165 Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
2009273 ESD Events in SiN RF-MEMS Capacitive Switches
2011329 ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
2011343 Investigating the Probability of Susceptibility Failure within ESD System Level Consideration
2013155 20GHz On-Chip Measurement of ESD Waveform for System Level Analysis
2013258 Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement
2014053 Novel 3D Back-to-Back Diodes ESD Protection
20154B1 TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators
20167A3 From Quasi-Static to Transient System Level ESD Simulation: Extraction of Turn-on Elements

Noll, C.G.
97195 Comparison of Germanium and Silicon Needles as Emitter Electrodes for Air Ionizers
99131 Balanced Static Elimination in Variable Ion Mobility Environments

Nomura, C.
2004361 Electrostatic Discharge (ESD) Protection of Giant Magneto-resistive (GMR) Recording Heads with a Silicon Germanium Technology

Nomura, T.
2005290 A Study of Relation between a Power Supply ESD and Parasitic Capacitance

Noras, M.A.
2003265 Ion Imbalances on the Ionizer Controlled Work Surface
2005357 A Miniature Charged Plate for Testing of Charge Accumulation in Hard Disk Drives
2006240 Trends in External Ionizer Monitoring and Control
2008142 Static Control Standards in the Semiconductor Industry

Nordin, D.
2000205 HDA-Level ESD Testing of Giant Magnetoresistive (GMR) Recording Heads

Notermans, G.H.J.
97221 On the Use of N-Well Resistors for Uniform Triggering of ESD Protection Elements
98096 High Voltage Resistant ESD Protection Circuitry for 0.5 μm CMOS OTP/EPROM Programming Pin
98170 Pitfalls When Correlating TLP, HBM, and MM Testing
2006077 ESD Protection for the High-Voltage CMOS Technologies
2007047 Designing HV Active Clamps for HBM Robustness
2008006 Gate Oxide Protection and ggNMOSTs in 65 nm
2008099 A Methodology for the ESD Test Reduction for Complex Devices
2010083 On-Chip System ESD Protection of FM Antenna Pin
20154A2 An Off-Chip ESD Protection for High-Speed Interfaces
20157B1 Air-Discharge Testing of Single Components
20166B3 Gun Tests of a USB3 Host Controller Board

Nouet, P.
2003233 STMSCR: A New Multi-Finger SCR-Based Protection Structure against ESD
2005053 Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology
2006166 Partially Depleted SOI Body-Contacted MOSFET- Triggered Silicon Controlled Rectifier for ESD Protection
2007165 Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain
2008067 A Physics-Based Compact Model for ESD Protection Diodes under Very Fast Transients

Nuebel, J.
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79027  Proposed MIL-STD and MIL-HDBK for an Electrostatic Discharge Control Program -- Background and Status --

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2006087  Operation Analysis and Implementation of CMOS Compatible Vertical Bipolar ESD Protection Devices for Automotive Applications
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2007037  Layout Technique to Alleviate Soft Failure for Short Pitch Multi Finger ESD Protection Device
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2010119  Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation
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20166A4  CDM Protection Design using Internal Power Node for Cross Power Domain in 16nm CMOS Technology

Okuyama, K.

97255  A Study of ESD Protection Devices for Input Pins: Discharge Characteristics of Diode, Lateral-Bipolar and Thyristor under MM and HBM Tests

Oliver, D.

2001096  Automatic Layout Based Verification of Electrostatic Discharge Paths

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96062  A Combined Socketed and Non-Socketed CDM Test Approach for Eliminating Real-World CDM Failures
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98332  Ion Milling Induced ESD Damage during MR Head Fabrication

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2006152  Radiated ESD Noise of 5GHz-band from Walkers

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2014197  Visualization Technology to Capture an ESD Event

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91083  A Characterization of Components for an Optimized CMOS Input Protection System

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2013183  A Systematic Method for Determining Soft-Failure Robustness of a Subsystem
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2001175  A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)

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88092  Standardized Qualification and Verification Procedures for Electrostatic Discharge (ESD) Protective Materials

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2003414  Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies

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2007318  Simulation and Physics of Charged Board Model for ESD

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2005203  ESD Control in Automated Placement Process

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2009257  EOS/ESD Sensitivity of Phase-Change-Memories

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2011100  Small Footprint ESD Protection of Hot-Swappable I/Os

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98118  Electrostatic Discharges from Charged Particles Approaching a Grounded Surface

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2001050  Performance of Fiber Based ESD Protective Packaging

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2010091  An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies  
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20171A3 Enhanced nFinFET ESD Performance

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80023 Electrostatic Discharge (ESD) Monitor Design

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95295 Melt Filaments in n+pn+ Lateral Bipolar ESD Protection Devices
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2012105 Comparing Room Ionization Technologies in FPD Manufacturing

Park, H.
95021 A Novel ESD Protection Technique for Submicron CMOS/BICMOS Technologies

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2000407 A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process

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2008125 The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
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20165B1 Empirical ESD Simulation Flow for ESD Protection Circuits Based on Snapback Devices
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2001272 Electronic Part Damage by Antistat Vapor

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95229 Electrically Conductive Polypropylene-Polyaniline Blend in ESD Protection

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83134 ESD Evaluation of Radiation-Hardened, High Reliability CMOS and MNOS ICs

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96032 A Low Cost Visual Indicator for Detecting Ground Connection Failure of CRT Filter Screens

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20173A3 Characterizing ESD Stress Currents in Human Wearable Devices
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2000233 Investigation of ESD Transient EMI Causing Spurious Clock Track Read Transitions during Servo-Write

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2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
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85024  A Design Methodology for ESD Protection Networks

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2004248  ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure  
2005421  SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies  
2007185  Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI  
2008235  ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology

Pellinen, D.  
80225  Measurement of Fast Transients and Application to Human ESD

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82049  A Survey of EOS/ESD Data Sources  
85100  A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models with

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2000379  Measurement Technique Developed to Evaluate Transient EMI in a Photo Bay with and Without Air Ionization  
2003259  Creating and Measuring Photomask Damage

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20176B2  Novel SCR Structure for Power Supply Protection in FinFET Technology

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2008272  EOS/ESD Sensitivity of Functional RF-MEMS Switches

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2005131  Guard Rings:  Theory, Experimental Quantification and Design

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93029  Electrostatic Discharge Analyses for Spacecraft in Geosynchronous Orbit

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2001149  DC Transient Monitoring and Analysis to Prevent EOS in Burn-In Systems

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81120  An Overview of Electrical Overstress Effects on Semiconductor Devices
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20155A1  ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package

Plaster, J.S.
87010  ESD Control in the Automotive Electronics Industry - a Case Study [BPP]

Pogany, D.
99241  Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices
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2002387  Investigation of ESD Protection Elements under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry
2003116  Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness
2003313  Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
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2011059  ESD Robust DeMOS Devices in Advanced CMOS Technologies
2011147  HBM ESD Robustness of GaN-on-Si Schottky Diodes

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2001192  Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

Polewski, M.
2010341  Pitfalls for CDM Calibration Procedures

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89167  Improving the ESD Failure Threshold of Silicided NMOS Output Transistors by Ensuring Uniform Current Flow

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2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
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2000085 TLP Calibration, Correlation, Standards, and New Techniques
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2006032 Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies

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79022 The Generation of Electrostatic Charges in Silicone Encapsulants during Cyclic Gaseous Pressure Tests

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2003034 Real-World Charged Board Model (CBM) Failures
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2011329 ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver

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2012181 Triboelectrification of Static Dissipative Materials
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2010433  A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic

Ritter, H-M.  
2009308  Latent Damage Due to Multiple ESD Discharges  
20154A2  An Off-Chip ESD Protection for High-Speed Interfaces  
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20166B3  Gun Tests of a USB3 Host Controller Board

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2005212  Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

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<td>Ryl, P.</td>
<td>85100 A Comparison of Discrete Semiconductor Electrical Overstress Permanent Damage Threshold Predictions from Various Models</td>
</tr>
<tr>
<td>Ryser, H.</td>
<td>90045 The Relationship between ESD Test Voltage and Personnel Charge Voltage</td>
</tr>
<tr>
<td>Sachdev, M.</td>
<td>2007395 A Transient Power Supply ESD Clamp with CMOS Thyristor Delay Element</td>
</tr>
<tr>
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<td>96291 CMOS-ON-SOI ESD Protection Networks</td>
</tr>
<tr>
<td>Safeer, N.I.</td>
<td>84085 A Material Evaluation Program for Decorative Static Control Table Top Laminates</td>
</tr>
<tr>
<td>Sagisaka, K.</td>
<td>2008185 Carbon Nanotube Plastic - Packaging Materials for Class 0 Device ESD Protection</td>
</tr>
<tr>
<td>Saini, R.</td>
<td>95090 Human Hand/Metal ESD and Its Physical Simulation</td>
</tr>
<tr>
<td>Saito, T.</td>
<td>2015RCJ Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply RCJ</td>
</tr>
<tr>
<td>Saitoh, T.</td>
<td>90177 Model of Leakage Current in LDD Output MOSFET Due to Low-Level ESD Stress</td>
</tr>
<tr>
<td>Sakakima, H.</td>
<td>2003382 ESD Phenomena in GMR Heads in the Manufacturing Process for HDD and GMR Heads</td>
</tr>
<tr>
<td>Sakamoto, K.</td>
<td>2015RCJ Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply RCJ</td>
</tr>
<tr>
<td>Sakata, H.</td>
<td>2006104 Study on EMI Phenomena for GMR/TMR Head</td>
</tr>
<tr>
<td>Sakimoto, M.</td>
<td>92076 An Advanced ESD Test Method for Charged Device Model</td>
</tr>
<tr>
<td></td>
<td>94170 Clarification of Ultra-High-Speed Electrostatic Discharge and Unification of Discharge Model</td>
</tr>
<tr>
<td>Sakui, K.</td>
<td>99225 Design Methodology of a Robust ESD Protection Circuit for STI Process 256Mb NAND Flash Memory</td>
</tr>
<tr>
<td>Sakuma, K.</td>
<td>20155A2 3D Integration ESD Protection Design and Analysis</td>
</tr>
<tr>
<td>Sakuyama, M.</td>
<td>2006235 Development of Ion Balance Sensor by using MOSFET</td>
</tr>
<tr>
<td>Salamero, C.</td>
<td>2006069 Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology</td>
</tr>
<tr>
<td></td>
<td>2010137 Impact of the Power Supply on the ESD System Level Robustness</td>
</tr>
<tr>
<td>Salcedo, J.A.</td>
<td>2009017 Transient Safe Operating Area (TSOA) Definition for ESD Applications</td>
</tr>
<tr>
<td></td>
<td>2009173 CDM ESD Current Characterization - Package Variability Effects and Comparison to Die-Level CDM</td>
</tr>
<tr>
<td></td>
<td>2010249 A New ESD Design Methodology for High Voltage DMOS Applications</td>
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<td></td>
<td>20165A4 Design of ESD Protection for Fault Tolerant Interface Applications with EMC Immunity</td>
</tr>
<tr>
<td></td>
<td>20172A1 High Blocking Voltage ESD Timer Clamp with Mistrigger Protection</td>
</tr>
<tr>
<td>Salem, A.</td>
<td>2000296 High Current Characteristics of Devices in a 0.18 μm CMOS Technology</td>
</tr>
</tbody>
</table>
Salhi, E.A.
97386 Characterization of ESD Damaged Magnetoresistive Recording Heads

Salisbury, J.
98341 Evaluation of Wrist Strap Monitors from an MR Head Perspective
2003414 Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2006240 Trends in External Ionizer Monitoring and Control
20164B2 Reducing EOS Current in Hot Bar Process in Manufacturing of Fiber Optics Components

Salles, A.
2010151 Correlation between System Level and TLP Tests Applied to Stand-Alone ESD Protections and Commercial Products
2011329 ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
2012409 Impact of Snapback Behavior on System Level ESD Performance with Single and Double Stack of Bipolar ESD Structures
20154B1 TLP-Based Human Metal Model Stress Generator and Analysis Method of ESD Generators
20175B2 High-Performance Bi-Directional SCR Developed on a 0.13 um SOI-Based Smart Power Technology for Automotive Applications

Salling, C.
2001192 Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

Salman, A.A.
2001205 Evaluation of Diode-Based and NMOS/Lnnp-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13µm CMOS Logic
2004248 ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure
2005421 SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies
2007185 Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI
2010031 The Relevance of Long-Duration TLP Stress on System Level ESD Design
2010309 Solutions to Mitigate Parasitic NPN Bipolar Action in High Voltage Analog Technologies
2011069 Novel Technologies to Modulate the Holding Voltage in High Voltage ESD Protections
2012373 A Flexible Simulation Model for System Level ESD Stresses with Applications to ESD Design and Troubleshooting
2013133 Mutual Ballasting: A Novel Technique for Improved Inductive System Level IEC ESD Stress Performance for Automotive Applications
2014252 Multi-Reflection TLP: A New Measurement Technique for System-Level Automotive ESD/EMC Characterization
20157A1 Design and Optimization on ESD Self-Protection Schemes for 700V LDMOS in High Voltage Power IC
20163B2 Case Study of DPI Robustness of a MOS-SCR Structure for Automotive Applications

Salmela, H.
2003143 ESD Sensitivity of Devices on a Charged Printed Wiring Board
2003151 New Methods for the Assessment of ESD Threats to Electronic Components
2004229 Electrostatic Field Limits and Charge Threshold for Field Induced Damage to Voltage Susceptible Devices
2005203 ESD Control in Automated Placement Process

Salminen, V.
2001050 Performance of Fiber Based ESD Protective Packaging

Salzone, G.
20173B2 EDA Checker for Identification of Excessive ESD Voltage Drop – Implementation to Smart Power IC’s
Samad, M. H. B. A
20162B2 Product Qualification & Degradation of Steel Toe ESD Footwear

Sambandan, S.
20172B2 On the ESD Behavior of Pentacene Channel Organic Thin Film Transistors

Sambi, M.
2008211 Novel 190V LIGBT-Based ESD Protection for 0.35μm Smart Power Technology Realized on SOI Substrate

San, H.F.
94063 A Correlation Study between Different Types of CDM Testers and “Real” Manufacturing In-Line Leakage Failures [BPR]

Sanayei, A.
2001318 GMR Heads as ESD Detectors-A Direct Assessment of Subtle ESD

Sanchez, M.
98341 Evaluation of Wrist Strap Monitors from an MR Head Perspective

Sancho, J.D.
2007226 Quick Check of ESD Bags for Shielding Efficiency

Sanesi, M.
91010 Recent Developments in ESD Waveform Evaluation

Sangameswaran, S.
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors
2009265 A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response under EOS-ESD Stress
2010443 Behavior of RF MEMS Switches under ESD Stress
2011130 A SCR-Based ESD Protection for MEMS-Merits and Challenges

Sankaralingam, R.
2013383 Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components
2014298 Threshold Voltage Shift Due to Incidental Pulse on Non-Stressed Pins during HBM Testing
20153B1 HBM Failures Induced by ESD Cell Turn-Off and Circuit Interaction with ESD Protection
20154B2 ESD Protection of Open-Drain I²C using Fragile Devices in Embedded Systems

Saotome, K.
98218 Measures against Electrostatic Destruction of Electronic Devices at Electronic Equipment Assembly Shops

Saraswat, K.C.
87001 VLSI Interconnections Technology, Present and Future

Sarbisheai, H.
2007395 A Transient Power Supply ESD Clamp with CMOS Thyristor Delay Element

Sarkar, A.
2011300 Efficient Multi-Domain ESD Analysis and Verification of Large SoC Designs

Sarkar, T.K.
85077 Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstressings: A Model
85092 Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Wunsch-Bell Model

Sasaki, S
20171A4 Oscillation of RC Power Clamp Inside IC Package

Sato, K.
2008332 New Protection Techniques and Test Chip Design for Achieving High CDM Robustness

Sato, M.
2002197 The ESD Preventive Measure Based on the Excessive Mobile Charge for Advanced Electron Devices and Production Lines
2003137 Advanced Technology for Monitoring Plasma Sparking ESD Damage using High Frequency Magnetic Wave Sensors
2004024 Nano-transient Current and Transient Resistance on the Conductive or Dissipative Materials for Extremely Sensitive Devices
Sato, T
2013037 Basic Characteristics of the Field Assisted Air Ionizer

Satterfield, H.W.
87258 Statistical and Graphical Analyses of Oxide Thickness and ESD Failure Modes

Sauers, J.P.
82175 In-Circuit Analysis of ESD Damaged Devices
84020 Test Equipment – A Source of ESD!!

Sauter, M.
20174A3 How to Build a Generic Model of Complete ICs for System ESD and Electrical Stress Simulation

Sawada, M.
2005025 Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor
2006039 Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications
2007053 Voltage Overshoot Study in 20V DeMOS-SCR Devices
2007089 Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis
2007158 Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions
2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD Stress
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
2009038 ESD Parameter Extraction by TLP Measurement
2009152 Calibration of Very Fast TLP Transients
2009364 Self-Protection Capability of Power Arrays
2009405 On-Wafer Human Metal Model Measurements for System-Level ESD Analysis
2010157 SCCF-System to Component Level Correlation Factor
2010349 Study of FI-CDM Discharge Waveforms
2010425 HBM Parameter Extraction and Transient Safe Operating Area
2012051 Misalignment between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester
2012379 Mixed-Mode Simulations for Power-on ESD Analysis
2014061 CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus

Scanlon, J.B.
96040 Recommendations to Further Improvements of HBM ESD Component Level Test Specifications [BPR]

Schaafhausen, J.
2005178 Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices

Scheier, S.
2014368 Analysis of ESD-Robustness of Multi-Layer Ceramic Capacitors in System Applications ESD German Forum Invited Paper

Scheucher, W.
2009292 A DRC-Based Check Tool for ESD Layout Verification
20172B1 Window Effects in HBM and TLP Testing

Schichl, J.
2001445 Integration of TLP Analysis for ESD Troubleshooting
2004141 Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
2005307 Problems with IO to all Other IOs ESD Stress Test: Two Case Studies
2006024 HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2007283 CDM Peak Current Variations and Impact upon CDM Performance Thresholds
2008094 Single Pulse CDM Testing and its Relevance to IC Reliability
2009183 Influence of CDM Tester Plate Size on Discharge Current
2010417 Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing
2011197 Capturing Real World ESD Stress with Event Detector
2011379 Two New Unexplained and Unresolved HBM Tester Related Failures
2014298 Threshold Voltage Shift Due to Incidental Pulse on Non-Stressed Pins during HBM Testing
Schimon, M.  
2006014 ESD Damage due to HBM Stressing of Non-Connected Pins

Schmeir, H.R.  
92218 Testing ESD Shielding Bags with an improved Bag Tester According to EIA-541  
96259 Some Results in Measuring Static Decay

Schmid, P.  
97027 Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs

Schmidt, N.  
2000239 Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors

Schmitt, M.  
2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation

Schmitt-Landsiedel, D.  
2003122 High Abstraction Level Permutational ESD Concept Analysis  
2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations  
2005033 RF ESD Protection Strategies: Codesign vs. Low-C Protection  
20166A3 Gain-Product on pn+pn-Structures at High Current Densities and the Impact on the IVCharacteristic

Schneider, J.  
97027 Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs  
2005413 PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latch-up Robustness  
2006214 Tunable Bipolar Transistor for ESD Protection of HV CMOS Applications  
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications  
2009221 IGBT Plugged in SCR Device for ESD Protection in Advanced CMOS Technology  
2011307 An Automated Approach for Verification of On-Chip Interconnect Resistance for Electrostatic Discharge Paths

Schneider, M.  
20157B1 Air-Discharge Testing of Single Components

Schnetker, T.R.  
79122 Human Factors in Electrostatic Discharge Protection

Scholten, A.  
2004040 ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions

Scholz, M.  
2006039 Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications  
2007053 Voltage Overshoot Study in 20V DeMOS-SCR Devices  
2007089 Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis  
2007158 Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions  
2007242 T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology  
2007408 Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications  
2008204 Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD Stress  
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors  
2008295 Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets  
2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness  
2009076 Electrical and Thermal Scaling Trends for SOI FinFET ESD Design  
2009265 A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response under EOS-ESD Stress  
2009329 CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS  
2009352 A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS  
2009364 Self-Protection Capability of Power Arrays  
2009371 Center Balanced Distributed ESD Protection for 1-110 GHz Distributed Amplifier in 45 nm CMOS Technology  
2009405 On-Wafer Human Metal Model Measurements for System-Level ESD Analysis  
2010157 SCCF-System to Component Level Correlation Factor  
2010293 Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays
HBM Parameter Extraction and Transient Safe Operating Area
Behavior of RF MEMS Switches under ESD Stress
A SCR-Based ESD Protection for MEMS-Merits and Challenges
HBM ESD Robustness of GaN-on-Si Schottky Diodes
ESD Protection Devices Placed Inside Keep-Out Zone (KOZ) of Through Silicon via (TSV) in 3D Stacked Integrated Circuits
Mis correlation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester
HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform
Mixed-Mode Simulations for Power-on ESD Analysis
Exploring ESD Challenges in Sub-20-nm Bulk FinFET CMOS Technology Nodes
ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices
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VFTLP Characteristics of ESD Protection Diodes in Advanced Bulk FinFET Technology
ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies
ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package
HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document?
VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires
VFTLP Characteristics of ESD Diodes in Bulk Si Gate-all-Around Vertically Stacked Horizontal Nanowire Technology

Scholz, S.
ESD Protection Design in a-IGZO TFT Technologies

Schrimpf, R.D.
Electrostatic-Discharge Detectors
ESD Effects on the Radiation Response of Power VDMOS Transistors
Detection of ESD-Induced Non-Catastrophic Damage in P-Channel Power MOSFETs
Annealing of ESD-induced Damage in Power MOSFETs

Schroder, H.
High Voltage Resistant ESD Protection Circuitry for 0.5 μm CMOS OTP/EPROM Programming Pin

Schrufer, K.
ESD Evaluation of the Emerging MuGFET Technology

Schulman, M.
Contact Transfer of Anions from Hands as a Function of the Use of Hand Lotions

Schulz, R.
CMOS-ON-SOI ESD Protection Networks

Schulz, T.
ESD Evaluation of the Emerging MuGFET Technology

Schwank, J.R.
Surprising Patterns of CMOS Susceptibility to ESD and Implications on Long-Term Reliability

Schwencker, R.
High Abstraction Level Permutational ESD Concept Analysis

Schwingshackl, T
Powered System-Level Conductive TLP Probing Method for ESD/EMI Hard Fail and Soft Fail Threshold Evaluation

Scott, T.
Shallow Trench isolation Double-Diode Electrostatic Discharge Circuit and Interaction with DRAM Output Circuitry

Scott, D.B.
A Lumped Element Model for Simulation of ESD Failures in Silicided Devices

Seantumpol, P.
Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment
<table>
<thead>
<tr>
<th>Author</th>
<th>Year</th>
<th>Title</th>
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<tbody>
<tr>
<td>Secareanu, R.</td>
<td>2014</td>
<td>Device Interactions between ESD Diodes and NMOS Clamps in CMOS Processes</td>
</tr>
<tr>
<td></td>
<td>2017</td>
<td>An Automated Tool for Minimizing Product Failures Due to Parasitic BJTs and SCRs</td>
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<tr>
<td></td>
<td>2007</td>
<td>Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology</td>
</tr>
<tr>
<td></td>
<td>2007</td>
<td>Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies</td>
</tr>
<tr>
<td></td>
<td>2008</td>
<td>ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology</td>
</tr>
<tr>
<td></td>
<td>2009</td>
<td>Impact of Stress Engineering on High-k Metal Gate ESD Diodes in 32 nm SOI Technology</td>
</tr>
<tr>
<td></td>
<td>2010</td>
<td>Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies</td>
</tr>
<tr>
<td></td>
<td>2011</td>
<td>A Current Density Analysis Tool to Identify BEOL Fails Under ESD Stress</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Identification and Verification of BEOL Metal Fails due to ESD Stress using Current Density Analysis Tool</td>
</tr>
<tr>
<td>Segura, P.L.</td>
<td>2003</td>
<td>Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits</td>
</tr>
<tr>
<td>Sei, T.</td>
<td>2008</td>
<td>New Protection Techniques and Test Chip Design for Achieving High CDM Robustness</td>
</tr>
<tr>
<td>Seider, S.</td>
<td>2016</td>
<td>Gun Tests of a USB3 Host Controller Board</td>
</tr>
<tr>
<td>Seidi, S.</td>
<td>2015</td>
<td>Using CC-TLP to get a CDM Robustness Value</td>
</tr>
<tr>
<td></td>
<td>2016</td>
<td>Predict the Product Specific CDM Stress Using Measurement-Based Models of CDM Discharge Heads</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Influence of Machine Configuration on EOS Damage during Wafer Cleaning Process</td>
</tr>
<tr>
<td>Seitz, M.A.</td>
<td>2009</td>
<td>Thermal Stability of Metal Oxide Surge Suppression Devices</td>
</tr>
<tr>
<td>Sekine, T.</td>
<td>2016</td>
<td>Mirrored Power Distribution Network Noise Injection for Soft Failure Root Cause Analysis</td>
</tr>
<tr>
<td>Sekino, S.</td>
<td>9819</td>
<td>ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate</td>
</tr>
<tr>
<td>Seliger, N.</td>
<td>9924</td>
<td>Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices</td>
</tr>
<tr>
<td>Semenov, O.</td>
<td>2007</td>
<td>A Transient Power Supply ESD Clamp with CMOS Thyristor Delay Element</td>
</tr>
<tr>
<td>Seng, L.</td>
<td>9915</td>
<td>Conductive Floor and Footwear System as Primary Protection against Human Body Model ESD Event</td>
</tr>
<tr>
<td>Sengupta, R.</td>
<td>2017</td>
<td>On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism</td>
</tr>
<tr>
<td>Senko, G.</td>
<td>9802</td>
<td>Metrology and Methodology of System Level ESD Testing</td>
</tr>
<tr>
<td>Seol, B.</td>
<td>2011</td>
<td>A Study of a Measurement and Simulation Method on ESD Noise Causing Soft-Errors by Disturbing Signals</td>
</tr>
<tr>
<td></td>
<td>2012</td>
<td>A Novel Method for ESD Soft Error Analysis on Integrated Circuits Using a TEM Cell</td>
</tr>
<tr>
<td></td>
<td>2014</td>
<td>System-Level ESD Failure Diagnosis with Chip-Package-System Dynamic ESD Simulation</td>
</tr>
<tr>
<td></td>
<td>2016</td>
<td>Measurement of Discharging Currents through an IC due to the Charged Board Event Using a Shielded Rogowski Coil</td>
</tr>
<tr>
<td>Serneels, B.</td>
<td>2011</td>
<td>Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in a 40 nm Pure 1.8V Process</td>
</tr>
</tbody>
</table>
Servais, G.E.
95175  A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices

Setoya, T.
20164B1  An ESD Control Method Considering the Semiconductor Device Charged Voltage

Seva, R.
20178A1  On-Chip Sensors to Measure Level of Transient Events

Shah, B.M.
88077  Test Methods to Characterize Triboelectric Properties of Materials
89102  Test Method to Characterize Triboelectric Properties of Adhesive Tapes

Shah, G.
95175  A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices

Shahidi, G.G.
96291  CMOS-ON-SOI ESD Protection Networks
97210  Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks
99105  Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips
2000029  Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

Shankar, B.
20172A2  On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism

Sharma, A.
20175A3  Correlation Study of Different CDM Testers and CCTLP

Sharp, M.J.
82157  ESD Minimization Technique for MOS Manufacturing Final Test Area

Shaw, J.M.
94226  Electrically Conducting Polyanilines for Electrostatic Dissipation

Shaw, R.N.
83048  A Programmable Equipment for Electrostatic Discharge Testing to Human Body Models
83185  ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics [BPP]
84165  Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
85132  An Experimental Investigation of ESD-Induced Damage to Integrated Circuits on Printed Circuit Boards
86224  An Experimental Validation of the Field-Induced ESD Model
86232  A Programmable Equipment for ESD Testing to the Charged-Device Model

Sheehan, D.K.
82185  Electrostatic Discharge Immunity in Computer Systems

Shen, Y.
2000355  Baseline Popping of Spin-Valve Recording Heads Induced by ESD

Sheridan, D.
2002092  Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

Sherony, M.
2000029  Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry

Sherry, S.C.K.
2002382  Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD
Shibkov, A.
2011140 Active Clamp Implementation in Complementary BiCMOS Process with High Voltage BJT Devices
2012348 SCR Clamps with Transient Voltage Detection Driver
2012379 Mixed-Mode Simulations for Power-on ESD Analysis
2014189 AutomatedLatch-up Analysis
2015A43 Active Clamps with Hybrid BJT-CMOS Operation Mode
2015A1 ESD Protection Design in Active-Lite Interposer for 2.5 and 3D Systems-in-Package
2016A4 Low Voltage SCR Clamp with High-VT Reference
2016B1 PMOS Arrays Self-Protection Capability Limitation
2017A1 Cross-Domain Interaction at System Level Stress

Shichijo, H.
2001012 5-V Tolerant Fail-Safe ESD Solutions for a 0.18µm Logic CMOS Process

Shieh, W-T.
2009011 New Layout Scheme to Improve ESD Robustness of I/O Buffers in Fully-Silicided CMOS Process

Shigematsu, S.
2004075 Evaluation of ESD Hardness of Fingerprint Sensor LSIs

Shiley, W.L.
84144 An Evaluation of EOS Failure Models
88137 Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses

Shim, J.S.
2002362 ESD Characterization of Grounded-Gate NMOS with 0.35 µm/18 V Technology Employing Transmission Line Pulser (TLP) Test

Shim, K-H
2012396 Current-Voltage, S-Parameter, LFN Properties in T-R-T Type ESD/EMI Filters with TVS Zener Diodes Developed Using Epitaxy-Based

Shimaya, M.
2000260 ESD Protection in Fully-Depleted CMOS/SIMOX with a Tungsten-Clad Source/Drain

Shimizu, T.
2006116 Effect of Electrostatic Discharge on Tunneling Magnetoresistive Sensor

Shimoyama, N.
2004075 Evaluation of ESD Hardness of Fingerprint Sensor LSIs

Shinde, S.
2017A2 An ESD Demonstrator System for Evaluating the ESD Risks of Wearable Devices

Shintani, T.
2010349 Study of FI-CDM Discharge Waveforms
2014061 CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus

Shinzawa, T.
2006087 Operation Analysis and Implementation of CMOS Compatible Vertical Bipolar ESD Protection Devices for Automotive Applications
2007037 Layout Technique to Alleviate Soft Failure for Short Pitch Multi Finger ESD Protection Device

Shiochi, M.
2006196 An Active ESD Protection Technique for the Power Domain Boundary in a Deep Submicron IC

Shrier, K.
2004088 Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance
2005270 Cell Phone GaAs Power Amplifiers: ESD, TLP, and PVS Devices
Shrivastava, M.
2009221  IGBT Plugged in SCR Device for ESD Protection in Advanced CMOS Technology
2011022  Technology Scaling Effects on the ESD Performance of Silicide-Blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies
2011059  ESD Robust DeMOS Devices in Advanced CMOS Technologies
2014001  ESD Behavior of Metallic Carbon Nanotubes
2016A2   Unique Current Conduction Mechanism through Multi Wall CNT Interconnects under ESD Conditions
2017A2   On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism
2017B2   On the ESD Behavior of Pentacene Channel Organic Thin Film Transistors
2017A2   FinFET SCR: Design Challenges and Novel Fin SCR Approaches for On-Chip ESD Protection

Shubitidze, P.
96203    Numerical Calculation of ESD

Shukla, V.
2010041  CDM Simulation Study of a System-in-Package
2010389  Investigation of Current Flow during Wafer-Level CDM using Real-Time Probing
2013383  Predictive Modeling of Peak Discharge Current during Charged Device Model Test of Microelectronic Components

Shumiya, H

Siansuri, E.
2010381  CDM Effect on a 65 nm SOC LNA

Sias, R.
91210    A New Permanent ESD and Corrosion Resistant Material [BPR]

Sieck, A.
2002073  Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies

Siemsen, K.B.
87168    EOS Test Limits for Manufacturing Equipment

Silberman, J.
2015A2   3D Integration ESD Protection Design and Analysis

Sillanpaa, L.
2009414  ESD Event Receiver for System Level Testing

Simbürger, W.
2008221  ESD Concept for High-Frequency Circuits
2013191  Powered System-Level Conductive TLP Probing Method for ESD/EMI Hard Fail and Soft Fail Threshold Evaluation

Simcoe, R.J.
84202    A CMOS VLSI ESD Input Protection Device, DIFIDW
86188    Design and Test Results for a Robust CMOS VLSI Input Protection Network

Simin, A
2013283  ESD Protection Circuit for a Sub-1 dB Noise Figure LNA in a SiGe: C BiCMOS Technology

Simoen, E.
2008059  Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques

Simon, N.
2007237  Noise Characteristics of MOSFET Ionizer Balance Sensor

Singh, A.
2000505  Effect of 1nS to 250 mS ESD Transients on GMR Heads
Sinha, R.  
20172B2 On the ESD Behavior of Pentacene Channel Organic Thin Film Transistors

Sinha, S.  
98208 An Automated Tool for Detecting ESD Design Errors

Sinkevitch, V.F.  
97013 Gate Burnout of Small Signal MODFETs at TLP Stress  
97330 Electrical Filamentation in GGMOS Protection Structures

Siritaratiwat, A.  
2001299 Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process

Sithanandam, R.  
2012015 ESD Design Challenges in 28 nm Hybrid FDSOI/Bulk Advanced CMOS Process

Sittampalam, Y.  
2000296 High Current Characteristics of Devices in a 0.18 μm CMOS Technology

Skelton, D.J.  
82091 Second Breakdown in Switching Transistors

Skjeie, D.A.  
90092 Testing Electronic Products for Susceptibility to Electrostatic Discharge

Slaby, R.  
2008178 Considerations for CPM Measurements of Fast Switching Ionizers

Slenski, G.  
83021 Air Force Maintenance Program for Electrical Overstress/Electrostatic Discharge (EOS/ESD) Control

Slinkman, J.A.  
92277 Shallow Trench isolation Double-Diode Electrostatic Discharge Circuit and Interaction with DRAM Output Circuity  
94246 Three-Dimensional Transient Electrothermal Simulation of Electrostatic Discharge Protection Circuits  
95043 Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors

Sloan, J.  
2004166 ESD Design Automation for a 90nm ASIC Design System  
2004182 CDM Failure Modes in a 130nm ASIC Technology  
2005126 Design Automation to Suppress Cable Discharge Event (CDE) Induced Latch-up in 90nm CMOS ASICs

Smalanskas, G.  
95129 Effectiveness of ESD Training Using Multimedia

Smallwood, J.M.  
2003143 ESD Sensitivity of Devices on a Charged Printed Wiring Board  
2003151 New Methods for the Assessment of ESD Threats to Electronic Components  
2004229 Electrostatic Field Limits and Charge Threshold for Field Induced Damage to Voltage Susceptible Devices  
2010217 CDM Damage due to Automated Handling Equipment  
2010233 Comparison of Methods of Evaluation of Charge Dissipation from AHE Soak Boats  
2014033 Optimizing Investment in ESD Control  
2014206 Electrostatic Threats in Hospital Environment  
20162B1 Electrostatic Shock Risks in Assembly of Large Wind Turbine Blades  
20171B4 Charged Device Discharge Measurement Methods in Electronics Manufacturing  
20174B1 Qualification Challenges of Footwear and Flooring Systems  
20174B2 The Main Parameters Affecting Charged Device Discharge Waveforms in CDM Qualification and Manufacturing

Smedes, T.  
2001096 Automatic Layout Based Verification of Electrostatic Discharge Paths  
2001426 The Application of Transmission Line Pulse Testing for the ESD Analysis of Integrated Circuits  
2002267 ESD Protection by Keep-On Design for a 550 V Fluorescent Lamp Control IC with Integrated LDMOS Power Stage
2002354 The Impact of Substrate Resistivity on ESD Protection Devices
2003108 ESD Phenomena in Interconnect Structures
2005001 Selecting an Appropriate ESD Protection for Discrete RF Power LDMOSTs
2006077 ESD Protection for the High-Voltage CMOS Technologies
2006136 Relations between System Level ESD and (vF) TLP
2007047 Designing HV Active Clamps for HBM Robustness
2007357 Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections during Fast Transients
2008006 Gate Oxide Protection and ggNMOSTs in 65 nm
2008014 On the Relevance of IC ESD Performance to Product Quality
2008099 A Methodology for the ESD Test Reduction for Complex Devices
2009292 A DRC-Based Check Tool for ESD Layout Verification
2010083 On-Chip System ESD Protection of FM Antenna Pin
2010341 Pitfalls for CDM Calibration Procedures
2011163 Predictive CDM Simulation Approach Based on Tester, Package and Full Integrated Circuit Modeling
2011267 A Contribution to the Evaluation of HMM for IO Design
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results
2012060 HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform
2012143 Analysis of ESD Fails in a 45 nm Mixed Signal SoC
2013283 ESD Protection Circuit for a Sub-1 dB Noise Figure LNA in a SiGe: C BiCMOS Technology
2014384 Characterization Methods to Replicate EOS Fails
2015A1 A Study of the Effect of Remote CDM Clamps in Integrated Circuits
2015A1 Weart out Effects in ESD Characterization and Testing
2016A4 PNP-eSCR ESD Protection Device with Tunable Trigger and Holding Voltage for High Voltage Applications
2016B3 HMM Single Site Testing: Can We Reproduce Component Failure Level with the HMM Document?
2016A2 JS-002 Module and Product CDM Result Comparison to JEDEC and ESDA CDM Methods
2017A1 A New Type of Furniture ESD and Its Implications
2017B1 Window Effects in HBM and TLP Testing

Smith, B.L.
87134 Constant Monitoring: Quality You Can't Afford to be without

Smith, D.A.
86030 Internal Quality Auditing and ESD Control

Smith, D.C.
86100 Computer Simulation of ESD and Lightning Events
89114 Applying High Frequency Techniques to Measuring ESD Phenomena and its Effects
92047 Techniques and Methodologies for Making System Level ESD Response Measurements for Troubleshooting or Design Verification
93003 A New Type of Furniture ESD and Its Implications
96211 Measurements of ESD HBM Events, Simulator Radiation and Other Characteristics toward Creating a More Repeatable Simulation
96223 An Investigation into the Performance of the IEC 1000-4-4 Capacitive Clamp
98029 Metrology and Methodology of System Level ESD Testing
98368 Electromagnetic Interference (EMI) Damage to Giant Magneto resistive (GMR) Recording Heads
99329 Unusual Forms of ESD and Their Effects
2000048 ESD Immunity in System Designs, System Field Experiences and Effects of PWB Layout
2001385 The EMI/ESD Environment of Large Server Installations
2002026 Sources of Impulsive EMI in Large Server Farms
2002032 Electromagnetic Interference (EMI) Inside a Hard Disk Drive Due to External ESD

Smith, J.
2012A1 Latch-up Characterization and Checking of a 55 nm CMOS Mixed Voltage Design

Smith, J.C.
97356 Prediction of ESD Protection Levels and Novel Protection Devices in Thin Film SOI Technology
98063 A Substrate Triggered Lateral Bipolar Circuit for High Voltage Tolerant ESD Protection Applications
99062 An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction during EOS/ESD Events
A MOSFET Power Supply Clamp with Feedback Enhanced Triggering for ESD Protection in Advanced CMOS Technologies

Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window

A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65nm CMOS Technologies

Smith, J.G.

ESD Sensitivity and Latency Effects of Some HCMOS Integrated Circuits

Smith, J.S.

Modeling of Electrical Overstress in Silicon Devices
Modeling of EOS in Silicon Devices
Prediction of Thin-Film Resistor Burnout
General EOS/ESD Equation
EOS Analysis of Soldering Iron Tip Voltage

Smith, M.

Contaminated Antistatic Polyethylene

Smith, S.

Unique ESD Failure Mechanisms during Negative to Vcc HBM Tests

Smooha, Y.

Characterization of a 0.16μm CMOS Technology using SEMATECH ESD Benchmarking Structures
A Comparison of ESD Failure Thresholds of CMOS I/O Buffers Using Real Human Body and Human Body Model Simulators

Smy, P.R.

Mathematical Modeling of Electrostatic Propensity of Protective Clothing Systems

Smyth Jr., J.B.

Solar Cell Electrical Overstress Analysis

Snow, L.

A Successful ESD Training Program

Snyder, H.C.

A Comprehensive ESD Control Program for a Large Disk File
Effects of Unbalanced Ionizers on Magnetoresistive Recording Heads
A Study of Methods to Eliminate Metal Contact in GMR Head Manufacturing

Snyder, H.Z.

The Effects of High Humidity Environments on Electrostatic Generation and Discharge

So, H.T.

ESD Characterization of Grounded-Gate NMOS with 0.35 μm/18 V Technology Employing Transmission Line Pulser (TLP) Test

Soda, Y.

A Study of Electrostatic Discharge on MR Heads in Digital Tape Systems
Discharge Current and Electric Field Radiated from a Small Capacitance Device
A Second ESD Threat for ESD Sensitive Devices with Copper Leads
A Study of ESD Protection for Helical-scan Tape Heads
A Resistive Ferrite Substrate for the GMR Head in Helical-scan Tape Systems
Modeling of Discharge between Wire and GMR Head

Soden, J.M.

The Dielectric Strength of Silicon Dioxide in a CMOS Transistor Structure
ESD Evaluation of Radiation-Hardened, High Reliability CMOS and MNOS ICs
Latent Failures Due to Electrostatic Discharge in CMOS Integrated Circuits
Extent and Cost of EOS/ESD Damage in an IC Manufacturing Process
Human Body Model, Machine Model, and Charged Device Model ESD Testing of Surface Micromachined Microelectromechanical
Soder, B.  
97170  Grounding Personnel via the Floor/Footwear System

Sohl, J.E.  
80218  An Evaluation of Wrist Strap Parameters

Soloro, Y.  
2014007  Thin-body ESD Protections in 28nm Utbb-Fdsoi: from Static to Transient Behavior  
20151A1  Innovative High-Density ESD Protection Device in State of the Art FDSOI UTBB Technologies

Soldner, W.  
2003328  A Traceable Method for the Arc-free Characterization and Modeling of CDM-Testers and Pulse Metrology Chains  
2005033  RF ESD Protection Strategies: Co-design vs. Low-C Protection  
2013115  Thyristor Compact Model for ESD, DC and RF Simulation

Somasiri, N.L.D.  
96227  Vanadium Pentoxide Based Antistatic Coatings

Somayaji, A.  
2006222  High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies

Sommerfeld, H.  
91045  Implementation of Computer-Based ESD Training: A Case Study Comparing the Computer Approach with Traditional Classroom

Song, L.  
20151A2  Design and Optimization of ESD Lateral NPN Device in 14nm FinFET SOI CMOS Technology

Song, M.  
95304  Quantifying ESD/EOS Latent Damage and Integrated Circuit Leakage Currents

Song, M-H.  
2011116  CDM Protection for Millimeter-Wave Circuits  
2011267  A Contribution to the Evaluation of HMM for IO Design  
2012324  High-k Metal Gate-Bounded Silicon Controlled Rectifier for ESD Protection  
2012331  Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process  
2012336  Schottky Emitter High Holding Voltage ESD Clamp in BCD Power Technology  
2013015  High CDM Resistant Low-Cap SCR for 0.9 V Advanced CMOS Technology  
2013278  Novel Isolation Ring Structure for Latch-up and Power Efficiency Improvement of Smart Power Ics  
2013357  An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs  
2014349  High Flexibility SCR Clamp for ESD Protection in BCD Power Technology  
2014354  A High-Reliable Self-Isolation Current-Mode Transmitter (CM-Tx) Design for +/-60V Automotive Interface with Bulk-BCD Technology  
20157A3  Investigation and Solution to the Early Failure of Parasitic NPN Triggered by the Adjacent PNP ESD Clamps  
20163A2  An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology  
20171A2  Deep N-well Induced Latch-up Challenges in Bulk FinFET Technology  
20176B2  Novel SCR Structure for Power Supply Protection in FinFET Technology

Soni, A.  
20172A2  On the ESD Behavior of AlGaN/GaN Schottky Diodes and Trap Assisted Failure Mechanism

Soppa, W.  
2003088  Characterization and Modeling of Transient Device Behavior under CDM ESD Stress  
2003116  Impact of Layer Thickness Variations of SOI-Wafer on ESD-Robustness  
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Sorgeloos, B.  
2008325  CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between IO Test Chips and Product Level  
2010167  On-Chip ESD Protection with Improved High Holding Current SCR (HHISCR) Achieving IEC 8 kV Contact System Level  
20175B3  Low Capacitive Dual Bipolar ESD Protection
Soto, A.
95124 ESD Measurements and Corrective Actions for Integrated Circuits (IC) Lead Inspection/Handling Systems

Soussan, P.
2005025 Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Spehar, J.R.
94257 The Effect of Oxidation of the Poly Gate on the ESD Performance of CMOs ICs

Splingart, B.
97027 Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs

Sreedhar, K.
20156A1 A Full-Chip ESD Simulation Flow

Srinivasan, K.
2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation
20156A2 A New Full-Chip Verification Methodology to Prevent CDM Oxide Failures

Srinivasan, S.
2013361 Using Static Voltage Analysis and Voltage-Aware DRC to Identify EOS and Oxide Breakdown Reliability Issues

Srinivasan, V.
2000437 A Scalable Analytical Model for the ESD N-Well Resistor

Srivastava, A.
2011106 Effect of On-Chip ESD Protection on 10 Gb/s Receivers
2013140 On-Chip System Level ESD Protection for Class G Audio Power Amplifiers
2013209 HBM ESD Protection for Class G Power Amplifiers

Srivastava, P.
2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes

Srur, S.
2002123 Effects of ESD Transients on the Properties of GMR Heads

Stadler, A.
20173A1 Risk Assessment of Cable Discharge Events

Stadler, W.
97366 Does the ESD-Failure Current Obtained by Transmission Line Pulsing Always Correlate to Human Body Model Tests?
98271 Bipolar Model Extension for MOS Transistors Considering Gate Coupling Effects in the HBM ESD Domain
2000422 Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase
2001205 Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13µm CMOS Logic
2002073 Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies
2002387 Investigation of ESD Protection Elements under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry
2003080 Transient Latch-up: Experimental Analysis and Device Simulation
2003088 Characterization and Modeling of Transient Device Behavior under CDM ESD Stress
2003122 High Abstraction Level Permutational ESD Concept Analysis
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2003328 A Traceable Method for the Arc-free Characterization and Modeling of CDM-Testers and Pulse Metrology Chains
2003338 Capacitively Coupled Transmission Line Pulsing CC-TLP - A Traceable and Reproducible Stress Method in the CDM-Domain
2004067 From the ESD Robustness of Products to the System ESD Robustness
2004299 Development Strategy for TLU-Robust Products
2005178 Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices
2005245 SoC-A Real Challenge for ESD Protection?
2006144 Cable Discharges into Communication Interfaces
2006284 Ultra-thin Gate Oxide Reliability in the ESD Time Domain
Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses

CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts

Reliability Aspects of Gate Oxide under ESD Pulse Stress

External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique

VF-TLP Round Robin Study, Analysis and Results

Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests

Characterization and Simulation of Real-World Cable Discharge Events

Triggering of Transient Latch-up (TLU) by System Level ESD

SCCF-System to Component Level Correlation Factor

HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform

Is There Correlation Between ESD Qualification Values and the Voltages Measured in the Field?

Sampling Pin Approaches for ESD Test Applications

On the Characterization of ESD Properties of JEDEC Trays

A Systematic Method for Determining Soft-Failure Robustness of a Subsystem

Activities Towards a New Transient Latch-up Standard

Do Devices on PCBs Really See a Higher CDM-like ESD Risk?

Practical HBM Testing with Statistical Pin Combinations

Charged Device Discharge Measurement Methods in Electronics Manufacturing

Risk Assessment of Cable Discharge Events

The Main Parameters Affecting Charged Device Discharge Waveforms in CDM Qualification and Manufacturing

A Newly Observed High Frequency Effect on the ESD Protection Utilized in a Gigahertz NMOS Technology

Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

Wide Range Control of the Sustaining Voltage of ESD Protection Elements Realized in a Smart Power Technology

Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices

Study of Trigger Instabilities in Smart Power Technology ESD Protection Devices Using a Laser Interferometric Thermal Mapping

Investigation of ESD Protection Elements under High Current Stress in CDM-Like Time Domain Using Backside Laser Interferometry

Coupled Bipolar Transistors as Very Robust ESD Protection Devices for Automotive Applications

ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive

A TLP-Based Characterization Method for Transient Gate Biasing of MOS Devices in High-Voltage Technologies

On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD

ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology

Degraded Device Detection

Selecting Materials for Protection against ESD Using an ESD Shielding Effectiveness Meter

A Study on the Effectiveness of ESD Smocks

An Automated Approach for Verification of On-Chip Interconnect Resistance for Electrostatic Discharge Paths

Chasing a Latent CDM ESD Failure by Unconventional FA Methodology

Current Filament Movement and Silicon Melting in an ESD-Robust DENMOS Transistor

Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers

Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps
Steinman, A.
93065 Periodic Verification of Air Ionizer Performance
94028 Ionization for Production Tools
95245 Best Practices for Applying Air Ionization
96022 Static Charge Control Issues for Disk Drive Production Using MR Heads
96145 Developing an Exit Charge Specification for Production Equipment
96365 Electrostatic Problems in TFT-LCD Production and Solutions Using Ionization
97298 Static Control Technology Preserves Ancient Egyptian Artifacts
99168 Test Methodologies for Detecting ESD Events in Automated Processing Equipment

2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2006240 Trends in External Ionizer Monitoring and Control
2008142 Static Control Standards in the Semiconductor Industry
2010225 Measurements to Establish Process ESD Compatibility
2012111 Process ESD Capability Measurements
2013048 Equipment ESD Capability Measurements
2014046 Measuring Handler CDM Stress Provides Guidance for Factory Static Controls
20151B2 Manufacturing Changes Air Ionization Technology

Stella, R.
2003088 Characterization and Modeling of Transient Device Behavior under CDM ESD Stress
2003319 Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages
2004107 Study of CDM Specific Effects for a Smart Power Input Protection Structure

Stephan, R.
2008006 Gate Oxide Protection and ggNMOSTs in 65 nm

Stephens, C.E.
85163 A Technique for Real Time Examination of Sub-System ESD/EOS Damage in Integrated Circuits [BPR]
86219 A Study of EOS in Microcircuits Using the Infra-Red Microscope

Sterrantino, S.
2006222 High Voltage ESD Protection Strategies for USB and PCI Applications for 180nm/130nm/90nm CMOS Technologies

Steven S.
20156A1 A Full-Chip ESD Simulation Flow

Stevens, B.N.
86136 Determining the Surface Resistivity of ESD Protective Cellular Packaging Materials

Stevens, M.
96167 Charged Device Model (CDM) Metrology: Limitations and Problems

Stewart, H.D.
83134 ESD Evaluation of Radiation-Hardened, High Reliability CMOS and MNOS ICs

Steyaert, M.
2001062 Analysis and Improved Compact Modeling of the Breakdown Behavior of Sub-0.25 Micron ESD Protection ggNMOS Devices
2002018 A 6mW, 1.5dB NF CMOS LNA for GPS with 3kV HBM ESD-Protection
2002111 Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices
2003195 Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits
2004098 Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies

Stiegler, H.
88201 A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes [BPR]

Stockin, D.
2000368 Designing and Testing of Facilities Ground
Stockinger, M.
2001082 Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies
2003017 Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
2004255 Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies
2004280 Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications
2005070 ESD Protection for Advanced CMOS SOI Technologies
2006046 Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe
2006186 Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology
2007289 A Novel Testing Approach for Full-Chip CDM Characterization
2009091 CDM Protection Design for CMOS Applications Using RC-Triggered Rail Clamps
2011007 A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction
2011076 When Good Trigger Circuits Go Bad: A Case History
2013214 An Active MOSFET Rail Clamp Network for Component and System Level Protection
2013313 Investigation of Product Burn-in Failures due to Powered NPN Bipolar Latching of Active MOSFET Rail Clamps
2014223 Device Interactions between ESD Diodes and NMOS Clamps in CMOS Processes
20178A1 On-Chip Sensors to Measure Level of Transient Events

Stoker, D.K.
89111 Development of the Corporate ESD Control Programme within British Telecommunications

Stokes, S.
2002123 Effects of ESD Transients on the Properties of GMR Heads

Storm, D.C.
79004 Controlling Electrostatic Problems in the Fabrication and Handling of Spacecraft Hardware

Stotts, L.J.
83118 Temperature at Second Breakdown at a Well-Defined Site

Strachan, A.
2010293 Improving the ESD Self-Protection Capability of Integrated Power NLDMOS Arrays

Strand, C.J.
82145 An Effective Electro- Static Discharge Protection Program

Strang, S.
2002296 An Automated Electrostatic Discharge Computer-Aided Design System with the Incorporation of Hierarchical Parameterized Cells in BiCMOS Analog and RF Technology For Mixed Signal Applications

Strauss, M.S.
87059 Variations in Failure Modes and Cumulative Effects Produced by Commercial Human-Body-Model Simulators
91110 Protecting N-Channel Output Transistors from ESD Damage

Streibl, M.
2002073 Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies
2003080 Transient Latch-up: Experimental Analysis and Device Simulation
2003122 High Abstraction Level Permutational ESD Concept Analysis
2004322 Multi-Terminal Pulsed Force & Sense ESD Verification of I/O Libraries and ESD Simulations
2005033 RF ESD Protection Strategies: Co-design vs. Low-C Protection
2005060 SCR Operation Mode of Diode Strings for ESD Protection

Stricker, A.D.
95205 Layout Optimization of an ESD-Protection N-MOSFET by Simulation and Measurement
98290 Characterization and Optimization of a Bipolar ESD –Device by Measurements and Simulations
99001 Analysis and Compact Modeling of Lateral DMOS Power Devices under ESD Stress Conditions

Stroncer, C.G.
94315 Root Cause Analysis and Packaging Enhancements to Improve Processor ESD Susceptibility
Stubbart, J.  
2000505  Effect of 1nS to 250 mS ESD Transients on GMR Heads

Stucchi, M.  
94292  A Method for the Characterization and Evaluation of ESD Protection Structures and Networks

Stuckert, G.  
2003414  Wrist Strap Monitor Testing for Use with the Latest MR Head Technologies

Studel, K.  
20161A1  ESD Protection Design in a-IGZO TFT Technologies

Stuffer, A.  
20153B3  ESD Failure Caused by Parasitic SCR in an Overvoltage Tolerant I/O

Stunkard, D.  
86159  Electrostatic Discharge Effects on Gallium Arsenide Integrated Circuits [BPP]

Su, Y-T.  
2013015  High CDM Resistant Low-Cap SCR for 0.9 V Advanced CMOS Technology  
20171A2  Deep N-well Induced Latch-up Challenges in Bulk FinFET Technology

Subba, N.  
2004248  ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure

Suchak, M.  
20178A1  On-Chip Sensors to Measure Level of Transient Events

Suh, K.S.  
2002233  ESD Protection Materials Using Conductive Polymers  
2008191  Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer  
2010279  Static Charge Induced Orientation of Liquid Crystals in LCD Panels  
2012091  Minimizing Electrostatic Charge Generation and ESD Event in TFT-LCD Production Equipment  
2013323  Electrostatic Control and its Analysis of Roller Transferring Processes in FPD Manufacturing

Sukpitikul, A.  
2011210  Relationship between Moulding Compounds and Tribocharging in IC Manufacturing and Tape & Reel Shipment

Sullivan, S.S.  
85103  The Automobile Environment Its Effects on the Human Body ESD Model

Sumida, H.  
87232  Occurrence and Modes of Approaching Discharges and Separating Discharges - Characteristic Features of Electrostatic Discharges

Sun, J.  
2000355  Baseline Popping of Spin-Valve Recording Heads Induced by ESD

Sun, J.Y.C.  
96291  CMOS-ON-SOI ESD Protection Networks

Sun, X.  
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor

Sundquist, J.  
2004166  ESD Design Automation for a 90nm ASIC Design System

Suopys, A.  
92179  Thermoformable Materials for Static Protection

Sutorius, G.  
99043  A Study of ESD Induced Lockups in a Semiconductor Photolithography Area
Suwannata, N.
2001299 Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process

Suzuki, K.
99116 A Simulation Analysis of Quarter-Micron CMOS LSI Input Circuit Behavior under CDM-ESD for Protection Device Improvement
2002197 The ESD Preventive Measure Based on the Excessive Mobile Charge for Advanced Electron Devices and Production Lines
2003137 Advanced Technology for Monitoring Plasma Sparking ESD Damage using High Frequency Magnetic Wave Sensors
2004024 Nano-transient Current and Transient Resistance on the Conductive or Dissipative Materials for Extremely Sensitive Devices

Suzuki, T.
98199 ESD and Latch-up Characteristics of Semiconductor Device with Thin Epitaxial Substrate
99078 Invited Paper: A Study of Fully Silicided 0.18µm CMOS ESD Protection Devices
2004016 Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process
2005290 A Study of Relation between a Power Supply ESD and Parasitic Capacitance
2007403 A Study of Relation between a Power Supply ESD and Parasitic Capacitance
2008325 CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between IO Test Chips and Product Level

Svanstrom, H
2012181 Triboelectrification of Static Dissipative Materials

Swaminathan, H.
98208 An Automated Tool for Detecting ESD Design Errors

Swenson, D.E.
87274 Triboelectric Charge - Discharge Damage Susceptibility of Large Scale IC’s
92209 Triboelectric Testing of Packaging Materials - Practical Considerations What Is Important? What Does It Mean?
94230 A New Technology in Low Tribocharging Adhesives
95141 Resistance to Ground and Tribocharging of Personnel, As Influenced By Relative Humidity
96241 Antistatic Masking Tapes for Solder Flux Reflow Processing of Printed Circuit Boards
97303 Shock in the Shower
2000360 Invited Paper: ESD Control in the Factory of the Future or 20.20 to the Rescue
2004187 Compliance Verification: The Critical Component of a Certified ANSI/ESD S20.20 ESD Control Program Plan
2006240 Trends in External Ionizer Monitoring and Control
2012191 Test Method Recommendations for the Evaluation of Packaging Materials Used for Small Static Sensitive Electronic Components
2012207 Electrical Fields: What to Worry About?

Swent, R.L.
86054 Avoiding Thermal Breakdown in Overdriven Digital Circuit Outputs

Swiecicki, M.
97292 Electrostatics Concerns in the Graphic Arts Industry

Sydänheimo, L.
2014375 ESD Sensitivity of 01005 Chip Resistors and Capacitors
20155B2 ESD and Disturbance Cases in Electrostatic Protective Areas
20157B2 The Effect of USB Ground Cable and Product Dynamic Capacitance on IEC61000-4-2 Qualification

Sydney, G.T.
90231 The Versatility of Electron Beam Processing, and the Conversion of Medium and High Performance Polymeric Films for ESD Protection

Sztatkowski, J.
2002073 Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies

Szymanski, M.
98341 Evaluation of Wrist Strap Monitors from an MR Head Perspective
<table>
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<tr>
<th>Name</th>
<th>Year</th>
<th>Title</th>
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<tr>
<td>Tabat, N.</td>
<td>2000</td>
<td>Limitations of the Adiabatic Model for ESD Failure in GMR Structures</td>
</tr>
<tr>
<td>Tabata, Y.</td>
<td>2000</td>
<td>Floating Gate EEPROM as EOS Indicators during Wafer-Level GMR Processing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Effects of ESD Transients on the Properties of GMR Heads</td>
</tr>
<tr>
<td>Tachamaneeekorn, P.</td>
<td>2000</td>
<td>Estimation of Discharge Energy Released From Charged Insulator</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Shield Effect of Electrically Conductive Materials against Electromagnetic Waves Radiated by Electrostatic Discharge</td>
</tr>
<tr>
<td>Tagashira, K.</td>
<td>2000</td>
<td>Soft ESD Phenomena in GMR Heads in the HDD Manufacturing Process</td>
</tr>
<tr>
<td>Tag-at, R.N.</td>
<td>2010</td>
<td>A Study on the Application of On-Chip EOS/ESD Full-Protection Device for TMR Heads</td>
</tr>
<tr>
<td>Taka, T.</td>
<td>2015</td>
<td>Electrically Conductive Polypropylene-Polyaniline Blend in ESD Protection</td>
</tr>
<tr>
<td>Takahara, M.</td>
<td>2005</td>
<td>ESD Protection Network Evaluation by HBM and CDM (Charged Package Method)</td>
</tr>
<tr>
<td>Takahashi, K.</td>
<td>2015</td>
<td>Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply RCJ</td>
</tr>
<tr>
<td>Takahashi, T.</td>
<td>2014</td>
<td>Visualization Technology to Capture an ESD Event</td>
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<tr>
<td>Takahashi, Y.</td>
<td>2006</td>
<td>A Resistive Ferrite Substrate for the GMR Head in Helical-scan Tape Systems</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Occurrence and Modes of Approaching Discharges and Separating Discharges - Characteristic Features of Electrostatic Discharges</td>
</tr>
<tr>
<td>Takai, T.</td>
<td>2011</td>
<td>Characteristic of Radiated Electromagnetic Wave by ON/OFF Discharge on Sub-Micron Gap</td>
</tr>
<tr>
<td></td>
<td></td>
<td>One of the Methods of Observing ESD around Electronic Equipment</td>
</tr>
<tr>
<td>Takaoka, H.</td>
<td>2005</td>
<td>A Study of Relation between a Power Supply ESD and Parasitic Capacitance</td>
</tr>
<tr>
<td>Takatsuji, W</td>
<td>2013</td>
<td>Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate</td>
</tr>
<tr>
<td>Takaya, S.</td>
<td>2014</td>
<td>CDM Protection of a 3D TSV Memory IC with a 100 GB/s Wide I/O Data Bus</td>
</tr>
<tr>
<td>Takekuma, H.</td>
<td>2006</td>
<td>A Resistive Ferrite Substrate for the GMR Head in Helical-scan Tape Systems</td>
</tr>
<tr>
<td>Takeuchi, M.</td>
<td>2006</td>
<td>Development of Ion Balance Sensor by using MOSFET</td>
</tr>
<tr>
<td>Takita, Y.</td>
<td>2016</td>
<td>Mirrored Power Distribution Network Noise Injection for Soft Failure Root Cause Analysis</td>
</tr>
<tr>
<td>Talbot, J.W.</td>
<td>86238</td>
<td>The Effect of ESD on LED III-V Materials</td>
</tr>
<tr>
<td>Talbot, V.M.</td>
<td>96227</td>
<td>Vanadium Pentoxide Based Antistatic Coatings</td>
</tr>
</tbody>
</table>
Tam, A.
2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation

Tamm, H.
20175A3 Correlation Study of Different CDM Testers and CCTLP

Tamminen, P.
2002250 ESD Control Tools for Surface Mount Technology and Final Assembly Lines
2003143 ESD Sensitivity of Devices on a Charged Printed Wiring Board
2005203 ESD Control in Automated Placement Process
2007202 Characterization of ESD Risks in an Assembly Process by Using Component Level CDM Withstand Voltage
2010267 Characterizing Slowly Dissipative Materials
2011202 Product Specific ESD Risk Analysis
2011279 Measurements and Simulations in Product Specific Risk Analysis
2012248 Low Level Human Body Model ESD
2012363 System Level ESD Discharges with Electrical Products
2013084 Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials
2014033 Optimizing Investment in ESD Control
2014206 Electrostatic Threats in Hospital Environment
2014375 ESD Sensitivity of 01005 Chip Resistors and Capacitors
20155B2 ESD and Disturbance Cases in Electrostatic Protective Areas
20156B1 Benchmarking of Factory Level ESD Control
20156B3 Uncertainties in Charge Measurements of ESD Risk Assessment
20157B2 The Effect of USB Ground Cable and Product Dynamic Capacitance on IEC61000-4-2 Qualification
20162B3 Charge Relaxation of Slowly Dissipative Polymers
20166B2 Charged Cable–System ESD Event
20171B4 Charged Device Discharge Measurement Methods in Electronics Manufacturing
20173A2 Charged Device ESD Threats with High Speed RF Interfaces
20174B1 Qualification Challenges of Footwear and Flooring Systems
20174B2 The Main Parameters Affecting Charged Device Discharge Waveforms in CDM Qualification and Manufacturing
20174B3 Electrostatic Discharge Characteristics of Conductive Polymers

Tan, D.
2001120 Controlling ESD Damage of ICs at Various Steps of Back-End Process

Tan, J.
2000060 Detecting ESD Events using a Loop Antenna

Tan, P.
2011100 Small Footprint ESD Protection of Hot-Swappable I/Os

Tan, P.Y.
2002183 A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology
2002382 Copper Interconnect Microanalysis and Electromigration Reliability Performance due to the Impact of TLP ESD
2005413 PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latch-up Robustness

Tan, W.H.
93057 Minimizing ESD Hazards in IC Test Handlers and Automatic Trim/Form Machines
94013 Implementing an ESD Program in a Multi-National Company: A Cross-Cultural Experience
94022 Evaluating and Qualifying Automated Test Handlers in a Semiconductor Company
95134 ESD Control Program: A Viewpoint from the Receiving End
95218 Use of Static-Safe Polymers in Automated Handling Equipment
95236 Carbon Loaded Device Handling Trays: Analysis and Measurements
97049 Non-Particulate Static Dissipative Polymers Used in Wafer Handling Equipment
98233 Magneto Optical Static Event Detector
99168 Test Methodologies for Detecting ESD Events in Automated Processing Equipment
2001149 DC Transient Monitoring and Analysis to Prevent EOS in Burn-in Systems
Tan, Y.C. 2002183 A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology

Tanabe, H. 2006104 Study on EMI Phenomena for GMR/TMR Head

Tanabe, T. 2007237 Noise Characteristics of MOSFET Ionizer Balance Sensor

Tanaka, H. 2007107 Study on High Field Transfer Curves of GMR Heads with Damaged Pinned Layer by ESD

Tanaka, K. 2008290 A Study of Advanced Technique on RC-Triggered NMOSFET Power Clamp

Tanaka, M. 92076 An Advanced ESD Test Method for Charged Device Model
94170 Clarification of Ultra-High-Speed Electrostatic Discharge and Unification of Discharge Model
96054 CDM ESD Test Considered Phenomenons of Division and Reduction of High Voltage Discharge in the Environment
20163A1 Area-Efficient ESD Design Using Power Clamps Distributed Outside I/O Cell Ring

Tanaka, S. 2010369 Anomalous ESD Failures in MLDMOS during Reverse Recovery

Tandan, N. 94120 ESD Trigger Circuit

Tang, H. 2000105 Comparison and Correlation of ESD HBM (Human Body Model) Obtained Between TLPG, Wafer-Level, and Package-Level Tests
2009028 Whole-Chip ESD Protection Design Verification by CAD

Taniguchi, H. 2001306 Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group

Tanitsuji, K. 2011338 Characteristic of Radiated Electromagnetic Wave by ON/OFF Discharge on Sub-Micron Gap

Tanner, D.M. 2001238 Human Body Model, Machine Model, and Charged Device Model ESD Testing of Surface Micromachined Microelectromechanical

Tanno, M. 2004075 Evaluation of ESD Hardness of Fingerprint Sensor LSIs

Tao, R. 2000202 The Effect of Bonding Sequence on GMR ESD Protection
2000327 Threshold of ESD Damage to GMR Sensor
2001295 A Study of GMR Breakdown Damage in Cleaning
2002332 ESD Damage by Arcing near GMR Heads

Tappura, K. 2002250 ESD Control Tools for Surface Mount Technology and Final Assembly Lines

Tarvainen, T. 2007318 Simulation and Physics of Charged Board Model for ESD

Tasca, D.M. 81174 Pulse Power Response and Damage Characteristics of Capacitors

Tasker, P.J. 97027 Novel Concept for High Level Overdrive Tolerance of GaAs Based FETs
Tatsumi, T.
20166A1 Ultra-Low Standby Current ESD Clamp MOSFET with P/N Hybrid Gate

Taylor, G.
2003250 Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design

Taylor, R.G.
81097 Input Protection Design for the 3 Micro NMOS Process
83185 ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics [BPP]
84165 Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
84189 A Failure Analysis Methodology for Revealing ESD Damage to Integrated Circuits
85141 Deficiencies in ESD Testing Methodology Highlighted by Failure Analysis
86092 Junction Degradation and Dielectric Shorting: Two Mechanisms for ESD Recovery

Taylor, T.
89190 Input Protection Design for Overall Chip Reliability

Tazzoli, A.
2006274 Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
2007058 CDM Circuit Simulation of a HV Operational Amplifier Realized in 0.35µm Smart Power Technology
2007264 ESD Robustness of AIGaN/Gan HEMT Devices
2008059 Electrostatic Discharge Effects in Fully Depleted SOI MOSFETs with Ultra-Thin Gate Oxide and Different Strain-Inducing Techniques
2008211 Novel 190V LiGBT-Based ESD Protection for 0.35µm Smart Power Technology Realized on SOI Substrate
2008272 EOS/ESD Sensitivity of Functional RF-MEMS Switches
2009240 Application of 3D Electromagnetic Modeling to ESD Design and Control for Class 0 Devices
2009257 EOS/ESD Sensitivity of Phase-Change-Memories
2010433 A Comprehensive Study of MEMS Behavior under EOS/ESD Events: Breakdown Characterization, Dielectric Charging, and Realistic
2011171 A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts
2012240 A µ-TLP System Realized in MEMS Technology
20154A3 Active Clamps with Hybrid BJT-CMOS Operation Mode
20157A2 Engineering of Dual-Direction SCR Cells for Component and System Level ESD, Surge, and Longer EOS Events
20166B1 PMOS Arrays Self-Protection Capability Limitation

Tcherniaev, A.
2009204 2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses
2010301 Study of Power Arrays in ESD Operation Regimes

Teague, E.
2010317 Problematic Natural Gas Power Plant Pumping/Irrigation

Teene, M.
89175 A "Waffle" Layout Technique Strengthens the ESD Hardness of the NMOS Output Transistor

Templar, L.C.
81151 EOS/ESD Failure Threshold Analysis Errors, Their Source, Size and Control

Teng, T.
79168 Susceptibility of LSI MOS to Electrostatic Discharge at Elevated Temperature
80087 LSI Design Considerations for ESD Protection Structures Related to Process and Layout Variations

Teng, Z.Y.
2001295 A Study of GMR Breakdown Damage in Cleaning
2002332 ESD Damage by Arcing near GMR Heads
2004346 Breakdown Behavior of TMR Head in ESD Transients
2006108  Breakdown Evaluation of Ultrathin Barrier Magnetic Tunnel Junctions with V-Ramp Testing
2007111  Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions
2011323  Machine Model Evaluation and Interconnect Effect Study for TMR HGA

Tennyson, M.
95013   Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junctions

Tenzer, F.D.
81044   An Analysis of Antistatic Cushioning Materials

Ter Beek, M.
2002101  Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway
2004117  Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application
2006039  Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications

Terashige, T.
2002240  Noise Reduction of Corona Discharge Air Ionizer
2006235  Development of Ion Balance Sensor by using MOSFET
2007237  Noise Characteristics of MOSFET Ionizer Balance Sensor
2008174  Electrostatic Control System Using Ceramic Transformer
2009055  Space Charge Balance Sensing for Static Control
2010273  Neutralizing Current Sensor for AC Corona Ionizer
2013037  Basic Characteristics of the Field Assisted Air Ionizer

Terauchi, T.
98018   Controlling ESD and Absorbing and Shielding EMW by Using Conductive Fiber in Aircraft

Terol, G.
94301   A Comparative Study of "Low Cost" 1.3 µm Laser Diodes: ESD Performance

Tesarek, P.
2000481  Floating Gate EEPROM as EOS Indicators during Wafer-Level GMR Processing

Testin, A.
2009387  Human Metal Model (HMM) Testing, Challenges to Using ESD Guns

Tew, C.P.
2003291  Exploring a Clean ESD Laminate & Ionic Contamination Methodology

Thean, A.
20151A3  VFTLP Characteristics of ESD Protection Diodes in Advanced Bulk FinFET Technology
20151A4  ESD Characterization of Diodes and ggMOS in Germanium FinFET Technologies
20166A2  VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires

Theis, T.L.
97188   ESD Program Auditing: The Auditor's Perspective

Thiemann, U.

Thijis, S.
2003195  Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits
2003242  Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2004040  ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions
2004098  Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies
2004316  Multilevel Transmission Line Pulse (MTLP) Tester
2005025  Class 3 HBM and Class M4 ESD Protected 5.5 GHz LNA in 90nm RF CMOS using Above – IC Inductor
2005152  Transient Voltage Overshoot in TLP testing - Real or Artifact?
2007053  Voltage Overshoot Study in 20V DeMOS-SCR Devices
Thurmer, D.
20159A3 Source of Miscorrelation of Product Level HBM to TLP Test Results

Thurmer, J.
96338 Functional Methods to Determine the EPA Compatibility of Mechanical Tools
20162B1 Electrostatic Shock Risks in Assembly of Large Wind Turbine Blades

Thys, G.
2014282 Anti-Series GgNMOS ESD Clamp for Space Application IC’s

Tian, G-C.
2011285 A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal Ics

Tian, H.
2000202 The Effect of Bonding Sequence on GMR ESD Protection
99315 ESD Protection of GMR Heads in Manufacturing
99380 ESD Damage of GMR Sensors at Head Stack Assembly

Tian, Y.
2010001 A Scalable Verilog-A Modeling Method for ESD Protection Devices

Tiebout, M.
2005033 RF ESD Protection Strategies: Co-design vs. Low-C Protection
2008221 ESD Concept for High-Frequency Circuits

Ting, L.M.
2001445 Integration of TLP Analysis for ESD Troubleshooting
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004141 Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems
2004146 The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps
2006024 HBM Stress of Non-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed
2006353 HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins

Titus, R.
90214 Dependence of Input ESD Failure Thresholds on IC Design Style

Todoroki, S.
2001306 Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group

Togari, H.
96365 Electrostatic Problems in TFT-LCD Production and Solutions Using Ionization

Tokunaga, T.
2009055 Space Charge Balance Sensing for Static Control

Tomibe, J.
98018 Controlling ESD and Absorbing and Shielding EMW by Using Conductive Fiber in Aircraft

Tong, M.H.
96280 Study of Gated PNP as an ESD Protection Device for Mixed-Voltage and Hot-Pluggable Circuit Applications

Tong, P.
2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation

Tonoya, Y.
93009 Impulsive ESD Noise Occurred From an Office Chair
94164 Impulsive EMI Effects from ESD on Raised Floor
96327 Study of ESD Quench Effects by Air Ionization

Topolski, A.S.
81065 Incoming Inspection of Antistatic Packaging Materials
Torres, C.A.
2001082  Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies
2003017  Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies
2010075  TLP Characterization for Testing System Level ESD Performance

Torres, R.
2006131  A New Electrical Overstress (EOS) Test for Magnetic Recording Heads

Tournier, D.
20152A1  An Electrostatic-Discharge-Protection Solution for Silicon-Carbide MESFET

Tran-Quinn, T.
2009286  Using VFTLP Data to Design for CDM Robustness
20155A2  3D Integration ESD Protection Design and Analysis

Trémouilles, D.
2002281  Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN
2004174  ESD Induced Latent Defects in CMOS ICs and Reliability Impact
2005152  Transient Voltage Overshoot in TLP testing - Real or Artifact?
2006039  Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications
2007089  Calibrated Wafer-Level HBM Measurements for Quasi-Static and Transient Device Analysis
2007158  Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions
2007242  T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology
2007408  Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications
2008295  Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets
2009059  Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness
2009076  Electrical and Thermal Scaling Trends for SOI FinFET ESD Design
2009165  Accurate Transient Behavior Measurement of High-Voltage ESD Protections Based on a Very Fast Transmission-Line Pulse System
2009273  ESD Events in SiN RF-MEMS Capacitive Switches
2010127  Building-up of System Level ESD Modeling: Impact of a Decoupling Capacitance on ESD Propagation
2011045  High Temperature Operation MOS-IGBT Power Clamp for Improved ESD Protection in Smart Power SOI Technology
2011241  Investigation of Statistical Tools to Analyze Repetitive HMM Stress Endurance of System-Level ESD Protection
2011329  ESD System Level Characterization and Modeling Methods Applied to a LIN Transceiver
2011343  Investigating the Probability of Susceptibility Failure within ESD System Level Consideration
2013258  Transient-TLP (T-TLP): A Simple Method for Accurate ESD Protection Transient Behavior Measurement
20152A1  An Electrostatic-Discharge-Protection Solution for Silicon-Carbide MESFET

Trevino, O.
2001445  Integration of TLP Analysis for ESD Troubleshooting

Trigonis, A.C.
85175  ESD Experience with the IRAS Spacecraft

Trinh, C.S.
2003250  Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design
2004289  ESD Protection Solutions for High Voltage Technologies

Trivedi, N.
2009292  A DRC-Based Check Tool for ESD Layout Verification
2011307  An Automated Approach for Verification of On-Chip Interconnect Resistance for Electrostatic Discharge Paths
2013174  Optimized Netlist Checks – Full Chip ESD Verification
2013305  CDM Single Power Domain Failures in 90 nm
20153A1  Essential – Integration of ESD Verification Methodologies
20165B3  EDA Approaches in Identifying Latch-up Risks
20173B4  Influence of Self-Heating on ESD Current Distribution in Metal Lines
Troussier, G.

2011082 Matrix Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology
2013199 Point to Point ESD Protection Network, a Flexible and Competitive Strategy Demonstrated in Advanced CMOS Technology

Tsaggaris, D.

2008001 Effect of Flip-Chip Package Parameters on CDM Discharge
2011100 Small Footprint ESD Protection of Hot-Swappable I/Os

Tsai, A.

98161 ESD-Related Process Effects in Mixed-Voltage Sub-0.5 μm Technologies

Tsai, C.

98281 Substrate Resistance Modeling and Circuit-Level Simulation of Parasitic Device Coupling Effects for CMOS I/O Circuits under ESD

Tsai, C.K.

2004160 Latch-up Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product

Tsai, C-C.

2013357 An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs

Tsai, M-F.

20157A3 Investigation and Solution to the Early Failure of Parasitic NPN Triggered by the Adjacent PNP ESD Clamps
20163A2 An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology

Tsai, M-H.

2012331 Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process

Tsai, S-Y.

2012331 Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process

Tsai, T-C.

2012324 High-k Metal Gate-Bounded Silicon Controlled Rectifier for ESD Protection
2013015 High CDM Resistant Low-Cap SCR for 0.9 V Advanced CMOS Technology
2013278 Novel Isolation Ring Structure for Latch-up and Power Efficiency Improvement of Smart Power Ics
2014349 High Flexibility SCR Clamp for ESD Protection in BCD Power Technology
20159A3 Source of Miscorrelation of Product Level HBM to TLP Test Results
20167A1 Physics of SOA Degradation Phenomena in Power Transistors under ESD Conditions
20175B1 Schottky LDN MOS for HV ESD Protection

Tsan, J.

20171B3 An ESD Case Study with High Speed Interface in Electronics Manufacturing and its Future Challenge

Tsao, R.R.

92019 An Evaluation of Air Ionizers for Static Charge Reduction and Particle Emission

Tseng, J.

200413 ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors

Tseng, J.C.

2004160 Latch-up Test-Induced Failure within ESD Protection Diodes in a High-Voltage CMOS IC Product
2011116 CDM Protection for Millimeter-Wave Circuits
2011267 A Contribution to the Evaluation of HMM for IO Design
2012324 High-k Metal Gate-Bounded Silicon Controlled Rectifier for ESD Protection
2012331 Design of ESD Protection Cell for Dual-Band RF Applications in a 65-nm CMOS Process
2013015 High CDM Resistant Low-Cap SCR for 0.9 V Advanced CMOS Technology
2013357 An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs
20157A3 Investigation and Solution to the Early Failure of Parasitic NPN Triggered by the Adjacent PNP ESD Clamps
20163A2 An On-Chip Combo Clamp for Surge and Universal ESD Protection in Bulk FinFET Technology
Tseng, W-J
20171A1 DNW-Controllable Triggered Voltage of the Integrated Diode Triggered SCR (IDT-SCR) ESD Protection Device

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Tsukuda, M.
20163A1 Area-Efficient ESD Design Using Power Clamps Distributed Outside I/O Cell Ring

Tsuruta, J.
2011094 CDM Secondary Clamp of RX and TX for High Speed SerDes Application in 40 nm CMOS Technology

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90162 Experimental & Theoretical Studies of EOS/ESD Oxide Breakdown in Unprotected MOS Structures
92112 Parametric Drift in Electrostatically Damaged MOS Transistors

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2001160 Field-Induced Charging and FIM ESD Tests on GMR Heads in Hard Disk Assembly
2001281 A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots
2004200 CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
2006240 Trends in External Ionizer Monitoring and Control

Turkman, I.R.
85077 Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstressings: A Model
85092 Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Wunsch-Bell Model
87158 A Novel On-Chip ESD Protection Device Using Static Induction Transistor Principle

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2013338 Evaluating Electrostatic Damage Prevention Methods for Full-Scale Reticle Manufacturing

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80095 Electrostatic Sensitivity of Various Input Protection Networks

Tweet, A.
82145 An Effective Electro-Static Discharge Protection Program

Twerefour, S.
95175 A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices

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80054 Identification of Latent ESD Failures
81014 Analysis of Electrostatic Discharge Failures
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Tyberg, C.
20155A2 3D Integration ESD Protection Design and Analysis

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94085 Charged Device Damage of PLCCs inside an Antistatic Shipping Tube - A Case History

Uchida, H.
2000152 New Methods for Measuring Resistance and Charge decay of Worksurfaces
97163 Control of Static Charge on Personnel in an Electronics Working Area
98245 Wrist Strap Designs and Comparison of Test Results According to MIL-PRF-87893 and ANSI EOS/ESD Association S1.1

Ueno, S-I.
20171A4 Oscillation of RC Power Clamp Inside IC Package
<table>
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<tr>
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<th>Title</th>
</tr>
</thead>
<tbody>
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<td>Ueno, Y</td>
<td>Real-Time Visualization Measurement of Electrostatic Potential on the Surface of a Dielectric Plate with a Small Charged Metal Plate</td>
</tr>
<tr>
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</tr>
<tr>
<td>Ujiie, S.</td>
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</tr>
<tr>
<td>Ukkonen, L.</td>
<td>ESD Sensitivity of 01005 Chip Resistors and Capacitors</td>
</tr>
<tr>
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<td>ESD and Disturbance Cases in Electrostatic Protective Areas</td>
</tr>
<tr>
<td></td>
<td>The Effect of USB Ground Cable and Product Dynamic Capacitance on IEC61000-4-2 Qualification</td>
</tr>
<tr>
<td>Umemura, E.</td>
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<tr>
<td>Unger, B.A.</td>
<td>ESD Damage from Triboelectrically Charged IC Pins</td>
</tr>
<tr>
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<td>Evaluation of Integrated Circuit Shipping Tubes [BPP]</td>
</tr>
<tr>
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<td>ESD by Static Induction</td>
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<td>The March of the EOS/ESD Ducks</td>
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<td>Interconnects for Device ESD Protection</td>
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<tr>
<td></td>
<td>Device Charging in Shipping Packages</td>
</tr>
<tr>
<td>Unikovski, A.</td>
<td>Empirical ESD Models for Cascode ESD Transistors</td>
</tr>
<tr>
<td>Upadhyaya, P.</td>
<td>Effect of Delay in Package Traces on CDM Stress and Peak Current</td>
</tr>
<tr>
<td>Ura, M.</td>
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</tr>
<tr>
<td>Uribeta, A.</td>
<td>Sensitivity Study to EOS/ESD of Bipolar Integrated Circuits</td>
</tr>
<tr>
<td>Utzig, J.</td>
<td>An Off-Chip ESD Protection for High-Speed Interfaces</td>
</tr>
<tr>
<td>Vaidya, R.</td>
<td>Interrogation of Damage-State in Lead-free Electronics under Sequential Exposure to Thermal Aging and Thermal Cycling</td>
</tr>
<tr>
<td>Vaidyanathan, S.</td>
<td>Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node</td>
</tr>
<tr>
<td>Vakiparta, K.</td>
<td>Electrically Conductive Polypropylene-Polyaniline Blend in ESD Protection</td>
</tr>
</tbody>
</table>
Van Camp, B.
2004289 ESD Protection Solutions for High Voltage Technologies
2005372 SCR Based ESD Protection in Nanometer SOI Technologies
2005393 Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies Avoiding Competitive
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2008325 CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between I/O Test Chips and Product Level
20175B3 Low Capacitive Dual Bipolar ESD Protection

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2001228 Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection

Van den Bempt, L.
92228 On Chip Electrostatic Discharge Protections for Inputs, Outputs and Supplies of CMOS Circuits
94307 Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit

van den Berg, A.
2002267 ESD Protection by Keep-On Design for a 550 V Fluorescent Lamp Control IC with Integrated LDMOS Power Stage

Van den Bergh, S.
97076 ESD Entry Points: Coaxial Cables vs. Shielding Apertures

Van der Borgh, J.
2011016 Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in a 40 nm Pure 1.8V Process

van der Vlist, H.
90157 Simulation of Thermal Runaway during ESD Events

Van Hoof, C.
2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors
2009265 A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response under EOS-ESD Stress

Van Hove, M.
2011147 HBM ESD Robustness of GaN-on-Si Schottky Diodes

van IJzerloo, A.
2010341 Pitfalls for CDM Calibration Procedures

Van Laecke, A.
2002092 Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)

Van Lint, V.A.
80149 Solar Cell Electrical Overstress Analysis
81229 Electrical Overstress Damage in Silicon Solar Cells

van Maasakkers, M.
2010083 On-Chip System ESD Protection of FM Antenna Pin

van Roozendaal, L.
90119 Standard ESD Testing of Integrated Circuits
90143 An Analysis of Low Voltage ESD Damage in Advanced CMOS Processes

Van Steenwijk, G.
98096 High Voltage Resistant ESD Protection Circuitry for 0.5 μm CMOS OTP/EPROM Programming Pin

Van Wijmeersch, S
2011016 Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in a 40 nm Pure 1.8V Process
van Zwol, H.
2006077  ESD Protection for the High-Voltage CMOS Technologies
2007047  Designing HV Active Clamps for HBM Robustness
2008006  Gate Oxide Protection and ggNMOSTs in 65 nm

van Zwol, J.
2002267  ESD Protection by Keep-On Design for a 550 V Fluorescent Lamp Control IC with Integrated LDMOS Power Stage
2002354  The Impact of Substrate Resistivity on ESD Protection Devices
2003051  Transmission Line Pulsed Photo Emission Microscopy as an ESD Troubleshooting Method
2006136  Relations between System Level ESD and (vf-) TLP
2009292  A DRC-Based Check Tool for ESD Layout Verification

Vanden Bossche, M.
2011395  Using Directional Couplers to Overcome the Bandwidth Limitations of IV-Probes in TLP Measurements

Vandenbroeck, J.
92228    On Chip Electrostatic Discharge Protections for Inputs, Outputs and Supplies of CMOS Circuits
94307    Failure Analysis of CDM Failures in a Mixed Analog/Digital Circuit

Vandersteen, G.
2009405  On-Wafer Human Metal Model Measurements for System-Level ESD Analysis
2012051  Miscorrelation between IEC 61000-4-2 Type of HMM Tester and 50 Ohm HMM Tester
2012379  Mixed-Mode Simulations for Power-on ESD Analysis

Vannorsdel, K.
2004361  Electrostatic Discharge (ESD) Protection of Giant Magneto-resistive (GMR) Recording Heads with a Silicon Germanium Technology

Vanysacker, P.
2005372  SCR Based ESD Protection in Nanometer SOI Technologies

Varrot, M.
95034    Impact of I/O Buffer Configuration on the ESD Performance of a 0.5 µm CMOS Process

Vaserman, Y.
20165B1  Empirical ESD Simulation Flow for ESD Protection Circuits Based on Snapback Devices
20174A4  Empirical ESD Models for Cascode ESD Transistors

Vashchenko, V.A.
97013    Gate Burnout of Small Signal MODFETs at TLP Stress
97330    Electrical Filamentation in GGMOS Protection Structures
2002101  Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway
2004117  Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application
2005387  Implementation of High VT Turn-on in Low-Voltage SCR Devices
2006039  Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications
2006064  Dual-Direction Isolated NMOS-SCR Device for System Level ESD Protection
2007053  Voltage Overshoot Study in 20V DeMOS-SCR Devices
2007075  Implementation of Dual-Direction SCR Devices in Analog CMOS Process
2008196  Small Footprint Trigger Voltage Control Circuit for Mixed-Voltage Applications
2008204  Extreme Voltage and Current Overshoots in HV Snapback Devices during HBM ESD Stress
2008242  A Dual-Base Triggered SCR with Very Low Leakage Current and Adjustable Trigger Voltage
2009204  2.5-Dimensional Simulation for Analyzing Power Arrays Subject to ESD Stresses
2009344  System Level and Hot Plug-in Protection of High Voltage Transient Pins
2009364  Self-Protection Capability of Power Arrays
2009405  On-Wafer Human Metal Model Measurements for System-Level ESD Analysis
2010157  SCCF-System to Component Level Correlation Factor
2010293  Improving the ESD Self-Protection Capability of Integrated Power NLDNOS Arrays
2010301  Study of Power Arrays in ESD Operation Regimes
2010425  HBM Parameter Extraction and Transient Safe Operating Area
2011140  Active Clamp Implementation in Complementary BiCMOS Process with High Voltage BJT Devices
2011147  HBM ESD Robustness of GaN-on-Si Schottky Diodes
2012348  SCR Clamps with Transient Voltage Detection Driver
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Vassilev, V.
2001062  Analysis and Improved Compact Modeling of the Breakdown Behavior of Sub-0.25 Micron ESD Protection ggNMOS Devices
2002018  A 6mW, 1.5dB NF CMOS LNA for GPS with 3kV HBM ESD-Protection
2002111  Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices
2003195  Co-Design Methodology to Provide High ESD Protection Levels in the Advanced RF Circuits
2003242  Impact of Elevated Source Drain Architecture on ESD Protection Devices for a 90nm CMOS Technology Node
2004040  ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions
2004098  Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90nm CMOS Node Technologies
2004316  Multilevel Transmission Line Pulse (MTLP) Tester
2005152  Transient Voltage Overshoot in TLP testing - Real or Artifact?
2009322  Diode Isolation Concept for Low Voltage and High Voltage Protection Applications
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Vaughn, J.
2001281  A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots

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98001    New Injection Moldable ESD Compounds Based on Very Low Carbon Black Loadings
99251    Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing
2000139  Controlling ESD and Cleanliness by Using New Thermoplastic Compounds for Injection Molded and Corrugated Packaging Products

Velghe, R.
2011267  A Contribution to the Evaluation of HMM for IO Design
2012060  HMM Round Robin Study: What to Expect When Testing Components to the IEC 61000-4-2 Waveform

Velghe, R.M.D.A.
2001337  Diode Network Used as ESD Protection in RF Applications
2001426  The Application of Transmission Line Pulse Testing for the ESD Analysis of Integrated Circuits

Veloso, A.
2013022  ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices
2016A2   VFTLP Characteristics of ESD Devices in Si Gate-All-Around (GAA) Nanowires

Veltri, J.
96040    Recommendations to Further Improvements of HBM ESD Component Level Test Specifications [BPR]

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<thead>
<tr>
<th>Authors</th>
<th>Year</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>Venegas, R.</td>
<td>2002</td>
<td>Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices</td>
</tr>
<tr>
<td>Venkatasubramanian, R.</td>
<td>2014</td>
<td>Rail Clamp with Dynamic Time Constant Adjustment</td>
</tr>
<tr>
<td>Verbeyst, F.</td>
<td>2009</td>
<td>The Application of Large-Signal Calibration Techniques Yields Unprecedented Insight during TLP and ESD Testing</td>
</tr>
<tr>
<td></td>
<td>2011</td>
<td>Using Directional Couplers to Overcome the Bandwidth Limitations of IV-Probes in TLP Measurements</td>
</tr>
<tr>
<td>Verhaege, K.G.</td>
<td>9312</td>
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</tr>
<tr>
<td></td>
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<tr>
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<td></td>
<td>9630</td>
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</tr>
<tr>
<td></td>
<td>9830</td>
<td>Investigation into Socketed CDM (SDM) Tester Parasitics</td>
</tr>
<tr>
<td></td>
<td>2000</td>
<td>Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices</td>
</tr>
<tr>
<td></td>
<td>2000</td>
<td>TLP Calibration, Correlation, Standards, and New Techniques</td>
</tr>
<tr>
<td></td>
<td>2001</td>
<td>Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling</td>
</tr>
<tr>
<td></td>
<td>2002</td>
<td>GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes</td>
</tr>
<tr>
<td></td>
<td>2002</td>
<td>High Holding Current SCRs (HII-SCR) for ESD Protection and Latch-up Immune IC Operation</td>
</tr>
<tr>
<td></td>
<td>2002</td>
<td>Correlation Considerations II: Real HBM to HBM testers</td>
</tr>
<tr>
<td></td>
<td>2003</td>
<td>Active-Area-Segmentation (AAS) Technique for Compact, ESD Robust, Fully Silicided NMOS Design</td>
</tr>
<tr>
<td></td>
<td>2004</td>
<td>ESD Protection Solutions for High Voltage Technologies</td>
</tr>
<tr>
<td>Verleye, S.</td>
<td>2007</td>
<td>Characterizing the Transient Device Behavior of SCRs by Means of VFTLP Waveform Analysis</td>
</tr>
<tr>
<td>Verma, P.R.</td>
<td>2010</td>
<td>Engineering Fully Silicided Large MOSFET Driver for Maximum I(H) Performance</td>
</tr>
<tr>
<td>Vermillion, R.</td>
<td>9914</td>
<td>A Study of ESD Corrugated</td>
</tr>
<tr>
<td>Vermont, G.</td>
<td>2006</td>
<td>Concept for Bulk Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering</td>
</tr>
<tr>
<td></td>
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<td>On-Chip System ESD Protection of FM Antenna Pin</td>
</tr>
<tr>
<td>Verweij, J.F.</td>
<td>9426</td>
<td>Fast Turn-On of an NMOS ESD Protection Transistor; Measurements and Simulations</td>
</tr>
<tr>
<td>Viale, B.</td>
<td>2016</td>
<td>An Automated Tool for Chip-Scale ESD Network Exploration and Verification</td>
</tr>
<tr>
<td>Viheriäkoski, T.</td>
<td>2005</td>
<td>ESD Control in Automated Placement Process</td>
</tr>
<tr>
<td></td>
<td>2007</td>
<td>Characterization of ESD Risks in an Assembly Process by Using Component Level CDM Withstand Voltage</td>
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<tr>
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<td>2007</td>
<td>Simulation and Physics of Charged Board Model for ESD</td>
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<tr>
<td></td>
<td>2009</td>
<td>ESD Event Receiver for System Level Testing</td>
</tr>
<tr>
<td></td>
<td>2010</td>
<td>Characterizing Slowly Dissipative Materials</td>
</tr>
<tr>
<td></td>
<td>2011</td>
<td>Product Specific ESD Risk Analysis</td>
</tr>
<tr>
<td></td>
<td>2012</td>
<td>Triboelectrification of Static Dissipative Materials</td>
</tr>
<tr>
<td></td>
<td>2012</td>
<td>Low Level Human Body Model ESD</td>
</tr>
<tr>
<td></td>
<td>2013</td>
<td>Uncertainties in Surface Resistivity Measurements of Electrostatic Dissipative Materials</td>
</tr>
<tr>
<td></td>
<td>2014</td>
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</tbody>
</table>
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2017B3  Electrostatic Discharge Characteristics of Conductive Polymers

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87071  Cost Effective Failure Analysis Method for Detecting Failure Site Associated with Extremely Small Leakage

Virtanen, E.
95229  Electrically Conductive Polypropylene-Polyaniline Blend in ESD Protection

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88183  Communication Satellite Testing for ESD Effects

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92277  Shallow Trench isolation Double-Diode Electrostatic Discharge Circuit and Interaction with DRAM Output Circuitry
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94246  Three-Dimensional Transient Electrothermal Simulation of Electrostatic Discharge Protection Circuits
95043  Analysis of Snubber-Climped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors
95273  Failure Analysis of Shallow Trench Isolated ESD Structures
95322  ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads [BPP]
96101  Linewidth Control Effects on MOSFET ESD Robustness
96291  CMOS-ON-SOI ESD Protection Networks
97210  Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks
97316  ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced Semiconductor Technology
98151  Semiconductor Process and Structural Optimization of Shallow Trench Isolation- Defined and Polysilicon – Bound Source/Drain Diodes
99105  Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips
99212  A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies
2000029  Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuitry
2000239  Electrostatic Discharge Characterization of Epitaxial-Base Silicon-Germanium Heterojunction Bipolar Transistors
2001326  Silicon Germanium Heterojunction Bipolar Transistor ESD Power Clamps and the Johnson Limit
2001364  Influence of Process and Device Design on ESD Sensitivity of a Silicon Germanium Heterojunction Bipolar Transistor
2002052  Variable-Trigger Voltage ESD Power Clamps for Mixed Voltage Applications Using a 120 GHz/100 GHz (fT/fMAX) Silicon Germanium Heterojunction Bipolar Transistor with Carbon Incorporation
2002092  Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF)
2002296  An Automated Electrostatic Discharge Computer-Aided Design System with the Incorporation of Hierarchical Parameterized Cells in BiCMOS Analog and RF Technology For Mixed Signal Applications
2003214  The Effect of Deep Trench Isolation, Trench Isolation and Sub-collector Doping on the Electrostatic Discharge (ESD) Robustness of Radio Frequency (RF) ESD STI-Bound P+/N-Well Diodes in BiCMOS Silicon Germanium Technology
2003372  Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
2004057  Low-Voltage Diode-Configured SiGe: C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (fT/fMAX)
2004361  Electrostatic Discharge (ESD) Protection of Giant Magneto-resistive (GMR) Recording Heads with a Silicon Germanium Technology
2005090  The Influence of High Resistivity Substrates on CMOS Latch-up Robustness
2005100  Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies
2005108  The Influence of Implanted Sub-collector on CMOS Latch-up Robustness
2005131  Guard Rings: Theory, Experimental Quantification and Design
2006353  HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins
2008040  VF-TLP Round Robin Study, Analysis and Results
Activities Towards a New Transient Latch-up Standard

Volmerange, H.

An Improved EOS Conduction Model of Semiconductor Devices

Vora, S.

Application Level Investigation of System-Level ESD-Induced Soft Failures

Vosteen, W.

Analysis of Pulsed DC Ionizer Measurement Procedures with a CPM Using ESDA RP 3.11-2006.

Vosteen, W.E.

Alternate Uses for the Charged Plate Monitor
Measurement of Ionizer Performance - a New Approach

Vulliet, W.G.

Electrical Overstress Damage in Silicon Solar Cells

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Performance of Fiber Based ESD Protective Packaging

Wada, T.

The Dependence of Electrostatic Destruction Voltage on Device Structures of P-N Junctions and Insulated Films
Study of ESD Evaluation Methods for Charged Device Model
Study on EMI Phenomena for GMR/TMR Head

Wagieh, H.

Topology-Aware ESD Checking: A New Approach to ESD Protection

Wagner, A.

ESD Induced Leakage Current Increase of Diffused Diodes

Wagner, K.E.

Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses

Wagner, L.

Electrical Overstress (EOS) Power Profiles: A Guideline to Qualify EOS Hardness of Semiconductor Devices

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2000266 On-Chip ESD Protection Design by Using Polysilicon Diodes in CMOS Technology for Smart Card Applications
2005316 On-Chip System ESD Protection Design for STN LCD Drivers

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99385 A Study of Diode Protection for Giant Magnetoresistive Recording Heads

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Wang, X.
2007250 Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies
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2014027 Plant-level ESD Standards and the Practical Protection Engineering of China’s Electronics Manufacturing Industry
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82115  Electroactive Polymers as Alternate ESD Protective Materials

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20175A3  Correlation Study of Different CDM Testers and CCTLP
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Weber, U.
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<td>New Layout Scheme to Improve ESD Robustness of I/O Buffers in Fully-Silicided CMOS Process</td>
</tr>
<tr>
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<td>2010001</td>
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<tr>
<td></td>
<td>20176A3</td>
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<tr>
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<tr>
<td></td>
<td>93221</td>
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</tr>
<tr>
<td>Wei, Y.-L</td>
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</tr>
<tr>
<td>Wei, Z.G.</td>
<td>2010191</td>
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</tr>
<tr>
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<td>95141</td>
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</tr>
<tr>
<td>Weidner, E.</td>
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</tr>
<tr>
<td></td>
<td>2013174</td>
<td>Optimized Netlist Checks – Full Chip ESD Verification</td>
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<tr>
<td>Weight, M.E.</td>
<td>82145</td>
<td>An Effective Electro-Static Discharge Protection Program</td>
</tr>
<tr>
<td>Weijs, P.J.W.</td>
<td>2001228</td>
<td>Using Thin Emitters to Control BVceO Effects in Punch-Through Diodes for ESD Protection</td>
</tr>
<tr>
<td>Weil, G.</td>
<td>20151B1</td>
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<td></td>
<td>20151B3</td>
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<td></td>
<td>20174B4</td>
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<td>Weiss, G.H.</td>
<td>95194</td>
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<td></td>
<td>99178</td>
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<tr>
<td></td>
<td>2004153</td>
<td>Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps</td>
</tr>
<tr>
<td>Weitz, S.</td>
<td>2001281</td>
<td>A Study of the Electrical Properties of Polymeric Materials Used for Gloves and Finger Cots</td>
</tr>
<tr>
<td>Welander, A.</td>
<td>86081</td>
<td>Studies and Revelation of Latent ESD-Failsures</td>
</tr>
<tr>
<td>Weldon, J.C.</td>
<td>2000308</td>
<td>Engineering the Cascoded NMOS Output Buffer for Maximum Vt1</td>
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<td></td>
<td>2001082</td>
<td>Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies</td>
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<tr>
<td></td>
<td>2003017</td>
<td>Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies</td>
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<td></td>
<td>2004255</td>
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<tr>
<td></td>
<td>2005070</td>
<td>ESD Protection for Advanced CMOS SOI Technologies</td>
</tr>
<tr>
<td></td>
<td>2006186</td>
<td>Comprehensive ESD Protection for Flip-Chip Products in a Dual Gate Oxide 65nm CMOS Technology</td>
</tr>
</tbody>
</table>
Welker, R.W.  
2001288 Contact Transfer of Anions from Hands as a Function of the Use of Hand Lotions

Welsher, T.L.  
87059 Variations in Failure Modes and Cumulative Effects Produced by Commercial Human-Body-Model Simulators  
87078 The Metallurgical Study of ESD Damage in 256K DRAM Devices  
88015 Tape and Reel Packaging - An ESD Concern  
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92068 From Lightning to Charged-Device Model Electrostatic Discharges  
97139 Mitigating Electrostatic Discharge (ESD) in Solid CO₂, Pellet Cleaning of Printed Wiring Boards and Assemblies  
2012032 Progress towards a Joint ESDA/JEDEC CDM Standard: Methods, Experiments, and Results  
2012254 Sampling Pin Approaches for ESD Test Applications

Wen, S-J  
2013299 System Level EOS Case Studies not due to Excessive Voltages

Wendel, M.  
2000420 Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase  
2002073 Harnessing the Base-Pushout Effect for ESD Protection in Bipolar and BiCMOS Technologies  
2006214 Tunable Bipolar Transistor for ESD Protection of HV CMOS Applications  
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2013115 Thyristor Compact Model for ESD, DC and RF Simulation  
20153B3 ESD Failure Caused by Parasitic SCR in an Overvoltage Tolerant I/O

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87258 Statistical and Graphical Analyses of Oxide Thickness and ESD Failure Modes

Werner, A.  
2009308 Latent Damage Due to Multiple ESD Discharges

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99241 Interferometric Temperature Mapping during ESD Stress and Failure Analysis of Smart Power Technology ESD Protection Devices

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92095 A Newly Observed High Frequency Effect on the ESD Protection Utilized in a Gigahertz NMOS Technology

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2007273 Effect of Large Device Capacitance on FICDM Peak Current  
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2011155 CDM Event Simulation in SPICE: A Holistic Approach  
20176A4 Implementation Methodology of Industrial and Automotive ESD, EFT, and Surge Generator Models Which Predict EMC Robustness on

Whalen, J.J.  
79140 Square Pulse and RF Pulse Overstressing of UHF Transistors  
79147 Microwave Nanosecond Pulse Burnout Properties of One Micron MESFETS

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83181 A Summary of Most Effective Electrostatic Discharge Protection Circuits for MOS Memories and their Observed Failure Modes  
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2011007 A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction

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85055 The Elimination of Electrostatic Discharge Failures from Silicon Gate Logic Technologies

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2008178 Considerations for CPM Measurements of Fast Switching Ionizers

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2009059 Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness
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Wittman, J.
86069 Reversible Charge Induced Failure Mode of CMOS Matrix Switch

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2008249 ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors

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2001337 Diode Network Used as ESD Protection in RF Applications

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91098 Physics of Electro-Thermal Effects in ESD Protection Devices

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Wolfe, E.
2014312 Non-EOS Root Causes of EOS-Like Damage

Won, T.
93157 Two-Dimensional Electrothermal Simulations and Design of Electrostatic Discharge (ESD) Protection Circuit
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2001096  Automatic Layout Based Verification of Electrostatic Discharge Paths

Wong, C.Y.
2000485  Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach
2001175  A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)
2002147  Magnetoresistive Sensitivity Mapping (MSM) and Dynamic Electrical Test (DET) Correlation Study on GMR Sensor Induced by Low
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Wong, M.C.
2004346  Breakdown Behavior of TMR Head in ESD Transients

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2006116  Effect of Electrostatic Discharge on Tunneling Magnetoresistive Sensor

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Wong, W.
2009286  Using VFTLP Data to Design for CDM Robustness

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20162B2  Product Qualification & Degradation of Steel Toe ESD Footwear
20171B2  ESD Risk Assessment Considerations for Automated Handling Equipment

Woo, M.
2005380  Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90nm CMOS ASICs
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84165  Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors
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88047  ESD Latency: A Failure Analysis Investigation

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89089  ESD Polymer Alloys: a Novel Approach for Permanently Static Dissipative Thermoplastics

Woodward-Jack, J.
91045  Implementation of Computer-Based ESD Training: A Case Study Comparing the Computer Approach with Traditional Classroom

Woon, C-T-T
2012129  Implementing Air Ionizing Blower at KLA Tencor 2401 Metrology Tool Reduce Visual Inspection Failure for Semiconductor Wafers
Worley, E.R.
95013 Sub-Micron Chip ESD Protection Schemes Which Avoid Avalanching Junctions
98311 Ultra Low Impedance Transmission Line Tester
2000296 High Current Characteristics of Devices in a 0.18 μm CMOS Technology
2002062 Optimization of Input Protection Diode for High Speed Applications
2003372 Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)
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Wouters, J.
2014282 Anti-Series GgNMOS ESD Clamp for Space Application IC’s

Wrobel, T.F.
81229 Electrical Overstress Damage in Silicon Solar Cells

Wu, C.
80023 Electrostatic Discharge (ESD) Monitor Design

Wu, F.J.
99315 ESD Protection of GMR Heads in Manufacturing

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2000287 Breakdown and Latent Damage of Ultra-Thin Gate Oxides under ESD Stress Conditions

Wu, M-F
2013357 An Efficient Full-Chip ESD Paths Resistance Value Verification Flow for Large Scale Designs

Wu, S.
96291 CMOS-ON-SOI ESD Protection Networks

Wu, W.L.
2005018 ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process

Wu, Z.C.
97132 Measurements of Body Impedance for ESD
97135 Why the Human Body Capacitance is So Large

Wulfert, F.

Wunder, M.
88137 Electrical Overstress Testing of a 256K UVEPROM to Rectangular and Double Exponential Pulses

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2006172 Concept for Bulk Coupling in SOI MOS Transistors to Improve Multi-Finger Triggering
2007366 Characterizing the Transient Device Behavior of SCRs by Means of VFTLP Waveform Analysis

Wynants, J.
20154A2 An Off-Chip ESD Protection for High-Speed Interfaces

Xiang, S.
20175A2 An ESD Demonstrator System for Evaluating the ESD Risks of Wearable Devices
Xiao, G.
2007111 Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions

Xiao, Y.
20153B1 HBM Failures Induced by ESD Cell Turn-Off and Circuit Interaction with ESD Protection

Xiao, Y-P.
2011285 A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal ICs

Xiaobing, J.
98135 Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Xie, H.
2009028 Whole-Chip ESD Protection Design Verification by CAD

Xiong, W.
2005280 ESD Evaluation of the Emerging MuGFET Technology

Xu, C.
2009001 Prospects of Carbon Nanomaterials in VLSI for Interconnections and Energy Storage

Xu, P.P.
2014171 HBM Failure Diagnosis on a High-frequency Analog Design with Full-chip Dynamic ESD Simulation

Yamada, T.
2009038 ESD Parameter Extraction by TLP Measurement

Yamaguchi, M.
90111 The ARC Problem and Voltage Scaling in ESD Human Body Model

Yamaguchi, S.
2014197 Visualization Technology to Capture an ESD Event
2015RCJ Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply RCJ

Yamazaki, T.
2011088 Origin of It2 Drop Depending on Process and Layout with Fully Silicided ggMOS

Yan, G.
2007111 Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions

Yan, K.P.
2001125 An Effective ESD Protection System in the Back End (BE) Semiconductor Manufacturing Facility
2005220 An Alternative Method to Verify the Quality of Equipment Grounding
2006253 Is CO2 Bubbling (Carbonization) a Requirement at Semiconductor Wafer Sawing Process
2007212 ESD Concerns in Sawing Wafers with Discrete Semiconductor Devices
2008158 Experiences with an Alternative Method for Grounding Personnel during Sitting Operation
2009049 Automatic Handling Equipment - The Role of Equipment Maker on ESD Protection
2010211 ESD Protection Program at Electronics Industry - Areas for Improvement
2012215 Poor Grounding – Major Contributor to EOS
2013030 Semiconductor Back End Manufacturing Process – ESD Capability Analysis
2014039 An Effective ESD Program Management Based on $S_20.20$ plus ESD Capability/Risk Analysis
20164B3 Influence of Machine Configuration on EOS Damage during Wafer Cleaning Process
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<td>Yankelevich, A.</td>
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<td>Yap, B.C.</td>
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<td>Antistatic Masking Tapes for Solder Flux Reflow Processing of Printed Circuit Boards</td>
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<td>Development of a GAAS Solid State Model for High Power Applications</td>
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<td>Yeh, C.Y.</td>
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</table>
Yenni, Jr., D.M.  
79045 The Deficiencies in Military Specification MIL-B-81705: Considerations and a Simple Model for Static Protection  
82094 Test Methods for Static Control Products

Yezersky, G.  
2002209 An Automated Test of Tribocharging for Automotive Seating Fabric

Yin, L.G.  
2007111 Pulse Stress Testing for Ultra-thin MgO Barrier Magnetic Tunnel Junctions

Yin, S.  
96095 Identification of Electrical Over Stress Failures from Other Package Related Failures Using Package Delamination Signatures

Yokata, N.  
2007403 A Study for ESD Robustness of Cascoded NMOS Driver  
2008325 CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results between IO Test Chips and Product Level

Yoo, D.  
92159 PIN Photodetectors-The ESD Bottleneck in Laser Packages

Yoo, Y.H.J  
2008178 Considerations for CPM Measurements of Fast Switching Ionizers  
2012105 Comparing Room Ionization Technologies in FPD Manufacturing  
2013323 Electrostatic Control and its Analysis of Roller Transferring Processes in FPD Manufacturing

Yoo, K.  
93157 Two-Dimensional Electrothermal Simulations and Design of Electrostatic Discharge (ESD) Protection Circuit

Yoo, Y.J.  
2000407 A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process

Yoon, H.S.  
2000407 A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process

Yoon, S-H  
2013323 Electrostatic Control and its Analysis of Roller Transferring Processes in FPD Manufacturing

Yoshida, H.  
2001172 Field Emission Noise Caused by Capacitance Coupling ESD in AMR/GMR Heads

Yoshida, M.  
90177 Model of Leakage Current in LDD Output MOSFET Due to Low-Level ESD Stress

Yoshimizu, K.  
2010273 Neutralizing Current Sensor for AC Corona Ionizer

Yoshimochi, H.  
87153 Shield Effect of Electrically Conductive Materials against Electromagnetic Waves Radiated by Electrostatic Discharge

Yoshioka, S.  
2006235 Development of Ion Balance Sensor by using MOSFET

Yots, C.M.  
96028 ESD Induced Capacitor Shorts

Youn, S.Y.  
82157 ESD Minimization Technique for MOS Manufacturing Final Test Area

Young Kim, T.  
2008191 Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer
Young, A.  
2011285  A Predictive Full Chip Dynamic ESD Simulation and Analysis Tool for Analog and Mixed-Signal ICs

Young, D.  
99105  Electrostatic Discharge (ESD) Protection in Silicon-on-Insulator (SOI) CMOS Technology with Aluminum and Copper Interconnects in Advanced Microprocessor Semiconductor Chips  
2000029  Silicon-On-Insulator Dynamic Threshold ESD Networks and Active Clamp Circuity

Young, D.E.  
95194  Transient-induced Latch-up Testing of CMOS Integrated Circuits

Young, M.  
2000413  ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors

Young, P.A.  
81114  Electrical Overstress Investigations in Modern Integrated Circuit Technologies  
83056  Power Failure Modeling of Integrated Circuits

Young, W.  
2000097  A Method for Determining a Transmission Line Pulse Shape that Produces Equivalent Results to Human Body Model Testing Methods

Yu, B.  
95027  Punch-through Transient Voltage Suppressor for EOS/ESD Protection of Low-Voltage ICs

Yu, Ronghua  
20171A3  Enhanced nFinFET ESD Performance

Yu, S.  
89089  ESD Polymer Alloys: a Novel Approach for Permanently Static Dissipative Thermoplastics

Yue, W.  
98135  Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Zacher, D.  
96254  New Charged-Plate Monitor Design Offers Greater Flexibility

Zaengl, F.  
2005178  Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices

Zaharia, C.  
2001408  Development of an Experimental Platform to Study the Effect of Speed of Approach on the Electrostatic Discharge (ESD) Event

Zait, E.  
91191  ESD Attenuation by Thin Metal Films

Zajac, H.R.  
80058  Study of Effects of Electro-Static Discharge on Solid-State Devices

Zängl, F.  
2003122  High Abstraction Level Permutational ESD Concept Analysis  
2005245  SoC-A Real Challenge for ESD Protection?

Zanoni, E.  
2001102  Experimental Analysis and Electro-Thermal Simulation of Low- and High-Voltage ESD Protection Bipolar Devices in a Silicon-on-Insulator Bipolar-CMOS-DMOS Technology  
2001249  Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes  
2007264  ESD Robustness of AlGaN/Gan HEMT Devices
Zaridze, R.
95095 Calculation and Measurement of Transient Fields of Voluminous Objects
96203 Numerical Calculation of ESD

Zaza, I.
2000251 Investigation on Different ESD Protection Strategies Devoted to 3.3 V RF Applications (2 GHz) in a 0.18 µm CMOS Process

Ze, S.
2017A4 Scenarios of ESD Discharges to USB Connectors

Zeglen, T.
96351 Detection Hazards Caused by ESD - Case Study, Hazards in Silos

Zekert, S.
2012135 Chasing a Latent CDM ESD Failure by Unconventional FA Methodology

Zelcri, M.
2002348 Investigations for a Smart Power and Self-Protected Device under ESD Stress through Geometry and Design Considerations for

Zeng, R.
99315 ESD Protection of GMR Heads in Manufacturing
99380 ESD Damage of GMR Sensors at Head Stack Assembly

Zezulka, R.J.
89036 Tracking Results of an ESD Control Program within a Telecommunications Service Company

Zhan, C.R.
2009028 Whole-Chip ESD Protection Design Verification by CAD
2011035 New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications
2013232 High-Voltage Asymmetrical Bi-Directional Device for System-Level ESD Protection of Automotive Applications on a BICMOS Technology
20175B2 High-Performance Bi-Directional SCR Developed on a 0.13 um SOI-Based Smart Power Technology for Automotive Applications

Zhang, G.
2009028 Whole-Chip ESD Protection Design Verification by CAD
20167A1 Physics of SOA Degradation Phenomena in Power Transistors under ESD Conditions

Zhang, H.
20167A1 Physics of SOA Degradation Phenomena in Power Transistors under ESD Conditions

Zhang, L.Z.
2001175 A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping (MSM)
2002147 Magnetoresistive Sensitivity Mapping (MSM) and Dynamic Electrical Test (DET) Correlation Study on GMR Sensor Induced by Low

Zhang, W.
2013214 An Active MOSFET Rail Clamp Network for Component and System Level Protection

Zhang, X.
2010381 CDM Effect on a 65 nm SOC LNA
2013056 Design and Verification of a Novel Multi-RC-Triggered Power Clamp Circuit for On-Chip ESD Protection
20163A3 Novel Insights into the Power-off and Power-on Transient Performance of Power-Rail ESD Clamp Circuit

Zhang, Y.
2008185 Carbon Nanotube Plastic - Packaging Materials for Class 0 Device ESD Protection

Zhao, B.
2009028 Whole-Chip ESD Protection Design Verification by CAD
Zhao, F.G.
99380  ESD Damage of GMR Sensors at Head Stack Assembly
2000202  The Effect of Bonding Sequence on GMR ESD Protection
2000327  Threshold of ESD Damage to GMR Sensor

Zhao, H.
2009028  Whole-Chip ESD Protection Design Verification by CAD

Zhao, S.
2014384  Characterization Methods to Replicate EOS Fails
20161A4  PNP-eSCR ESD Protection Device with Tunable Trigger and Holding Voltage for High Voltage Applications

Zhiqing, L.
20159A3  Source of Miscorrelation of Product Level HBM to TLP Test Results

Zhou, J.
20174A1  Transient Electromagnetic Co-Simulation of Electrostatic Air Discharge
20175A2  An ESD Demonstrator System for Evaluating the ESD Risks of Wearable Devices
20176A3  On Secondary ESD Event Monitoring and Full-Wave Modeling Methodology

Zhou, Y.P.
2007175  Modeling Snapback of LVTSCR Devices for ESD Circuit Simulation Using Advanced BJT and MOS Models
2007273  Effect of Large Device Capacitance on FICDM Peak Current
2009017  Transient Safe Operating Area (TSOA) Definition for ESD Applications
2009028  Whole-Chip ESD Protection Design Verification by CAD
2010399  A New Method to Evaluate Effectiveness of CDM ESD Protection
2011155  CDM Event Simulation in SPICE: A Holistic Approach

Zhu, H.
2006131  A New Electrical Overstress (EOS) Test for Magnetic Recording Heads

Zhu, L.Y.
98351  ESD Prevention on an Unshunted MR Head
99367  ESD Damage by Directly Arcing to a MR Head

Zografos, O.
2012001  ESD Characterization of High Mobility SiGe Quantum Well and Ge Devices for Future CMOS Scaling
2013022  ESD Performance of High Mobility SiGe Quantum Well Bulk FinFET Diodes and pMOS Devices

Zonghan, W.
98135  Discussion on Electric Parameters of Standard for Anti-Electrostatic Floor

Zou, J.
2014027  Plant-level ESD Standards and the Practical Protection Engineering of China's Electronics Manufacturing Industry

Zu, Y.
2014298  Threshold Voltage Shift Due to Incidental Pulse on Non-Stressed Pins during HBM Testing
20163B2  Case Study of DPI Robustness of a MOS-SCR Structure for Automotive Applications

Zubeidat, M.
2003319  Test Circuits for Fast and Reliable Assessment of CDM Robustness of I/O Stages

Zulliano, L.
2003088  Characterization and Modeling of Transient Device Behavior under CDM ESD Stress
2004107  Study of CDM Specific Effects for a Smart Power Input Protection Structure
2006274  Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices
20162A1  HV ESD Diodes Investigation under vT-TLP Stresses: TCAD Approach
Zupac, D.
90137 ESD Effects on the Radiation Response of Power VDMOS Transistors
91151 Detection of ESD-Induced Non-Catastrophic Damage in P-Channel Power MOSFETs
92121 Annealing of ESD-induced Damage in Power MOSFETs

Zuri, L.
98001 New Injection Moldable ESD Compounds Based on Very Low Carbon Black Loadings
99251 Innovative ESD Thermoplastic Composites Structured Through Melt Flow Processing
2000139 Controlling ESD and Cleanliness by Using New Thermoplastic Compounds for Injection Molded and Corrugated Packaging Products

zur Nieden, F.
20154B3 Using CC-TLP to get a CDM Robustness Value
20164A3 Predict the Product Specific CDM Stress Using Measurement-Based Models of CDM Discharge Heads
20174A3 How to Build a Generic Model of Complete ICs for System ESD and Electrical Stress Simulation
SECTION 2
PAPER AWARDS
Best Paper 1979

79001 McAteer, O.J., Westinghouse Electric Corporation
An Effective ESD Awareness Training Program

Best Papers 1980

80073 Keller, J.K., AT&T Bell Laboratories
Protection of MOS Integrated Circuits from Destruction by Electrostatic Discharge

80192 Halperin, S.A., Analytical Chemical Laboratories
Facility Evaluation: Isolating Environmental ESD Problems

Best Paper 1981

81057 Unger, B.A., Chemelli, R.G., Bossard, P.R., Hudock, M.S., AT&T Bell Laboratories
Evaluation of Integrated Circuit Shipping Tubes

Best Presentation 1981

81021 Frank, D.E., Douglas Aircraft Company
The Perfect '10' - Can You Really Have One?

Best Paper 1982

82041 McAteer, O.J., Twist, R.E., Westinghouse Electric Corporation, Walker, R.C., SAR Associates
Latent ESD Failures

Best Presentation 1982

82142 Euker, R., Hewlett-Packard Company
ESD in I.C. Assembly (A Base Line Solution)

Best Paper 1983

83185 Enoch, D.R., Shaw, R.N., Taylor, R.G., British Telecom
ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics

Best Presentation 1983

83067 Mykkanen, C.F., Blinde, D.R., Honeywell, Inc.
The Room Air Ionization System, a Better Alternative than 40% Relative Humidity

Best Paper 1984

84179 DeChiaro, L.F., AT&T Bell Laboratories
Device ESD Susceptibility Testing and Design Hardening
Best Presentations 1984

84001  Dangelmayer, G.T., AT&T Technologies, Inc.
A Realistic and Systematic ESD Control Plan

84078  Holmes, G.C., Huff, P.J., Johnson, R.L., British Telecom
An Experimental Study of the ESD Screening Effectiveness of Anti-Static Bags

Best Paper 1985

85067  Pierce, D.G., Sandia National Laboratories
Electro-Thermomigration as an Electrical Overstress Failure Mechanism

Best Presentation 1985

85163  Amos, C.T., Stephens, C.E., British Telecom
A Technique for Real Time Examination of Sub-System ESD/EOS Damage in Integrated Circuits

Best Papers 1986

86159  Rubalcava, A.L., Stunkard, D., Roesch, W.J., TriQuint Semiconductor, Inc.
Electrostatic Discharge Effects on Gallium Arsenide Integrated Circuits

86166  Maloney, T.J., Intel Corporation
Contact Injection: A Major Cause of ESD Failure in Integrated Circuits

Best Presentation 1986

86173  McPhee, R.A., Duvvury, C., Rountree, R.N., Texas Instruments Inc., Domingos, H., Clarkson University
Thick Oxide Device ESD Performance under Process Variations

Best Papers 1987

87010  Lai, E.C., Plaster, J.S., Delco Electronics Corporation
ESD Control in the Automotive Electronics Industry - a Case Study

87252  Fong, Y., Hu, C., University of California, Berkeley
The Effects of High Electric Field Transients on Thin Gate Oxide MOSFETs

Best Presentation 1987

87186  Avery, L.R., RCA David Sarnoff Research Center
ESD Protection Structures to Survive the Charged Device Model (CDM)

Best Papers 1988

A Microwave-Bandwidth Waveform Monitor for Charged-Device Model Simulators

88206  Duvvury, C., Rountree, R.N., Texas Instruments Inc.
Output ESD Protection Techniques for Advanced CMOS Processes
Best Presentations 1988

88201  Rountree, R.N., Duvvury, C., Maki, T., Stiegler, H., Texas Instruments Inc.
A Process-Tolerant Input Protection Circuit for Advanced CMOS Processes

88103  Fowler, S.L., W.R. Grace and Co.
Triboelectricity and Surface Resistivity do not Correlate

Best Paper 1989

89059  Renniger, R.G., Jon, M.C., Lin, D.L., Diep,T., and Welsher, T.L., AT&T Bell Laboratories
A Field-induced Charged-Device Model Simulator

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Understanding Pink Poly

Best Paper 1990

90197  Maloney, T. J., Intel Corporation
Enhanced P+ Substrate Tap Conductance in the Presence of NPN Snapback

Best Presentation 1990

90218  Jaffe, M.D., and Cottrell, P.E., IBM General Technology Division
Electrostatic Discharge Protection for a 4-Mbit DRAM

Best Paper 1991

91127  Renninger, R.G., AT&T Bell Laboratories
Mechanisms of Charged-Device Model Electrostatic Discharges

Best Presentations 1991

91045  Woodward-Jack, J., Sommerfeld, H., Northern Telecom Electronics, Ltd.
Implementation of Computer-Based ESD Training: A Case Study Comparing the Computer Approach with Traditional Classroom Techniques

91210  Franey, J.P., and Freund, R.S., AT&T Bell Laboratories; Sias, R., Beamer, B., Baxter Industrial
A New Permanent ESD and Corrosion Resistant Material

Best Paper 1992

92168  Bock, K., Hartnagal, H., Technical University of Darmstadt, F.R.G.
Fieldemitter-Based ESD-Protection Circuits for High Frequency Devices and IC’s

Best Presentation 1992

92250  Krakauer, D., Mistry, K., Digital Equipment Corporation
ESD Protection in a 3.3V Sub-Micron Silicided CMOS Technology
Best Paper 1993

Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model

Best Presentation 1993

93109 Colvin, J., WSI, Inc.
The Identification and Analysis of Latent ESD Damage On CMOS Input Gates

Best Paper 1994

94237 Amerasekera, A., Duvvury, C., Texas Instruments, Inc.
The Impact of Technology Scaling On ESD Robustness and Protection Circuit Design

Best Presentation 1994

94063 Chaine, M., Liong, C., San, H., Texas Instruments, Inc.
A Correlation Study between Different Types of CDM Testers and "Real" Manufacturing In-Line Leakage Failures

Best Paper 1995

95322 Wallash, A., Hughbanks, T., IBM Storage Systems Division; Voldman, S., IBM Microelectronics Division
ESD Failure Mechanisms of Inductive and Magnetoresistive Recording Heads

Best Presentation 1995

95162 Duvvury, C., Amerasekera, A., Texas Instruments, Inc.
Advanced CMOS Protection Device Trigger Mechanisms During CDM

Best Paper 1996

96085 Gieser, H., Haunschild, M., Fraunhofer-Institut Festkorpertechnologie
Very-Fast Transmission Line Pulsing of Integrated Structures and the Charged Device Model

Best Presentation 1996

96040 Verhaege, K., David Sarnoff Research Center; Russ, C., Groeseneken, G., IMEC; Robinson-Hahn, D., Lin, D., Lucent Technologies; Farris, M., Intel; Scanlon, J., American Systems Corporation; Veltri, J., Digital
Recommendations to Further Improvements of HBM ESD Component Level Test Specifications

Best Paper 1997

97230 Chen, J., Amerasekera, A., Duvvury, C., Texas Instruments, Inc.
Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes
Best Presentation 1997

97316  Voldman, S., IBM Microelectronics Division
ESD Robustness and Scaling Implications of Aluminum and Copper Interconnects in Advanced Semiconductor Technology

Best Paper 1998

98161  V. Gupta, A. Amerasekera, S. Ramaswamy, A. Tsai, Texas Instruments, Inc.
ESD-Related Process Effects in Mixed-Voltage Sub-0.5 µm Technologies

Best Presentation 1998

98233  N. Jacksen, ExMod Corporation; W. Tan, AMD; D. Boehm, Novx Corporation
Magneto Optical Static Event Detector

Best Paper & Best Presentation 1999

99062  J. Smith, Motorola
An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Conduction During EOS/ESD Events

Best Paper 2000

2000308  J. Miller, M. Khazhinsky, J. Weldon, Motorola, Inc.
Engineering the Cascoded NMOS Output Buffer for Maximum Vt1

Best Presentation 2000

2000018  K. Verhaege, C. Russ, Sarnoff Corporation
Wafer Cost Reduction through Design of High Performance Fully Silicided ESD Devices

Best Paper 2001

2001082  C.A. Torres, J.W. Miller, M. Stockinger, M.D. Akers, M.G. Khazhinsky, J.C. Weldon, Motorola, Inc.
Modular, Portable, and Easily Simulated ESD Protection Networks for Advanced CMOS Technologies

Best Presentation 2001

Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling

Best Paper & Best Presentation 2002

2002257  G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.
Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 um ESD Protection Circuits
Best Paper & Best Presentation 2003

Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies

Best Paper 2004

ESD Protection for 5.5 GHz LNA in 90 nm RF CMOS – Implementation Concepts, Constraints and Solutions

Best Presentation 2004

2004255  M. G. Khazhinsky, J. W. Miller, M. Stockinger, J. C. Weldon, Freescale Semiconductor, Inc.
Engineering Single NMOS and PMOS Output Buffers for Maximum Failure Voltage in Advanced CMOS Technologies

Best Paper 2005

ESD Evaluation of the Emerging MuGFET Technology

Best Presentation 2005

2005043  G. Boselli, J. Rodriguez, C. Duvvury, J. Smith, Texas Instruments, Inc.
Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window

Best Paper 2006

2006284  A. Ille, Infineon Technologies and Universite de Provence-ISEN; W. Stadler, A. Kerber, T. Pompl, T. Brodbeck, K. Esmark, Infineon Technologies; A. Bravaix, Universite de Provence-ISEN
Ultra-thin Gate Oxide Reliability in the ESD Time Domain

Best Presentation 2006

2006024  H. Kunz, C. Duvvury, J. Brodsky, P. Chakraborty, A. Jahanzeb, S. Marum, L. Ting, J. Schichl, Texas Instruments, Inc
HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed Neighbor Pin
Best Paper 2007

2007357  T. Smedes, N. Guitard, NXP Semiconductors  
Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections during Fast Transients

Best Presentation 2007

2007283  A. Jahanzeb, Y-Y Lin, S. Marum, J. Schichl, C. Duvvury, Texas Instruments  
CDM Peak Current Variations and Impact upon CDM Performance Thresholds

Best Paper 2008

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A Study of Cable Discharge Events and Other Short Time Pulses of Cabled MR Sensors

Best Presentation 2008

2008030  Melanie Etherton, James Miller, Freescale Semiconductor, Inc.; Victor Axelrod, Haim Marom, Freescale Semiconductor Israel; Tom Meuse, Thermo Fisher Scientific  
HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike

Best Paper 2009

2009419  Wolfgang Stadler, Tilo Brodbeck, Josef Niemesheim, Reinhold Gaertner, Infineon Technologies AG; Kathleen Muhonen, Penn State Erie, The Behrend College  
Characterization and Simulation of Real-World Cable Discharge Events

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A DRC-Based Check Tool for ESD Layout Verification

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On the Dynamic Destruction of LDMOS Transistors beyond Voltage Overshoots in High Voltage ESD

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The Relevance of Long-Duration TLP Stress on System Level ESD Design
Best Paper 2011

2011187  Yiqun Cao, Infineon Technologies, Technische Universitat Dortmund; Ulrich Glaser, Joost Willemen, Filippo Magrini, Michael Mayerhofer, Matthias Stecher, Infineon Technologies; Stephan Frei, Technische Universitat Dortmund

ESD Simulation with Wunsch-Bell Based Behavior Modeling Methodology

Best Presentation 2011

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ESD Characterization of Atomically-Thin Graphene

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Chasing a Latent CDM ESD Failure by Unconventional FA Methodology

Best Paper & Best Presentation 2013

2013214  Michael Stockinger, Wenzhong Zhang, Kristen Mason, James Feddeler, Freescale Semiconductor

An Active MOSFET Rail Clamp Network for Component and System Level Protection

Best Paper 2014

2014242  Robert Mertens, Nicholas Thomson, Yang Xiu, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

Theory of Active Clamp Response to Power-On ESD and Implications for Power Supply Integrity

Best Presentation 2014

2014215  Reinhold Gärtner, Infineon Technologies; Wolfgang Stadler, Josef Niemesheim, Oliver Hilbricht, Intel Mobile Communications

Do Devices on PCBs Really See a Higher CDM-like ESD Risk?
Best Paper 2015

An Off-chip ESD Protection for High-speed Interfaces

Best Presentation 2015

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Low Impedance Contact CDM

Best Paper 2016

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Gun Tests of a USB3 Host Controller Board

Best Presentation 2016

2016A3  Friedrich zur Nieden, Kai Esmark, Stefan Seidl, Reinhold Gärtner, Infineon Technologies AG
Predict the Product Specific CDM Stress Using Measurement-Based Models of CDM Discharge Heads

2016B3  Michael Khazhinsky, Silicon Labs; Krzysztof Domanski, Harald Gossner; Intel; Guido Quax, Scott Ruth, NXP Semiconductors; Farzan Farbiz, Texas Instruments; Nitesh Trivedi, Infineon
EDA Approaches in Identifying Latch-up Risks
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79004 Storm, D.C., Aerospace Corporation
Controlling Electrostatic Problems in the Fabrication and Handling of Spacecraft Hardware

79007 Briggs, Jr., C., Charles Stark Draper Laboratory, Inc.
Electrostatic Conductivity Characteristics of Workbench-Top Surface Materials

79013 Halperin, S.A., Analytical Chemical Laboratories
Static Control Using Topical Antistats

79022 DerMarderosian, A., Rideout, L.B., Raytheon Company
The Generation of Electrostatic Charges in Silicone Encapsulants During Cyclic Gaseous Pressure Tests

79027 McMahon, E.J., Bhar, T.N., Reliability Sciences, Incorporated, Oishi, T., USN, Naval Sea Systems
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79045 Yenni, Jr., D.M., Huntsman, J.R., 3M Company
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79055 Branberg, G.A., Hewlett-Packard Company
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79078 King, W.M., Consultant
Dynamic Waveform Characteristics of Personnel Electrostatic Discharge

79088 Uetsuki, T., Mitani, S., Hitachi, Ltd.
Failure Analysis of Microcircuits Subjected to Electrical Overstress

Electrostatic Failure of X-Band Silicon Schottky Barrier Diodes

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ESD Susceptibilities of High Performance Analog Integrated Circuits

79109 Ward, A.L., Harry Diamond Laboratories
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Reverse-Bias Second Breakdown in Power Transistors

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79133 Kusnezov, N., Smith, J.S., Lockheed Palo Alto Research Laboratories
Modeling of Electrical Overstress in Silicon Devices

79140 Whalen, J.J., State University of New York at Buffalo, Domingos, H., Clarkson University
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Soden, J.M., Sandia National Laboratories
The Dielectric Strength of Silicon Dioxide in a CMOS Transistor Structure

Petrizio, C.J., RCA
Electrical Overstress Versus Device Geometry

Minear, R.L., Dodson, G.A., AT&T Bell Laboratories
The Phantom Emitter - an ESD-Resistant Bipolar Transistor Design and its Applications to Linear Integrated Circuits

Clark, O.M., General Semiconductor Industries, Inc.
Electrostatic Discharge Protection Using Silicon Transient Suppressors

Cabayan, H.S., Deadrick, F.J., Martin, L.C., Mensing, R.W., Lawrence Livermore National Laboratory
Statistical Failure Analysis of Military Systems for High Altitude EMP

Madison, J.A., Westinghouse Electric Corporation
The Analysis and Elimination of EOS Induced Secondary Failure Mechanisms

Berbeco, G.R., Charleswater Products, Inc.
Passive Static Protection: Theory and Practice

The Effects of High Humidity Environments on Electrostatic Generation and Discharge

Bosward, P.R., Chemelli, R.G., Unger, B.A., AT&T Bell Laboratories
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Transient Protection with ZnO Varistors: Technical Considerations

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Protective Level Comparisons for Voltage Transient Suppressors (120 V, AC Type)

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Gas Tube Surge Arresters for Control of Transient Voltages

McAteer, O.J., Twist, R.E., Westinghouse Electric Corporation, Walker, R.C., SAR Associates
Identification of Latent ESD Failures

Zajac, H.R., Tektronix, Inc.
Study of Effects of Electro-Static Discharge on Solid-State Devices

Alexander, D.R., Sandia National Laboratories, Enlow, E.W., Karaskiewicz, R.J., BDM Corporation
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Analysis of ESD Damage in JFET Preamplifiers

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SOS Protection - The Design Problem

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The Effects of VLSI Scaling on EOS/ESD Failure Threshold

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Input Protection Design for the 3 Micro NMOS Process

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Electrical Overstress Investigations in Modern Integrated Circuit Technologies


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Behavior of Thick-Film Power Resistors Subjected to Large Momentary Overloads

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EOS Threshold Determination of Electro-Explosive Devices

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Non-Linear Kinetics of Semiconductor Junction Thermal Failure
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Electrical Overstress Threshold Testing

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Latent ESD Failures [BPP]

A Survey of EOS/ESD Data Sources

Pierce, D.G., Booz, Allen & Hamilton, Inc.
Modeling Metallization Burnout of Integrated Circuits

Volmerange, H., TRW
An Improved EOS Conduction Model of Semiconductor Devices

Ward, A.L., Harry Diamond Laboratories
The Forward-Bias Characteristic as a Predictor and Screen of Reverse-Bias Second Breakdown

Yee, J.H., Orvis, W.J., Martin, L.C., Peterson, J.C., Lawrence Livermore National Laboratory
Modeling of Current and Thermal Mode Second Breakdown Phenomena

Pierce, D.G., Mason, Jr., R.M., Booz, Allen & Hamilton, Inc.
A Probabilistic Estimator for Bounding Transistor Emitter-Base Junction Transient-Induced Failures

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A Summary of Most Effective Electrostatic Discharge Protection Circuits for MOS Memories and their Observed Failure Modes

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ESD Sensitivity of NMOS LSI Circuits and their Failure Characteristics [BPP]

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A Study of ESD Latent Defects in Semiconductors

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ESD Damage, Does it Happen on PCBs?

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Electrostatic Measurement for Process Control

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Effects of Air Ions and Electric Fields on Health and Productivity

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A Room Ionization System for Electrostatic Charge and Dust Control

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Static-Electric Characterization of Semi-Insulating Materials

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Estimation of Discharge Energy Released From Charged Insulator

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A Material Evaluation Program for Decorative Static Control Table Top Laminates

Hohl, A.P., RCA David Sarnoff Research Center

A Wrist Strap Life Test Program


Testing of Electrostatic Materials Fed. Std. 101C, Method 4046.1

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Designing to Avoid Static - ESD Testing of Digital Devices

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EMI Characteristics of ESD in a Small Air Gap--ARP Governs the EMI--

Lafferty, D., Intel Corporation

Secondary Discharge: A New Jeopardy and a New Tool
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Protection of Components Against Electrical Overstress (EOS) and Transients in Monitors

An Evaluation of EOS Failure Models

Roberts, B.C., ERA Technology Ltd.
Determination of Threshold Energies and Damage Mechanisms in Semiconductor Devices Subjected to Voltage Transients

Shaw, R.N., Enoch, D.R., Taylor, R.G., Woodhouse, J., British Telecom
Degradation by ESD Transients of the Substrate Bias Voltage of NMOS 8085-Type Microprocessors

DeChiaro, L.F., AT&T Bell Laboratories
Device ESD Susceptibility Testing and Design Hardening [BPP]

Taylor, R.G., Woodhouse, J., Feasey, P.R., British Telecom
A Failure Analysis Methodology for Revealing ESD Damage to Integrated Circuits

Lin, C.M., Richardson, L.M., Chi, K.K., Simcoe, R.J., Digital Equipment Corporation
A CMOS VLSI ESD Input Protection Device, DIFIDW

Avery, L.R., RCA David Sarnoff Research Center
IC Technology: Where it is Going and What it Means for the ESD Industry

Renaud, D.P., Hill, H.W., IBM Corporation
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Integration of a Comprehensive Static Control Program Into an Automated Manufacturing Facility

Dangelmayer, G.T., Jesby, E.S., AT&T Technologies, Inc.
Employee Training for Successful ESD Control

Pelella, A.R., IBM Corporation, Domingos, H., Clarkson University
A Design Methodology for ESD Protection Networks

Korn, S.R., General Electric Company
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ESD Design Considerations for ULSI

Maloney, T.J., Khurana, N., Intel Corporation
Transmission Line Pulsing Techniques for Circuit Modeling

Wilcox, Jr., R.B., Doucette, R.E., IBM Corporation
The Elimination of Electrostatic Discharge Failures From Silicon Gate Logic Technologies

Jonassen, N., Technical University of Denmark
The Physics of Air Ionization

Pierce, D.G., Sandia National Laboratories
Electro-Thermomigration as an Electrical Overstress Failure Mechanism [BPP]

Neelakantaswamy, P.S., RIT Research Corporation, Sarkar, T.K., Turkman, I.R., Rochester Institute of Technology
Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstressings: A Model for Latent Failures

Bridgwood, M.A., Kelley, R.H., Clemson University
Modeling the Effects of Narrow Impulsive Overstress on Capacitive Test Structures

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ESD Control in the Factory of the Future or 20.20 to the Rescue
B. Unger, Burt Unger Associates
Device Charging in Shipping Packages

D. Stockin, Lyncole Industries, Inc.
Designing and Testing of Facilities Ground

J. Franey, Lucent Technologies Bell Labs
Corrosion Induced Electrostatic Damage

A. Rudack, M. Pendley, International SEMATECH; L. Levit, Ion Systems
Measurement Technique Developed to Evaluate Transient EMI in a Photo Bay With and Without Air Ionization

Y. Anand, D. Crowe, A. Feinberg, C. Jones, M/A-COM, Incorporated
Random GaAs IC’s ESD Failures Caused by RF Test Handler

J. Montoya, Intel Corporation; L. Levit, Ion Systems; A. Englisch, Dupont Photomasks
A Study of the Mechanisms for ESD Damage to Reticles

A Novel NMOS Transistor for High Performance ESD Protection Devices in a 0.18 µm CMOS Technology Utilizing Salicide Process

K-L Lei, C. Chu, J. Tseng, Y-M Chiang, M. Young, Advanced Custom Sensors, Inc.; G. Li, University of California
ESD Performance of Bridge-Resistance Pressure Diaphragm Sensors

K. Esmark, W. Stadler, M. Wendel, H. Gossner, X. Guggenmos, Infineon Technologies AG; W. Fichtner, ETH Zurich
Advanced 2D/3D ESD Device Simulation – A Powerful Tool Already Used in a Pre-Si Phase

Y. Wang, P. Juliano, S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign
Electrothermal Modeling of ESD Diodes in Bulk-Si and SOI Technologies

V. Puvvada, V. Srinivasan, V. Gupta, Texas Instruments (India) Ltd.
A Scalable Analytical Model for the ESD N-Well Resistor

M. Mergens, Bosch (now with Sarnoff Corporation); W. Wilkening, G. Kiesewetter, S. Mettler, J. Hieber, Robert Bosch GmbH; H. Wolf, Fraunhofer-Institut für Zuverlässigkeit un Mikrointegration (IZM); W. Fichtner, Swiss Federal Institute of Technology (ETHZ)
ESD-level Circuit Simulation – Impact of Gate RC-Delay on HBM and CDM Behavior

J. Lee, S. Kang, University of Illinois; Y. Huh, J-W Chen, P. Bendix, LSI Logic Corporation
Chip-Level Simulation for CDM Failures in Multi-Power ICs

M. Baird, Arizona State University and Motorola; R. Ida, Motorola
Verify ESD: A Tool for Efficient Circuit Level ESD Simulations of Mixed-Signal ICs

A. Wallash, J. Hillman, Quantum Corporation; D. Wang, Nonvolatile Electronics, Inc.
ESD Evaluation of Tunneling Magnetoresistive (TMR) Devices

W. Lukaszek, Wafer Charging Monitors, Inc.
Wafer Charging in Process Equipment and Its Relationship to GMR Heads Charging Damage

E. Granstrom, R. Cermak, P. Tesarek, N. Tabat, Seagate Recording Head Operations
Floating Gate EEPROM as EOS Indicators During Wafer-Level GMR Processing

R. Bordeos, Z. Lianzhu, Shenzhen Kaifa Technology Co. Ltd.; S. Hung, C. Wong, The Hong Kong University of Science & Technology
Investigation of GMR sensor microstructural changes induced by HBM ESD using advanced Microscopy Approach

C. Lam, Read-Rite Corporation
A Study of Static Dissipative Tweezers for Handling Giant Magneto-Resistive Recording Heads

D. Pritchard, Trek Incorporated
Electrostatic Voltmeter and Fieldmeter Measurements on GMR Recording Heads

S. Ramaswamy, J. Carter, J. Stubbart, A. Singh, R. Krasnick, MKPA/Panasonic; F. Gocemen, MKPA/Panasonic (now with Quantum Corporation)
Effect of 1nS to 250 mS ESD Transients on GMR Heads

Multi-Finger Turn-on Circuits and Design Techniques for Enhanced ESD Performance and Width-Scaling [BPR]

K. Kunz, C. Duvvury, H. Shichijo, Texas Instruments, Inc.
5-V Tolerant Fail-Safe ESD Solutions for a 0.18µm Logic CMOS Process
GGSCRs: GGNMOS Triggered Silicon Controlled Rectifiers for ESD Protection in Deep Sub-Micron CMOS Processes

ESD Protection Design for Mixed-Voltage I/O Buffer by Using Stacked-NMOS Triggered SCR Device

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A Study of GMR Read Sensor Induced by Soft ESD Using Magnetoresistive Sensitivity Mapping
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Using PSPICE to Study Transient Propagation in GMR Circuits

I-F Tsu, M. Davis, C. Chang, Seagate Technology
Effect of Low-Level ESD on the Lifetime of GMR Heads

K. Banerjee, Stanford University
Paper Not Available at Press Time
Invited Paper: Interconnect Reliability Under ESD Conditions: Physics, Models, and Design

C. Salling, J. Hu, J. Wu, C. Duvvury, R. Pok, Texas Instruments, Inc.
Development of Substrate-Pumped nMOS Protection for a 0.13µm Technology

R. Gauthier, M. Muhammad, C. Putnam, IBM Microelectronics Semiconductor Research and Development Center; W. Stadler, K. Esmark, P. Riess, Infineon Technologies AG; A. Salman, George Mason University
Evaluation of Diode-Based and NMOS/Lnpn-Based ESD Protection Strategies in a Triple Gate Oxide Thickness 0.13 µm CMOS Logic Technology

D. Pogány, M. Litzenberger, P. Kamvar, E. Gornik, Vienna University of Technology; C. Fürböck, Vienna University of Technology (now with Austria Microsystems); G. Groos, K. Esmark, H. Gossner, M. Stecher, Infineon Technologies
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Electrostatic Discharge and Electrical Overstress on GaN/InGaN Light Emitting Diodes

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H. Berndt, B.E.STAT
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J.M. Kolyer, A.A. Passchier, W.G. Peterson, The Boeing Company
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A. Wallash, Maxtor Corporation
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F. Deng, Z.Y. Teng, W. Li, R. Tao, SAE Magnetics (HK), Ltd.
A Study of GMR Breakdown Damage in Cleaning

A. Siritaratiwat, N. Suwannata, Khon Kaen University; J. Pinnoi, C. Puapaichitkul, Seagate Technology (Thailand) Ltd.
Voltage Raised in Al2O3 Gap of GMR Head in the Deshunting Process

Wafer Charging Evaluation Method of Ion Milling in GMR Head Manufacturing Using Antenna Test Element Group

B. Perry, Maxtor Corporation
ESD Audit Limits and Actual Damage Thresholds: A Theoretical Analysis

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GMR Heads as ESD Detectors-A Direct Assessment of Subtle ESD
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<tr>
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<tr>
<td>2002001</td>
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</tr>
<tr>
<td>2002006</td>
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</tr>
<tr>
<td>2002018</td>
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</tr>
<tr>
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S. Voldman, IBM Communications Research and Development Center (CRDC)

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E. R. Worley, A. Bakulin, Conexant Systems

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Y. Ma, G. P. Li, University of California

A Novel On-Chip ESD Protection Circuit for GaAs HBT RF Power Amplifiers


Test Methods, Test Techniques and Failure Criteria for Evaluation of ESD Degradation of Analog and Radio Frequency (RF) Technology

V. Vashchenko, A. Concannon, M. Ter Beek, P. Hopper, NSC

Technology CAD Evaluation of BiCMOS Protection Structures Operation Including Spatial Thermal Runaway

V. Vassilev, G. Groeseneken, S. Jenei, H. Maes, IMEC and KUL/ESAT; R. Venegas, IMEC; M. Steyaert, KUL/ESAT

Modeling and Extraction of RF Performance Parameters of CMOS Electrostatic Discharge Protection Devices

T. Hamaguchi, T. Ichihara, T. Ozue, Hitachi, Ltd.

Analysis of Barkhausen Noise Failure Caused by ESD in a GMR Head

E. Granstrom, H. Cho, S. Stokes, S. Srn, N. Tabat, Seagate Technology

Effects of ESD Transients on the Properties of GMR Heads

H. Patland, W. Ogle, Integral Solutions Int'l

High Frequency Instabilities in GMR Heads Due to Metal-to-Metal Contact ESD Transients

Y. Soda, K. Kasuga, T. Ozue, Sony Corporation

A Study of Electrostatic Discharge on MR Heads in Digital Tape Systems

J. Himle, A. Wallash, Maxtor Corporation

Tribocharging and Electrical Breakdown at the Magnetic Recording Head-Disk Interface

S. T. Hung, C.Y. Wong, The Hong Kong University of Science and Technology; R. Bordeos, L. Z. Zhang, Shenzhen Kaifa Technology Co. Ltd.

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J. Barth, J. Richner, Barth Electronics, Inc.; K. Verhaege, Sarnoff Europe; M. Kelly, Delphi Delco Electronics Systems; L. G. Henry, Ion Systems, Inc.

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A. Olney, A. Righter, D. Belisle, E. Cooper, Analog Devices, Inc.

A New ESD Model: The Charged Strip Model

H. Hyatt, Hyger Physics, Inc

ESD: Standards, Threats and System Hardness Fallacies

P-Y Tan, I. Manna, Y-C Tan, K-F Lo, P-H Li, Chartered Semiconductor Mfg. Ltd.

A Study of High Current Characteristics of Devices in a 0.13µm CMOS technology

B-C Jeon, S-C Lee, M-C Lee, K-C Moon, J-K Oh, M-K Han, Seoul Nat'l University

ESD Degradation Analysis of Poly-Si N-type TFT Employing TLP (Transmission Line Pulser) Test

K. Suzuki, M. Sato, NEC Corporation

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2002223  D. G. Bellmore, Universal Instruments Corporation
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2002233  K. S. Suh, J. E. Kim, Korea University and InsCon Tech.; T. Y. Kim, Korea University; K. S. Moon, H. S. Moon, Y. K. Park, Samsung Electronics
ESD Protection Materials Using Conductive Polymers

2002240  T. Terashige, Hiroshima International University; D. Ohashi, K. Okano, The Polytechnic University
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2002245  P. Gefter, Ion Systems
Biological Aspects of Clean-Room Ionization

2002250  J. Passi, P. Tamminen, T. Kalliohaka, H. Kojo, K. Tappura, VTT Industrial Systems
ESD Control Tools for Surface Mount Technology and Final Assembly Lines

2002257  G. Boselli, C. Duvvury, V. Reddy, Texas Instruments Inc.
Efficient pnp Characteristics of pMOS Transistors in Sub-0.13 um ESD Protection Circuits [BPP & BPR]

2002267  J. van Zwol, A. van den Berg, T. Smedes, Philips Semiconductors
ESD Protection by Keep-On Design for a 550 V Fluorescent Lamp Control IC with Integrated LDMOS Power Stage

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2002281  D. Tremouilles, LAAS-CNRS and ON Semiconductor; G. Bertrand, L. Lescouzères, ON Semiconductor; M. Bafleur, N. Nolhier, LAAS-CNRS
Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN

2002289  S. Joshi, E. Rosenbaum, University of Illinois at Urbana-Champaign
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2002296  S. Voldman, S. Strang, D. Jordan, IBM Communications Research and Development Center (CRDC)
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2002306  T. Cheung, ReadRite Corporation; L. Baril, A. Wallash, Maxtor Corporation
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2002315  L. Baril, A. Wallash, Maxtor Corporation; T. Cheung, ReadRite Corporation
Standardized Direct Charge Device Model ESD Test For Magnetoresistive Recording Heads II

2002321  R. Bordeos, Shenzhen Kaifa Technology Co. Ltd.
The Practical Approach of ESD Control Solution in Headstack Assembly (HSA) Manufacturing

2002326  B. Perry, T. Porter, W. Boone, Maxtor Corporation
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2002332  Z. Y. Teng, Y. G. Wang, W. Li, R. Tao, SAE Magnetics (HK) Ltd.
ESD Damage by Arcing near GMR Heads

2002337  A. Lai, SAE Magnetics (HK) Ltd.; A. Wallash, Maxtor Corporation
Effect of GMR Recording Head Resistance on Human Body and Machine Model ESD Waveforms

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ESD Characterization of Grounded-Gate NMOS with 0.35 um/18 V Technology Employing Transmission Line Pulser (TLP) Test

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<td>2003008</td>
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<tr>
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<td>Transient Latch-up:Experimental Analysis and Device Simulation</td>
</tr>
<tr>
<td>2003098</td>
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</tr>
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<tbody>
<tr>
<td>2003319</td>
<td>W. Stadler, K. Esmark, Infineon Technologies; K. Reynders, M. Zubeidat, AMIS; M. Graf, Atmel; W. Wilkening, J. Willemen, N. Qu, S. Mettler, M. Etherton, Robert Bosch GmbH; D. Nuernbergk, H. Wolf, H. Gieser, Fraunhofer-IZM; W. Soppa, FH Osnabrück; V. De He</td>
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Y. Ma, Rockwell Scientific; G. P. Li, University of California
InGaP/GaAs HBT DC-20 GHz Distributed Amplifier with Compact ESD Protection Circuits

S. H. Voldman, E. G. Gebreselasie, IBM Microelectronics
Low-Voltage Diode-Configured SiGe:C HBT Triggered ESD Power Clamps Using a Raised Extrinsic Base 200/285 GHz (fT/fMAX) SiGe:C HBT Device

W. Stadler, S. Bargstädt-Franke, T. Brodbeck, R. Gaertner, M. Goroll, H. Goßner, N. Jensen, Chr. Müller, Infineon Technologies AG
From the ESD Robustness of Products to the System ESD Robustness

N. Shimoyama, M. Tanno, S. Shigematsu, H. Morimura, Y. Okazaki, K. Machida, NTT Microsystem Integration Laboratories
Evaluation of ESD Hardness of Fingerprint Sensor LSIs

M. Honda, Impulse Physics Laboratory, Inc.
Induced ESD on Metal Object with a Small Air Gap

K. Shrier, T. Truong, J. Felps, Electronic Polymer, Inc.
Transmission Line Pulse Test Methods, Test Techniques and Characterization of Low Capacitance Voltage Suppression Device for System Level Electrostatic Discharge Compliance

Advanced Modelling and Parameter Extraction of the MOSFET ESD Breakdown Triggering in the 90 nm CMOS Node Technologies

Study of CDM Specific Effects for a Smart Power Input Protection Structure

V. A. Vashchenko, W. Kindt, M. ter Beek, P. Hopper, National Semiconductor Corporation
Implementation of 60V Tolerant Dual Direction ESD Protection in 5V BiCMOS Process for Automotive Application

ESD Protection Design Using a Mixed-Mode Simulation for Advanced Devices

C. Duvvury, R. Steinhoff, G. Boselli, V. Reddy, H. Kunz, S. Marum, R. Cline, Texas Instruments, Inc.
Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers

T. Meuse, R. Barrett, D. Bennett, M. Hopkins, J. Leiserson, Thermo Electron Corporation; L. Ting, J. Schichl, R. Cline, C. Duvvury, H. Kunz, R. Steinhoff, Texas Instruments, Inc.
Formation and Suppression of a Newly Discovered Secondary EOS Event in HBM Test Systems

ESD Design Automation for a 90nm ASIC Design System

N. Guitard, D. Trémouilles, S. Alves, M. Bafleur, LAAS-CNRS; F. Beaudoin, P. Perdu, CNES-THALES; A. Wislez, LCIE ESD Induced Latent Defects in CMOS ICs and Reliability Impact

C. Brennan, J. Sloan, D. Picozzi, IBM Microelectronics
CDM Failure Modes in a 130nm ASIC Technology

D. E. Swenson, Affinity Static Control Consulting, LLC
Compliance Verification: The Critical Component of a Certified ANSI/ESD S20.20 ESD Control Program Plan

V. Kraz, Credence Technologies, Inc.
Notes on Maintaining Sub-1V Balance of an Ionizer

R. Rodrigo, Simco; D. Bellmore, Universal Instrument Corp.; J. Diep, AMD; T. Jarrett, Guidant Corp.; N. Jonassen, Technical University of Denmark; C. Newberg, River’s Edge Technical Service/MicroStat Labs; D. Parkin, IBM Corporation; D. Pritchard, Pritch Company
CPM Study: Discharge Time and Offset Voltage, Their Relationship to Plate Geometry
**2004205**  
J. Brodbeck, Air Force Research Laboratories; B. Grunden, METSS Corporation  
**Humidity Effects on Laminated ESD Worksurface Resistance and Charge Dissipation Properties**

**2004211**  
B-C. Yap, Nanotronix Technology; C. Newberg, MicroStat Laboratories, Inc.  
**Study of "Hot Spots" Arising from Non-Homogeneity in the Micro-Structures of Dissipative Materials**

**2004219**  
D. G. Bellmore, Universal Instruments Corporation  
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**Electrostatic Field Limits and Charge Threshold for Field Induced Damage to Voltage Susceptible Devices**

**2004238**  
E. R. Worley, Conexant Systems  
**Distributed Gate ESD Network Architecture for Inter-Power Domain Signals**

**2004248**  
A. Salman, M. Pelella, S. Beebe, N. Subba, Advanced Micro Devices  
**ESD Protection for SOI Technology Using an Under-The-Box (Substrate) Diode Structure**

**2004255**  
M. G. Khazhinsky, J. W. Miller, M. Stockinger, J. C. Weldon, Freescale Semiconductor, Inc.  
**Engineering Single NMOS and PMOS Output Buffers for Maximum Fault Voltage in Advanced CMOS Technologies [BPR]**

**2004265**  
K-H Lin, M-D Ker, National Chiao-Tung University  
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**2004273**  
J. Li, E. Rosenbaum, University of Illinois at Urbana-Champaign; R. Gauthier, IBM Semiconductor Research and Development Center  
**A Compact, Timed-Shutoff, MOSFET-Based Power Clamp for On-Chip ESD Protection**

**2004280**  
M. Stockinger, J. W. Miller, Freescale Semiconductor  
**Advanced ESD Rail Clamp Network Design for High Voltage CMOS Applications**

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B. Keppens, M. P. J. Mergens, B. Van Camp, K. G. Verhaege, Sarnoff Europe; C. S. Trinh, Sarnoff Corporation; C. C. Russ, Infineon Technologies  
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K. Domanski, Infineon Technologies AG and Nicolaus Copernicus University; S. Bargstädt-Franke, W. Stadler, Infineon Technologies; U. Glaser, Infineon Technologies AG and Integrated Systems Laboratory; W. Bala, Nicolaus Copernicus University  
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**2004338**  
E. Grund, Oryx Instruments Corp., R. Gauthier, IBM Semiconductor Research and Development Center  
**VF-TLP Systems Using TDT and TDRT for Kelvin Wafer Measurements and Package Level Testing**

**2004346**  
Z-Y Teng, M. Mo, W. Li, M-B Wong, S. Chou, SAE Magnetics (HK), Ltd.  
**Breakdown Behavior of TMR Head in ESD Transients**

**2004352**  
L. Baril, B. Higgins, A. Wallash, Maxtor Corporation  
**Effects of ESD Transients on Noise in Tunneling Recording Heads**

**2004356**  
Y. Yang, M. Asheghi, Carnegie Mellon University  
**Comparison of Thermal Response of GMR Sensor Subjected to HBM and CDM Transients**

**2004361**  
S. H. Voldman, IBM Microelectronics; S. Luo, C. Nomura; K. Vannorsdel, N. Feilchenfeld, IBM San Jose  
**Electrostatic Discharge (ESD) Protection of Giant Magneto-resistive (GMR) Recording Heads with a Silicon Germanium Technology**

**2004370**  
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**Dynamic Temperature Rise of Shielded MR Sensors During Simulated Electrostatic Discharge Pulses of Variable Pulse Width**
2004380  T. Ohtsu, K. Kataoka, S. Natori, Hitachi Global Storage Technologies
Improvement of ESD Robustness and Magnetic Stability by Structure of GMR Head

2005001  T. Smedes, J. de Boet, T. Rödle, Philips Semiconductors
Selecting an Appropriate ESD Protection for Discrete RF Power LDMOSTs

2005009  S. Hyvonen, E. Rosenbaum, University of Illinois at Urbana-Champaign
Diode-Based Tuned ESD Protection for 5.25-GHz CMOS LNAs

2005018  M-D Ker, W-L Wu, National Chiao-Tung University
ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process

2005025  S. Thijs, E. Rosenbaum, University of Illinois at Urbana-Champaign
Diode-Based Tuned ESD Protection for 5.25-GHz CMOS LNAs

RF ESD Protection Strategies: Codesign vs. Low-C Protection

2005043  G. Boselli, J. Rodriguez, C. Duvvury, J. Smith, Texas Instruments, Inc.
Analysis of ESD Protection Components in 65nm CMOS Technology: Scaling Perspective and Impact on ESD Design Window [BPR]

2005053  C. Entringer, P. Flatresse, P. Salome, ST Microelectronics Crolles; P. Noutet, F. Azais, LIRMM Physics and Design Optimization of ESD Diode for 0.13 µm PD-SOI Technology

SCR Operation Mode of Diode Strings for ESD Protection

ESD Protection for Advanced CMOS SOI Technologies

2005080  M. Etherton, Robert Bosch GmbH and Swiss Federal Institute of Technology (ETHZ); J. Willemen, W. Wilkening, N. Qu, S. Mettler, Robert Bosch GmbH ; W. Fichtner, Swiss Federal Institute of Technology Verification of CDM Circuit Simulation Using an ESD Evaluation Circuit (ETHZ)

2005090  S. Voldman, E. Gebreselasie, X. F. Liu, D. Coolbaugh, A. Joseph, IBM Microelectronics The Influence of High Resistivity Substrates on CMOS Latchup Robustness

2005100  Y. Huh, K. Min, P. Bendix, Global Technology Leader; V. Axelrad, Sequoia Device Designer, R. Narayan, J-W Chen, L. D. Johnson, LSI Logic Corporation; S. H. Voldman, IBM Microelectronics Corporation Chip Level Layout and Bias Considerations for Preventing Neighboring I/O Cell Interaction-Induced Latch-up and Inter-Power Supply Latch-up in Advanced CMOS Technologies

2005108  S. Voldman, E. G. Gebreselasie, IBM Microelectronics The Influence of Implanted Sub-collector on CMOS Latchup Robustness

2005118  S-F Hsu, M-D Ker, National Chiao-Tung University
Dependences of Damping Frequency and Damping Factor of Bi-Polar Trigger Waveforms on Transient-Induced Latchup

2005126  C.J. Brennan, K. Chatty, J. Sloan, P. Dunn, M. Muhammad, R. Gauthier, IBM Microelectronics Design Automation to Suppress Cable Discharge Event (CDE) Induced Latchup in 90nm CMOS ASICs

2005131  S. H. Voldman, C.N. Perez, A. Watson, IBM Microelectronics Guard Rings: Theory, Experimental Quantification and Design

2005141  J. Barth, J. Richner , Barth Electronics, Inc.; R. A. Ashton, White Mountain Labs; E. Worley, Silicon Voltages Before and After Current in HBM Testers and Real HBM

2005152  D. Trémouilles, S. Thijs, P. Roussel, M. I. Natarajan, V. Vassilev, IMEC vzw; G. Groeseneken, IMEC vzw and Katholieke Universiteit
Transient Voltage Overshoot in TLP testing - Real or Artifact?

2005161  E. Grund, Oryx Instruments Corp. Snapback Device Studies Using Multilevel TLP and Multi-impedance TLP Testers

2005170  C. Goëau, C. Richier, P. Salomé, H. Jaouen, STMicroelectronics; J-P Chante, CEGELY-INSa de Lyon Impact of the CDM Tester Ground Plane Capacitance on the DUT Stress Level

2005178  R. Gaertner, R. Aburano, T. Brodbeck, H. Gossner, J. Schaafhausen, W. Stadler, F. Zaengl, Infineon Technologies AG Partitioned HBM Test – A New Method to Perform HBM Tests on Complex Devices
T. Brodbeck, R. Gaertner, Infineon Technologies AG
Experience in HBM ESD Testing of High Pin Count Devices

J. T. Kinnear, IBM
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D. G. Bellmore, Universal Instruments Corporation; J. Bernier
Characterizing Automated Handling Equipment Using Discharge Current Measurements II

J. Paasi, H. Salmela, VTT Technical Research Centre of Finland; P. Tamminen, J-P Leskinen, T. Viheriakoski, Nokia Corporation
ESD Control in Automated Placement Process

C. Buhler, M. Ritz, J. Starnes, C. Calle, NASA; S. Clements, Appalachian State University
Proposed Test Method to Evaluate the Safety of Materials Using Spark Incendivity

J. A. Montoya, T. J. Maloney, Intel Corporation
Unifying Factory ESD Measurements and Component ESD Stress Testing

W. Farwell, K. Hein, D. Ching, Raytheon Corporation
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ESD Evaluation of the Emerging MuGFET Technology [BPP]

M-D Ker, S-F Hsu, National Chiao-Tung University
Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup Under System-Level ESD Test

Cell Phone GaAs Power Amplifiers: ESD, TLP, and PVS Devices

J. C. Smith, R. A. Cline, G. Boselli, Texas Instruments, Inc.
A Low Leakage Low Cost-PMOS Based Power Supply Clamp with Active Feedback for ESD Protection in 65 nm CMOS Technologies

Y-Y Lin, S. Marum, C. Duvvury, J. Schichl, R. Watson, Texas Instruments, Inc.
Problems with IO to all Other IOs ESD Stress Test: Two Case Studies

T-H Wang, W-H Ho, L-C Chen, Sunplus Technology Co., Ltd.
On-Chip System ESD Protection Design for STN LCD Drivers

A. Wallash, Hitachi Global Storage Technologies
A Study of ESD Damage to a Device Inside a Metal Enclosure

M. Lam, I. E. T. Iben, IBM Corporation
Amplitude and Asymmetry Study using Magnetoresistive Sensitivity Mapping (MSM) on Manufacturing ESD Failures and ESD Simulation Experiments

S. Koike, Tokyo Electronics Trading Co., Ltd.; Y. Soda, Sony Corporation; M. Honda, Impulse Physics Laboratory, Inc.
A Second ESD Threat for ESD Sensitive Devices with Copper Leads

V. Kraz, Credence Technologies, Inc.; P. Tachamaneekorn, D. Napombejar, Seagate Technology (Thailand), Ltd.
EOS Exposure of Magnetic Heads and Assemblies in Automated Manufacturing

I. E. T. Iben, IBM
The Thermodynamics of Physical and Magnetic Changes to AMR Sensors from EOS at Variable Pulse Widths

M. A. Noras, Trek, Inc.; B. Wang, V. Nguyen, Samsung Information Systems America, Inc.
A Miniature Charged Plate for Testing of Charge Accumulation in Hard Disk Drives
2005362 I. E. T. Iben, J. Eaton, IBM
Tribocharging of Materials Used In Tape Heads and Associated ESD Damage

2005372 O. Marichal, G. Wybo, B. Van Camp, P. Vanyssacker, B. Keppens, Sarnoff Europe
SCR Based ESD Protection in Nanometer SOI Technologies

2005380 C. J. Brennan, S. Chang, M. Woo, K. Chatthy, R. Gauthier, IBM Microelectronics
Implementation of Diode and Bipolar Triggered SCRs for CDM Robust ESD Protection in 90 nm CMOS ASICs

2005387 V. A. Vashchenko, P. Lindorfer, P. Hopper, National Semiconductor Corporation
Implementation of High VT Turn-on in Low-Voltage SCR Devices

2005393 B. Van Camp, F. De Ranter, B. Keppens, Sarnoff Europe
Current Detection Trigger Scheme for SCR Based ESD Protection of Output Drivers in CMOS Technologies
Avoiding Competitive Triggering

2005400 Y. Morishita, NEC Electronics Corporation
A PNP-Triggered SCR with Improved Trigger Techniques for High-Speed I/O ESD Protection in Deep Sub-Micron CMOS LSIs

2005407 K. Reynders, P. Moens, AMI Semiconductor
Design and Characterization of a High Voltage SCR with High Trigger Current

PMOSFET-based ESD Protection in 65nm Bulk CMOS Technology for Improved External Latchup Robustness

2005421 A. Salman, S. Beebe, M. Pelella, G. Gilfeather, Advanced Micro Devices
SOI Lateral Diode Optimization for ESD Protection in 130nm and 90nm Technologies

2006001 D. Wang, S. Marum, W. Kemper, D. McLain, Texas Instruments, Inc.
System Event TriggeredLatch-up in IC Chips: Test Issues and Chip Level Protection Design

2006008 C. Ito, W. Loh, LSI Logic Corp.
A New Mechanism for Core Device Failure during CDM ESD Events

ESD Damage due to HBM Stressing of Non-Connected Pins

2006024 H. Kunz, C. Duvvury, J. Brodsky, P. Chakraborty, A. Jahanzeb, S. Marum, L. Ting, J. Schichl, Texas Instruments, Inc
HBM Stress of No-Connect IC Pins and Subsequent Arc-over Events that Lead to Human-Metal-Discharge-Like Events into Unstressed Neighbor Pin [BPR]

2006032 L. Cerati, L. Cecchetto, M. Dissegna, A. Andreini, G. Ricotti, STMicroelectronics
Novel Technique to Reduce Latch-up Risk Due to ESD Protection Devices in Smart Power Technologies

Turn-Off Characteristics of the CMOS Snapback ESD Protection Devices- New Insights and its Implications

2006046 M. Stockinger, J. W. Miller, Freescale Semiconductor, Inc.
Characterization and Modeling of Three CMOS Diode Structures in the CDM to HBM Timeframe

2006054 M. P. J. Mergens, M. T. Mayerhofer, J. A. Willemen, M. Stecher, Infineon Technologies AG
ESD Protection Considerations in Advanced High-Voltage Technologies for Automotive

2006064 V. A. Vashchenko, P. J. Hopper, National Semiconductor Corporation
Dual-Direction Isolated NMOS-SCR Device for System Level ESD Protection

2006069 A. Gendron, P. Renaud, P. Besse, Freescale Semiconductor; C. Salamero, M. Bafleur, N. Nolhier, LAAS-CNRS
Area-Efficient Reduced and No-Snapback PNP-based ESD Protection in Advanced Smart Power Technology

ESD Protection for the High-Voltage CMOS Technologies

2006087 M. Okushima, T. Shinzawa, NEC Electronics Corporation
Operation Analysis and Implementation of CMOS Compatible Vertical Bipolar ESD Protection Devices for Automotive Applications

2006095 Y. Soda, Sony Corporation
A Study of ESD Protection for Helical-scan Tape Heads

2006100 T. Ohtsu, K. Kataoka, N. Koyama, S. Luo, Hitachi Global Storage Technologies
ESD Induced Instability of Pinned Layer in GMR Head
2006253  KP Yan, R. Gaertner, KK Ng, Infineon Technologies (Malaysia) Sdn. Bhd.
Is CO2 Bubbling (Carbonization) a Requirement at Semiconductor Wafer Sawing Process

2006260  C. Nakanishi, Nippon Fusso Co., Ltd.
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2006266  S. Isofuku, Tokyo Electronics Trading Co., Ltd.
Voltage Dependence of Spark Resistance at Low Voltage ESD in Air and Reed Switch

2006274  M. Heer, S. Bychikhin, D. Dubec, D. Pogany, E. Andreini, Vienna University of Technology; M. Dissegna, L. Cerati, L. Zullino, A. Tazzoli, G. Meneghesso, University of Padova
Analysis of the Triggering Behavior of Low Voltage BCD Single and Multi-Finger gc-NMOS ESD Protection Devices

2006284  A. Ille, Infineon Technologies and Universite de Provence-ISEN; W. Stadler, A. Kerber, T. Pompl, T. Brodbeck, K. Esmark, Infineon Technologies; A. Bravaix, Universite de Provence-ISEN
Ultra-thin Gate Oxide Reliability in the ESD Time Domain [BPP]

2006294  A. Tazzoli, V. Peretti, E. Zanoni, G. Meneghesso, University of Padova

2006303  H. Wolf, H. Gieser, Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration; W. Stadler, Infineon Technologies; W. Wilkening, P. Rose, N. Qu, Robert Bosch GmbH
Transient Analysis of ESD Protection Elements by Time Domain Transmission Using Repetitive Pulses

2006310  T.J. Maloney, S.S. Poon; Intel Corporation
Using Coupled Lines to Produce Highly Efficient Square Pulses for VF-TLP

A Frequency-Domain VF-TLP Pulse Characterization Methodology and its Application to CDM ESD Modeling

2006325  R. A. Ashton, White Mountain Labs; E. Worley, Silicon Crossing
Pre Pulse Voltage in the Human Body Model

2006334  E.Grund, M. Hernandez, Oryx Instruments
Methods to Remove Anomalies from Human Body Model Pulse Generators

2006342  L. G. Henry, Electronic Polymers, Inc.; R. Narayan, L. Johnson, LSI Logic; M. Hernandez, E. Grund, Oryx Instruments; K. Min, Y. Huh, Global Technology Leader
Different CDM ESD Simulators Provide Different Failure Thresholds from the Same Device Even Though All the Simulators Meet the CDM Standard Specifications

2006353  M. Chaine, Micron Technology, Inc.; T. Meuse, Thermo Electron Corp.; R. Ashton, White Mountain Labs, Inc.; L.G. Henry, Leo C ESD Consultants; Natarajan Mahadeva Iyer, IMEC; J. Barth, Barth Electronics; L. Ting, Texas Instruments, Inc.; H. Gieser, Fraunhofer
HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins

2007001  T. Brodbeck, K. Esmark, W. Stadler, Infineon Technologies AG
CDM Tests on Interface Test Chips for the Verification of ESD Protection Concepts

A Self Protecting RF Output with 2kV HBM Hardness

2007019  K. Bhatia, E. Rosenbaum, University of Illinois at Urbana-Champaign
Layout Guidelines for Optimized ESD Protection Diodes

Design Optimization of Gate-Silicided ESD NMOSFETs in a 45nm bulk CMOS Technology

2007037  M. Okushima, T. Shinzawa, Y. Morishita, NEC Electronics Corporation
Layout Technique to Alleviate Soft Failure for Short Pitch Multi Finger ESD Protection Device

Designing HV Active Clamps for HBM Robustness

Voltage Overshoot Study in 20V DeMOS-SCR Devices

2007058  M. Dissegna, L. Cerati, L. Cecchetto, E. Gevinti, A. Andreini, STMicroelectronics; A. Tazzoli, G. Meneghesso, University of Padova
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<td>W. D. Greason, University of Western Ontario</td>
<td>Analysis of Charge Injection Processes Including ESD in MEMS</td>
</tr>
<tr>
<td>2007132</td>
<td>Y. Soda, Sony Corporation</td>
<td>Modeling of Discharge between Wire and GMR Head</td>
</tr>
<tr>
<td>2007138</td>
<td>M. Lam, W. Bookin, S. Czarnecki, P. Golcher, I.E.T. Iben, R. DJ Wo, IBM</td>
<td>ESD Damage and Solutions in Tape Head Manufacturing</td>
</tr>
<tr>
<td>2007144</td>
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</tr>
<tr>
<td>2007152</td>
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<td>A Study of “Soft Grounding” of Tools for ESD/EOS/EMI Control</td>
</tr>
<tr>
<td>2007158</td>
<td>D. Linten, IMEC vzw and Vrije Universiteit Brussel; S. Thjis, G. Groeseneken, IMEC vzw and Katholieke Universiteit; M. Scholz, IMEC vzw; D. Tremouilles, LAAS-CNRS; M. Sawada, T. Nakaei, T. Hasebe, Hanwa Electronics Ind. Co. Ltd.</td>
<td>Characterization and Modeling of Diodes in sub-45nm CMOS Technologies under HBM Stress Conditions</td>
</tr>
<tr>
<td>2007165</td>
<td>J-R Manouvrier, STMicroelectronics and University of Montpellier II/CNRS; P. Fonteneau, C-A Legrand, STMicroelectronics; P. Nouet, F. Azais, University of Montpellier II/CNRS</td>
<td>Characterization of the Transient Behavior of Gated/STI Diodes and their Associated BJT in the CDM Time Domain</td>
</tr>
<tr>
<td>2007185</td>
<td>A.A. Salman, S. G. Beebe, M. M. Pelella, Advanced Micro Devices</td>
<td>Double Well Field Effect Diode: Lateral SCR-like Device for ESD Protection of I/Os in deep Sub-Micron SOI</td>
</tr>
<tr>
<td>2007192</td>
<td>R. Gaertner, Infineon Technologies</td>
<td>Do We Expect ESD-failures in an EPA Designed According to International Standards? The need for a Process-Related Risk Analysis</td>
</tr>
<tr>
<td>2007198</td>
<td>H. Kitabayashi, H. Muto, Mitsubishi Electric Corp.</td>
<td>Systematic Approach for the Electrification Suppression Using the Effective Work Function</td>
</tr>
<tr>
<td>2007212</td>
<td>KP Yan, R. Gaertner, CY Wong, KK Ng, Infineon Technologies</td>
<td>ESD Concerns in Sawing Wafers with Discrete Semiconductor Devices</td>
</tr>
</tbody>
</table>
2007226 J. D. Sancho, NASA
Quick Check of ESD Bags for Shielding Efficiency

2007231 A. Wallash, Hitachi Global Storage Technologies; V. Kraz, Credence Technologies / 3M
A Comparison of High-Frequency, Voltage, Current Field, and Probes and Implications for ESD/EMI/EOS Auditing

2007237 T. Tanabe, N. Simon, K. Okano, The Polytechnic University; T. Terashige, Hiroshima International Noise Characteristics of MOSFET Ionizer Balance Sensor

T-Diodes-A Novel Plug-and-Play Wideband RF Circuit ESD Protection Methodology

2007250 J. Li, R. Gauthier, K. Chatthy, S. Mitra, H. Li, R. Halbach, C. Seguin, IBM Semiconductor Research and Development Center, X. Wang, IBM ASIC Development Capacitance Investigation of Diodes and SCRs for ESD Protection of High Frequency Circuits in sub-100nm Bulk CMOS Technologies

2007257 S. Muthukrishnan, C. Iverson, N. Peachey, RFMD
A Novel On-Chip Protection Circuit for RFICs Implemented in D-Mode pHEMT Technology

2007264 A. Tazzoli, F. Danesin, E. Zanoni, G. Meneghesso, University of Padova
ESD Robustness of AlGaN/Gan HEMT Devices

2007273 B.C Atwood, Y. (P) Zhou, D. Clarke, T. Weyf, Analog Devices
Effect of Large Device Capacitance on FIDCM Peak Current

2007283 A. Jahanzeb, Y-Y Lin, S. Marum, J. Schichl, C. Duvvury, Texas Instruments
CDM Peak Current Variations and Impact upon CDM Performance Thresholds [BPR]

2007289 A. Gerdemann Freescale Semiconductor; E. Rosenbaum, University of Illinois at Urbana-Champaign; M. Stockinger, Freescale Semiconductor
A Novel Testing Approach for Full-Chip CDM Characterization

2007297 H. Wolf, H. Gieser, Fraunhofer-Institut Zuverlassigkeit in der Microsystems-Technik, D. Walter, Universitat der Bundeswehr
Investigating the CDM Susceptibility of IC’s at Package and Wafer Level by Capacitive Coupled TLP

2007304 N. Lacrampe, F. Caignet, M. Bafleur, N. Nolhier, N. Muraun LAAS-CNRS
Characterization and Modeling Methodology for IC’s ESD Susceptibility at System Level Using VF-TLP Tester

2007311 S. S. Poon, T. J. Maloney, Intel Corporation
Shielded Cable Discharge Induces Current on Interior Signal Lines

2007318 T. Reinvuo, T. Tarvainen, Esju Oy; T. Viheriakoski, Nokia Siemens Networks
Simulation and Physics of Charged Board Model for ESD

2007323 M. Honda, Impulse Physics Laboratory, Inc.
Measurement of ESD-gun Radiated Fields

Reliability Aspects of Gate Oxide under ESD Pulse Stress

2007338 F. Farbiz, E. Rosenbaum, University of Illinois at Urbana-Champaign
Analytical Modeling of External Latchup

2007347 K. Domanski, K. Esmark, W. Stadler, Infineon Technologies AG; M. Heer, D. Pogany, E. Gornik, Vienna University of Technology
External (transient) Latch-Up Phenomena Investigated by Optical Mapping (TIM) Technique

2007357 T. Smedes, N. Guitard, NXP Semiconductors
Harmful Voltage Overshoots Due to Turn-On Behaviour of ESD Protections during Fast Transients [BPP]

2007366 G. Wybo, S. Verleye, B. Van Camp, O. Marchial, Sarnoff Europe
Characterizing the Transient Device Behavior of SCRs by Means of VFTLP Waveform Analysis

2007376 Y. Morishita, M. Okushima, NEC Electronics Corporation
A Low-Leakage SCR Design Using Trigger-PMOS Modulations for ESD Protection

2007385 K. Chatthy, R. Gauthier, M. Abou-Khalil, IBM Systems and Technology Group; D. Alvarez, C. Russ, Infineon Technologies; B. J. Kwon, Samsung LSI
Process and Design Optimization of a Protection Scheme Based on NMOSFETs with ESD Implant in 65nm and 45nm CMOS Technologies
H. Sarbishaei, M. Sachdev, University of Waterloo, O. Semenov, Freescale Semiconductor
A Transient Power Supply ESD Clamp with CMOS Thyristor Delay Element

A Study for ESD Robustness of Cascoded NMOS Driver

D. Tremouilles, LAAS/CNRS ; S. Thijs, G. Groeseneken, IMEC vzw and Katholieke Universiteit; C. Russ, J. Schneider, H. Gossner, Infineon Technologies AG; C. Duvvury, Texas Instruments; N. Collaert, D. Linten, M. Scholz, M. Jurczak, IMEC vzw
Understanding the Optimization of Sub-45nm FinFET Devices for ESD Applications

T. Karp, Vassili Kireev, Dean Tsaggaris, Mohammed Fakhruddin, Xilinx Inc.
Effect of Flip-Chip Package Parameters on CDM Discharge

Guido Notermans, Željko Mrcarica, Ralph Stephan, Dejan Maksimovic, Theo Smedes, Peter de Jong, Hans van Zwol, NXP Semiconductors
Gate Oxide Protection and ggNMOSTs in 65 nm

T. Smedes, Y. Christoforou, NXP Semiconductors
On the Relevance of IC ESD Performance to Product Quality

Robert A. Ashton, Lionel Lescouzeres, ON Semiconductor
Characterization of Off Chip ESD Protection Devices

Melanie Etherton, James Miller, Freescale Semiconductor, Inc.; Victor Axelrod, Haim Marom, Freescale Semiconductor Israel; Tom Meuse, Thermo Fisher Scientific
HBM ESD Failures Caused by a Parasitic Pre-Discharge Current Spike [BPR]

Kathleen Muhonen, Penn State Erie, The Behrend College; Robert Ashton, ON Semiconductor; Jon Barth, Barth Electronics; Michael Chaine, Micron Technology Inc.; Horst Giesen, Fraunhofer IZM; Evan Grund, Grund Technical Solutions LLC; Leo G. Henry, ESD/TLP C
VF-TLP Round Robin Study, Analysis and Results

Jeffrey Lee, Elyse Rosenbaum, University of Illinois at Urbana-Champaign
Voltage Clamping Requirements for ESD Protection of Inputs in 90nm CMOS Technology

Alessio Griffoni, Augusto Tazzoli, Simone Gerardin, Gaudenzio Meneghesso, University of Padova; Eddy Simoen, IMEC; Cor Claeyts, IMEC and Katholieke Universiteit
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Jean-Robert Manouvrier, Pascal Fonteneau, Charles-Alexandre Legrand, Helene Beckrich-Ros, Corinne Richier, STMicroelectronics; Pascal Nouet, Florence Azais, LIRMM,CNRS/Univ Montpellier
A Physics-Based Compact Model for ESD Protection Diodes Under Very Fast Transients

Steffen Holland, Ingo Laasch, Lars Bade, NXP Semiconductors Germany GmbH
Discrete ESD Protection Diode During a System Level Pulse: Comparison of Simulation With Measurements

Madhur Bobde, Shekar Mallikarjunaswamy, Moses Ho, François Hébert, Alpha & Omega Semiconductor
Potential Barrier Based Clamp: A New Device Structure For Low Voltage Triggering

Jean-Robert Manouvrier, Pascal Fonteneau, Charles-Alexandre Legrand, Corinne Richier, Hélène Beckrich-Ros, STMicroelectronics
A Scalable Compact Model of Interconnects Self-Heating in CMOS Technology

Agha Jahanzeb, Charvaka Duvvury, Joe Schichl, James McGee, Steve Marum, Peter Koeppen, Scott Ward, Yen-Yi Lin, Texas Instruments
Single Pulse CDM Testing and its Relevance to IC Reliability

Dejan Maksimovic, Guido Notermans, Theo Smedes, Thomas Keller, NXP Semiconductors; Fabrice Blanc, ARM Grenoble Design Centre
A Methodology for the ESD Test Reduction for Complex Devices

Tilo Brodbeck, Reinhold Gaertner, Wolfgang stadler, Infineon Technologies; Charvaka Duvvury, Texas Instruments
Statistical Pin Pair Combinations - A New Proposal for Device Level HBM Tests

Bruce C. Chou, Timothy J. Maloney, Intel Corporation, Tze Wee Chen, Stanford University This paper is co-copyrighted by Intel Corporation and the ESD Association
Wafer-Level Charged Device Model Testing

Yen-Yi Lin, Jae Park, Charvaka Duvvury, Steve Marum, Tom Diep, Texas Instruments Inc.; Ori Isachar, Shlomy Chaikin, Texas Instruments Israel Ltd.; Ram Chundru, Apple Inc.
The Challenges of On-Chip Protection for System Level Cable Discharge Events (CDE)
<table>
<thead>
<tr>
<th>Paper ID</th>
<th>Authors</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008132</td>
<td>Evan Grund, Grund Technical Solutions LLC; Kathleen Muhonen, Penn State Erie, The Behrend College; Nathaniel Peachey, RFMD</td>
<td>Delivering IEC 61000-4-2 Current Pulses through Transmission Lines at 100 and 330 Ohm System Impedances</td>
</tr>
<tr>
<td>2008142</td>
<td>Arnold Steinman, MKS, Ion Systems; Maciej Noras, University of North Carolina at Charlotte</td>
<td>Static Control Standards in the Semiconductor Industry</td>
</tr>
<tr>
<td>2008148</td>
<td>Stephen Halperin, Stephen Halperin &amp; Associates Ltd.; Ronald Gibson, Celestica Incorporated; John Kinnear, Jr., IBM</td>
<td>Process Capability &amp; Transitional Analysis</td>
</tr>
<tr>
<td>2008168</td>
<td>Paul Holdstock, Holdstock Technical Services</td>
<td>Limitations of Using Resistance Measurements to Qualify Garments For Use in EPA</td>
</tr>
<tr>
<td>2008174</td>
<td>Takashi Terashige, Hiroshima International University; Shouta Ujiie, Michiyio Armura, Kazuo Okano, The Polytechnic University</td>
<td>Electrostatic Control System Using Ceramic Transformer</td>
</tr>
<tr>
<td>2008178</td>
<td>Larry Levit, Alvin Lau, MKS Ion Systems; Bruce Williams, Ronald Slaby, TREK, Inc; Joshua Y.H. Yoo, MKS Korea Co. Ltd.</td>
<td>Considerations for CPM Measurements of Fast Switching Ionizers</td>
</tr>
<tr>
<td>2008185</td>
<td>Yuanheng Zhang, Mark Hyman, Hyperion Catalysis International; Carl Newberg, MicroStat Laboratories, Inc.; Koichi Sagisaka, Yukadenshi Co., Ltd.</td>
<td>Carbon Nanotube Plastic - Packaging Materials for Class 0 Device ESD Protection</td>
</tr>
<tr>
<td>2008191</td>
<td>Tae Young Kim, Tae Hee Lee, Won Jung Kim, Korea University; Jong Eun Kim, Kwang S. Suh, Korea University and InsCon Tech Co. Ltd.</td>
<td>Liquid Crystal Distortion in LCD Panels and Their Solution Using a Conductive Polymer</td>
</tr>
<tr>
<td>2008196</td>
<td>Nicholas Olson, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Vladislav Vashchenko, Peter Hopper, National Semiconductor Corp.</td>
<td>Small Footprint Trigger Voltage Control Circuit for Mixed-Voltage Applications</td>
</tr>
<tr>
<td>2008204</td>
<td>D. Linten, M. Scholz, P. Jansen, IMEC vzw; V. Vashchenko, D. Lafontese, P. Hopper, National Semiconductor; S. Thijs, G. Groeseneken, IMEC vzw and Katholieke Universiteit; M. Sawada, T. Hasebe, HANWA Electronics</td>
<td>Extreme Voltage and Current Overshoots in HV Snapback Devices During HBM ESD Stress</td>
</tr>
<tr>
<td>2008211</td>
<td>Eleonora Gevinti, Lorenzo Cerati, Marco Sambi, Mariano Dissegna, Luca Cecchetto, Antonio Andreini, STMicroelectronics; Augusto Tazzoli, Gaudenzio Meneghesso, University of Padova</td>
<td>Novel 190V LIGBT-Based ESD Protection for 0.35μm Smart Power Technology Realized on SOI Substrate</td>
</tr>
<tr>
<td>2008221</td>
<td>Vadim Issakov, Infineon Technologies Austria AG and University Paderborn; David Johnsson, Yiqun Cao, Michael Mayerhofer, Werner Simburger, Infineon Technologies AG; Marc Tiebout, Infineon Technologies Austria AG; Linus Maurer, Danube Integrated Circuit</td>
<td>ESD Concept for High-Frequency Circuits</td>
</tr>
<tr>
<td>2008228</td>
<td>Junjun Li, Souvick Mitra, Hongmei Li, Michel J. Abou-Khalil, Kiran Chatty, Robert Gauthier, IBM Semiconductor Research and Development Center</td>
<td>Capacitance Investigation of Diode and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies</td>
</tr>
<tr>
<td>2008235</td>
<td>Shuqing Cao, Robert W. Dutton, Stanford University; Akram A. Salman, Stephen G. Beebe, Mario M. Pelella, Advanced Micro Devices; Jung-Hoon Chun, SungKyunKwan University</td>
<td>ESD Device Design Strategy for High Speed I/O in 45nm SOI Technology</td>
</tr>
<tr>
<td>2008242</td>
<td>James Di Sarro, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Vladislav Vashchenko, Peter Hopper, National Semiconductor</td>
<td>A Dual-Base Triggered SCR With Very Low Leakage Current And Adjustable Trigger Voltage</td>
</tr>
<tr>
<td>2008249</td>
<td>Sandeep Sangameswaran, Steven Thijs, Chris Van Hoof, Guido Groeseneken, Ingrid De Wolf, IMEC vzw and KU Leuven; Jeroen De Coster, Dimitri Linten, Mirko Scholz, Luc Haspeslagh, Ann Witvrouw, IMEC vzw</td>
<td>ESD Reliability Issues in Microelectromechanical Systems (MEMS): A Case Study in Micromirrors</td>
</tr>
<tr>
<td>2008258</td>
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<td>Ultra-Fast Transmission Line Pulse Testing of Tunneling and Giant Magnetoresistive Recording</td>
</tr>
<tr>
<td>2008262</td>
<td>Icko Eric Timothy Iben, IBM Almaden Research Center</td>
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</tr>
<tr>
<td>2008272</td>
<td>Augusto Tazzoli, Vanni Peretti, Enrico Autizi, Gaudenzio Meneghesso, University of Padova</td>
<td>EOS/ESD Sensitivity of Functional RF-MEMS Switches</td>
</tr>
</tbody>
</table>
2008281  William D. Greason, University of Western Ontario
Analysis of Charged Device Model (CDM) ESD in MEMS

2008290  Hiroyasu Ishizuka, Yoko Otsuka, Hiroyuki Ikeda, Kazuo Tanaka, Renesas Technology Corporation
A Study of Advanced Technique on RC-Triggered NMOSFET Power Clamp

2008295  S. Thijs, G. Groeseneken, IMEC vzw and Katholieke Universiteit Leuven; C. Russ, H. Gossner, Infineon Technologies AG; D. Trémouilles, LAAS/CNRS; A. Griffoni, University of Padova; D. Linten, M. Scholz, N. Collaert, R. Rooyackers, M. Jurczak, IMEC vzw; M.
Design Methodology of FinFET Devices that Meet IC-Level HBM ESD Targets

2008304  K. Chatty, M. J. Abou-Khalil, J. Li, R. Gauthier, IBM Systems and Technology Group; D. Alvarez, C. Russ, Infineon Technologies
Investigation of ESD Performance of Silicide-Blocked Stacked NMOSFETs in a 45nm Bulk CMOS Technology

2008312  Souvik Mitra, Robert Gauthier, Junjun Li, Michel Abou-Khalil, Chris S. Putnam, Ralph Halbach, Christopher Seguin, IBM Microelectronics Semiconductor Research and Development Center
ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology

2008317  Yorgos Christoforou, Gajanana Deepak, NXP Semiconductors
Active ESD Protection Design Methodology for DC/DC Converters

2008325  Teruo Suzuki, Nobuyoshi Isomura, Fujitsu VLSI Limited; Kenji Hashimoto, Noboru Yokota, Fujitsu Microelectronics Limited; Oliver Marichal, Bart Sorgeloos, Benjamin Van Camp, Bart Keppens, Sarnoff Europe BVBA
CDM Analysis on 65nm CMOS: Pitfalls When Correlating Results Between IO Test Chips and Product Level

2008332  Kentaro Watanabe, Takayuki Hiraoka, Koichi Sato, Toshikazu Sei, Kenji Numata, Toshiba Corporation
New Protection Techniques and Test Chip Design for Achieving High CDM Robustness

2009001  Kaustav Banerjee, Hong Li, Chuan Xu, University of California-Santa Barbara
Prospects of Carbon Nanomaterials in VLSI for Interconnections and Energy Storage

2009011  Ming-Dou Ker, National Chiao-Tung University, I-Shou University; Wen-Yi Chen, National Chiao-Tung University; Wuu-Trong Shieh, I-Ju Wei, ELAN Microelectronics Corporation
New Layout Scheme to Improve ESD Robustness of I/O Buffers in Fully-Silicided CMOS Process

2009017  Juin J. Liou, Slavica Malobabic, David F. Ellis, University of Central Florida; Javier A. Salcedo, Jean-Jacques Hajjar, Yuanzhong Zhou, Analog Devices
Transient Safe Operating Area (TSOA) Definition for ESD Applications

2009028  Lin Lin, Xin Wang, He Tang, Qiang Fang, Hui Zhao, Albert Wang, University of California; Rouying Zhan, Haolu Xie, Chai Gill, Bin Zhao, Freescale Semiconductor; Yumei Zhou, IMECAS; Gary Zhang, Xingang Wang, Skyworks Solution, Inc.
Whole-Chip ESD Protection Design Verification by CAD

2009038  Yasuhiro Fukuda, Tomomi Yamada, Oki Engineering Co., Ltd.; Masanori Sawada, Hanwa Electronic Industry Co., Ltd.
ESD Parameter Extraction by TLP Measurement

2009044  Vladimir Kraz, 3M Company
Origins of EOS in Manufacturing Environment and It's Classification

2009049  KP Yan, CY Wong, CT Ong, Infineon Technologies (Malaysia) Sdn. Bhd.; Reinhold Gaertner, Infineon Technologies
Automatic Handling Equipment - The Role of Equipment Maker on ESD Protection

2009055  Tetsuya Tokunaga, Takashi Ikehata, Ibaraki University; Takashi Terashige, Hiroshima International University; Syamsul Anfin, Kazuo Okano, The Polytechnic University
Space Charge Balance Sensing for Static Control

2009059  A. Griffoni, IMEC vze, University of Padova; S. Thijs, G. Groeseneken, IMEC vzw, Katholieke Universiteit Leuven; C. Russ, Infineon Technologies AG; D. Trémouilles, LAAS/CNRS, University of Toulouse; D. Linten, N. Collaert, L. Witters, IMEC vzw; M. Scholz, IMEC vzw, Vrije Universiteit
Next Generation Bulk FinFET Devices and Their Benefits for ESD Robustness

2009069  Junjun Li, Kiran Chatty, Robert Gauthier, Rahul Mishra, IBM Semiconductor Research and Development Center; Christian Russ, Infineon Technologies
Technology Scaling of Advanced Bulk CMOS On-Chip ESD Protection

2009076  S. Thijs, G. Groeseneken, IMEC vzw, Katholieke Universiteit Leuven; D. Trémouilles, LAAS/CNRS; A. Griffoni, IMEC vzw, University of Padova; C. Russ, Infineon Technologies AG; D. Linten, N. Collaert, R. Rooyackers, IMEC vzw; M. Scholz, IMEC vzw, Vrije Universiteit
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<td>2009247</td>
<td>Michelle Lam, Icko Eric Timothy Iben, Peter Golcher, Wayne McKinley, Ernie Gale, IBM Co.</td>
<td>A Study of ESD Protection Means of Cabled GMR Sensors</td>
</tr>
<tr>
<td>2009257</td>
<td>Augusto Tazzoli, Alberto Gasperin, Alessandro Paccagnella, Gaudenzio Meneghesso, University of Padova</td>
<td>EOS/ESD Sensitivity of Phase-Change-Memories</td>
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<tr>
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<td>A Study of Breakdown Mechanisms in Electrostatic Actuators Using Mechanical Response Under EOS- ESD Stress</td>
</tr>
<tr>
<td>2009273</td>
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<tr>
<td>2009286</td>
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</tr>
<tr>
<td>2009292</td>
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<td>A DRC-Based Check Tool for ESD Layout Verification [BPR]</td>
</tr>
<tr>
<td>2009301</td>
<td>Nathan Jack, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; James Davis, Michael Chaine, Micron Technology, Inc.</td>
<td>HBM Cross Power Domain Failure Due to Secondary Tester Pulse</td>
</tr>
<tr>
<td>2009308</td>
<td>Ingo Laasch, Hans-Martin Ritter, Achim Werner, NXP Semiconductors</td>
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</tr>
<tr>
<td>2009314</td>
<td>Johan Bourgeat, STMicroelectronics, LAAS/CNRS, Universite de Toulouse; Christophe Entringer, Philippe Galy, Pascal Fonteneau, STMicroelectronics; Marie Bafleur, LAAS/CNRS, Universite de Toulouse</td>
<td>Local ESD Protection Structure Based on Silicon Controlled Rectifier Achieving Very Low Overshoot Voltage</td>
</tr>
<tr>
<td>2009322</td>
<td>Yen-Yi Lin, Diodes Incorporated; Charvaka Duvvury, Agha Jahanzeb, Texas Instruments; Vesselin Vassilev, Novorell Technologies</td>
<td>Diode Isolation Concept for Low Voltage and High Voltage Protection Applications</td>
</tr>
<tr>
<td>2009329</td>
<td>S. Thijs, K. Raczkowski, G. Groeseneken, IMEC vzw, Katholieke Universiteit Leuven; D. Linten, IMEC vzw; M. Scholz, IMEC vzw, Vrije Universiteit Brussel; A. Griffoni, IMEC vzw, University of Padova</td>
<td>CDM and HBM Analysis of ESD Protected 60 GHz Power Amplifier in 45 nm Low-Power Digital CMOS</td>
</tr>
<tr>
<td>2009334</td>
<td>Robert Gauthier, Michel Abou-Khalil, Kiran Chatty, Souvick Mitra, Junjun Li, IBM Corporation</td>
<td>Investigation of Voltage Overshoots in Diode Triggered Silicon Controlled Rectifiers (DTSCRs) Under Very Fast Transmission Line Pulsing (VFTLP)</td>
</tr>
<tr>
<td>2009344</td>
<td>V.A. Vashchenko, D.J. LaFonteese, National Semiconductor Corporation</td>
<td>System Level and Hot Plug-in Protection of High Voltage Transient Pins</td>
</tr>
<tr>
<td>2009352</td>
<td>D. Linten, J. Borremans, M. Dehan, IMEC vzw; S. Thijs, G. Groeseneken, IMEC vzw, Katholieke Universiteit Leuven; M. Okushima, NEC Electronics Corporation; M. Scholz, IMEC vzw, Vrije Universiteit Brussel</td>
<td>A 4.5 kV HBM, 300 V CDM, 1.2 kV HMM ESD Protected DC-to-16.1 GHz Wideband LNA in 90 nm CMOS</td>
</tr>
<tr>
<td>2009358</td>
<td>Julien Lebon, Guillaume Jenicot, Peter Moens, ON Semiconductor Belgium; Dionyz Pogany, Sergey Bychkikhin, Institute for Solid State Electronics Vienna University of Technology</td>
<td>IEC vs. HBM: How to Optimize On-Chip Protections to Handle Both Requirements</td>
</tr>
<tr>
<td>2009371</td>
<td>S. Thijs, G. Groeseneken, IMEC vzw, Katholieke Universiteit Leuven; D. Linten, C. Pavageau, IMEC vzw; M. Scholz, IMEC vzw, Vrije Universiteit Brussel</td>
<td>Center Balanced Distributed ESD Protection for 1-110 GHz Distributed Amplifier in 45 nm CMOS Technology</td>
</tr>
<tr>
<td>2009377</td>
<td>Steve Marum, Charvaka Duvvury, Jae Park, Alan Chadwick, Agha Jahanzeb, Texas Instruments, Inc.</td>
<td>Protecting Circuits From the Transient Voltage Suppressor's Residual Pulse During IEC 61000-4-2 Stress</td>
</tr>
<tr>
<td>2009387</td>
<td>Kathleen Muhonen, Penn State Erie, The Behrend College; Nate Peachey, Al Testin, RFMD</td>
<td>Human Metal Model (HMM) Testing, Challenges to Using ESD Guns</td>
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<tr>
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<tr>
<td>2009396</td>
<td>Kathleen Muhonen, Penn State Erie, The Behrend College; Jeffrey Dunniho,</td>
<td>Failure Detection With HMM Waveforms</td>
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<tr>
<td></td>
<td>Anguel Brankov, California Micro Devices; Evan Grund, Grund Technical</td>
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<tr>
<td></td>
<td>Solutions, LLC; Nate Peachey, RFMD</td>
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<tr>
<td>2009405</td>
<td>M. Scholz, G. Vandersteen, IMEC vzw, Vrije Universiteit Brussels; D.</td>
<td>On-Wafer Human Metal Model Measurements for System Level ESD Analysis</td>
</tr>
<tr>
<td></td>
<td>Linten, IMEC vzw; S. Thijs, G. Groeseneken, IMEC vzw, Katholieke</td>
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<td>Universiteit Leuven; M. Sawada, T. Nakaei, T. Hasebe, Hanwa Electronics</td>
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<td>Ind. Co. Ltd.; D. LaFonteese, V. Vashchenko, P. Hopper, National</td>
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<td>Semiconductor</td>
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<td>Toni Viheriakoski, Cascade Metrology; Jukka Hillberg, IonPhasE Oy;</td>
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<tr>
<td>2009419</td>
<td>Wolfgang Stadler, Tilo Brodbeck, Josef Niemesheim, Reinhold Gaertner,</td>
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<td></td>
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<tr>
<td>2010001</td>
<td>Weiying Li, Yu Tian, Linpeng Wei, Chai Gill, Wei Mao, Chuanzheng Wang,</td>
<td>A Scalable Verilog-A Modeling Method for ESD Protection Devices</td>
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<tr>
<td></td>
<td>Freescale Semiconductor</td>
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<td>2010011</td>
<td>Johan Bourgeat, STMicroelectronics, LAAS/CNRS, Universite de Toulouse;</td>
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<tr>
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<td>Christophe Entringer, Philippe Galy, Frank Jezequel, STMicroelectronics;</td>
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<td>Marie Bafleur, LAAS/CNRS, Universite de Toulouse</td>
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<tr>
<td>2010021</td>
<td>Alexandru Romanescu, STMicroelectronics, IMEP-LAHC; Pascal Fonteneau,</td>
<td>A Novel Physical Model for the SCR ESD Protection Device</td>
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<td></td>
<td>Charles-Alexandre Legrand, Jean-Robert Manouvrier, Helene Beckrich-Ros,</td>
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<td></td>
<td>STMicroelectronics; Philippe Ferrari, Jean-Daniel Arould, IMEP-LAHC</td>
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<tr>
<td>2010031</td>
<td>Gianluca Boselli, Akram Salman, Jonathan Brodsky, Hans Kunz, Texas</td>
<td>The Relevance of Long-Duration TLP Stress on System Level ESD Design [BPR]</td>
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<td></td>
<td>Instruments, Inc.</td>
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<tr>
<td>2010041</td>
<td>Vrashank Shukla, Elyse Rosenbaum, University of Illinois at Urbana-Champa</td>
<td>CDM Simulation Study of a System-in-Package</td>
</tr>
<tr>
<td>2010049</td>
<td>Tilo Brodbeck, Wolfgang Stadler, Christian Baumann, Kai Esmark, Krysztof</td>
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<tr>
<td></td>
<td>Domanski, Infineon Technologies AG</td>
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<tr>
<td>2010059</td>
<td>Al Wallash, Hitachi Global Storage Technologies; Vladimir Kraz, BestESD</td>
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</tr>
<tr>
<td></td>
<td>Technical Services</td>
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<tr>
<td>2010065</td>
<td>Lifang Lou, Charvaka Duvvury, Agha Jahanzab, Jae Park, Texas Instruments,</td>
<td>SPICE Simulation Methodology for System Level ESD Design</td>
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<tr>
<td></td>
<td>Inc.</td>
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</tr>
<tr>
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<td>Agha Jahanzab, Lifang Lou, Charvaka Duvvury, Cynthia Torres, Scott</td>
<td>TLP Characterization for Testing System Level ESD Performance</td>
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<tr>
<td></td>
<td>Morrison, Texas Instruments, Inc.</td>
<td></td>
</tr>
<tr>
<td>2010083</td>
<td>Guido Notermans, Dejan Maksimovic, Gerd Vermont, Michiel van Maasakkers,</td>
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<td>Semiconductors</td>
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<tr>
<td>2010091</td>
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<td>An ESD Design Automation Framework and Tool Flow for Nano-scale CMOS Technologies</td>
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<td></td>
<td>Montstream, Souvick Mitra, Kiran Chatty, Amol Joshi, Karen Henderson,</td>
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<td>Nicholas Palmer, Brian Hulse, IBM</td>
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<tr>
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<td>Ziyang Lu, Mentor Graphics Company; David Averill Bell, LSI Corporation</td>
<td>Hierarchical Verification of Chip-Level ESD Design Rules</td>
</tr>
<tr>
<td>2010103</td>
<td>Hans Kunz, Gianluca Boselli, Jonathan Brodsky, Minas Hambardzumyan, Ryan</td>
<td>An Automated ESD Verification Tool for Analog Design</td>
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<td></td>
<td>Eatmon, Texas Instruments, Instruments, Inc.</td>
<td></td>
</tr>
<tr>
<td>2010111</td>
<td>Junjun Li, Robert Gauthier, Amol Joshi, Martin Lundberg, John Connor,</td>
<td>Predictive Full Circuit ESD Simulation and Analysis using Extended ESD Compact Models: Methodology and Tool Implementation</td>
</tr>
<tr>
<td></td>
<td>Shunhua Chang, Souvick Mitra, Mujahid Muhammad, IBM</td>
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<tr>
<td>2010119</td>
<td>Motosugu Okushima, Tomohiro Kitayama, Susumu Kobayashi, Tetsuya Kato,</td>
<td>Cross Domain Protection Analysis and Verification using Whole Chip ESD Simulation</td>
</tr>
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<td></td>
<td>Morhisra Hirata, Renesas Electronics Corporation</td>
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</tr>
<tr>
<td>2010127</td>
<td>Nicolas Monnereau, Fabrice Caignet, David Tremouilles, LAAS/CNRS,</td>
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<td>Universite de Toulouse; Christophe Salamero, ON Semiconductor; Fabrice</td>
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<td>Caignet, LAAS/CNRS</td>
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<tr>
<td>2010137</td>
<td>Sandra Giraldo, ON Semiconductor, LAAS/CNRS, Universite de Toulouse;</td>
<td>Impact of the Power Supply on the ESD System Level Robustness</td>
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<tr>
<td></td>
<td>Christophe Salamero, ON Semiconductor; Fabrice Caignet, LAAS/CNRS</td>
<td></td>
</tr>
</tbody>
</table>
Effects of TVS Integration on System Level ESD Robustness

2010151 Patrice Besse, Jean-Philippe Laine, Alain Salles, Mike Baird, Freescale Semiconductor
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2010157 S. Thijs, D. Linten, P. Jansen, IMEC; M. Scholz, IMEC, Vrije Universiteit Brussels; A. Griffoni, G. Groeseneken, IMEC, Katholieke Universiteit Leuven; C. Russ, W. Stadler, Infineon Technologies AG; D. LaFonteese, V. Vashchenko, A. Concannon, P. Hoppe, National Semiconductor
SCCF-System to Component Level Correlation Factor

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2010177 Yang Yang, Dimitris E. Ioannou, George Mason University; Robert Gauthier, James Di Sarro, Junjun Li, Souvick Mitra, Kiran Chatty, Rahul Mishra, IBM
Pulsed Gate Dielectric Breakdown in a 32 nm Technology under Different ESD Stress Configurations

2010185 Thomas Benoist, STMicroelectronics, CEA-Leti Minatec, IMEP-LAHC; Claire Fenouillet-Beranger, Jean-Luc Huguenin, Stephane Monfray, Pierre Perreau, STMicroelectronics, CEA-Leti Minatec; Nicolas Guittard, Philippe Galy, David Marin-Cudraz, STMicroelectronics
Improved ESD Protection in Advanced FDSOI by using Hybrid SOI/Bulk Co-Integration

2010191 Natarajan Mahadeva Iyer, Jiang Hao, Yap Hin Kiong, Zhang Guo Wei, Xiaoping Wang, Cheng Chao, Purakh Raj Verma, GLOBALFOUNDRIES
Engineering Fully Silicided Large MOSFET Driver for Maximum It1 Performance

2010197 Souvick Mitra, Robert Gauthier, Shunhua Chang, Junjun Li, Ralph Halbach, Chris Seguin, IBM
Maximizing ESD Design Window by Optimizing Gate Bias for Cascoded Drivers in 45 nm and Beyond SOI Technologies

2010203 Shuqing Cao, Robert W. Dutton, Stanford University; Jung-Hoon Chun, Eunji Choi, Sungkyunkwan University; Stephen Beebe, GLOBALFOUNDRIES, Inc.; Warren Anderson, Advanced Micro Devices
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2010211 KP Yan, Reinhold Gaertner, CY Wong, Infineon Technologies
ESD Protection Program at Electronics Industry - Areas for Improvement

2010217 Sean Millar, Xilinx Ireland, Ltd., First Silicon, Ltd.; Jeremy Smallwood, Electrostatic Solutions, Ltd.
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2010225 Arnold Steinman, Electronics Workshop; Leo G. Henry, ESD/TLP Consulting; Marcos Hernandez, Thermo Fisher Scientific
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2010249 Slavica Malobabic, Jun J. Liou, University of Central Florida; Javier A. Salcedo, Alan W. Righter, Jean-Jacques Hajjar, Analog Devices
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2010259 Toshikazu (Toshi) Numaguchi, Sumitomo 3M Co., Ltd.
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2010279 TaeYoung Kim, Korea University; DongSun Kim, JinHo Ju, WonHo Cho, LG Display; JongEun Kim, InsCon Tech Co., Ltd.; Kwang S. Suh, Korea University, InsCon Tech Co., Ltd.
Static Charge Induced Orientation of Liquid Crystals in LCD Panels
2010283 Yiqun Cao, Infineon Technologies, Technische Universitat Dortmund; Ulrich Glaser, Joost Willemen, Matthias Stecher, Infineon Technologies; Stephen Frei, Technische Universitat Dortmund

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2010293 V.A. Vashchenko, A. Strachan, D. LaFonteese, A. Concannon, P. Hopper, National Semiconductor Corporation; D. Linten, M. Scholz, S. Thijs, P. Jansen, G. Groeseneken, IMEC vzw

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2010301 Blerina Aliaj, Juin J. Liou, University of Central Florida; Vladislav Vashchenko, Philipp Lindorfer, Peter Hopper, National Semiconductor Corp.; Andrew Tcherniaev, Maxim Ershov, Silicon Frontline

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2010309 Akram A. Salman, Gianluca Boselli, Hans Kunz, Jonathan Brodsky, Texas Instruments, Inc.

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2010317 Douglas Miller, NNSA; Steven Hudson, Eddie Teague, Xcel Energy

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2010375 Xiaofeng Fan, Michael Chaine, Micron Technology, Inc.

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2010381 Eugene R. Worley, Reza Jalilizeiniali, Sreeker Dundigal, Evan Siansuri, Tony Chang, Vivek Mohan, Xiaonan Zhang, Qualcomm

CDM Effect on a 65 nm SOC LNA

2010389 Nathan Jack, Prashank Shukla, Elyse Rosenbaum, University of Illinois at Urbana-Champaign

Investigation of Current Flow during Wafer-Level CDM using Real-Time Probing

2010399 Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar, Andrew H. Olney, Analog Devices, Inc.; David F. Ellis, Juin J. Liou, University of Central Florida

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2010407 Timothy J. Maloney, Intel Corporation

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2010417 Scott Ward, Keith Burgess, Joe Schichl, Charleston Duvvury, Peter Koeppen, Hans Kunz, Texas Instruments; Evan Grund, Grund Technical Solutions

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2010425 D. Linten, S. Thijs, S-H. Chen, P. Jansen, IMEC; A. Griffoni, G. Groeseneken, IMEC, Katholieke Universiteit Leuven; M. Scholz, IMEC, Vrije Universiteit Brussels; D. LaFonteese, V. Vashchenko, A. Concannon, P. Hopper, National Semiconductor Corporation

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2010433 Augusto Tazzoli, Marco Barbato, Vincenzo Ritrovato, Gaudenzio Meneghesso, University of Padova

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2010459  Icko Eric Timothy Iben, IBM Corp.  
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2010465  Ray Nicanor M. Tag-at, Lloyd Henry Li, Hitachi Global Storage Technologies Philippines Corp.  
*A Study on the Application of On-Chip EOS/ESD Full-Protection Device for TMR Heads*

2010473  Icko Eric Timothy Iben, Gilda Lee, Stanley Czarnecki, Peter Golcher, Michelle Lam, IBM Co.  
*The Effect of ESD on the Performance of Magnetic Storage Drives*

2011001  Chih-Ting Yeh, National Chiao-Tung University, Industrial Technology Research Institute; Yung-Chih Liang, Industrial Technology Research Institute; Ming-Dou Ker, National Chiao-Tung University, I-Shou  
*PMOS-Based Power-Rail ESD Clamp Circuit with Adjustable Holding Voltage Controlled by ESD Detection Circuit*

2011007  Scott Ruth, Michael Stockinger, James W. Miller, Vincent Whitney, Mark Kearney, Sean Ngo, Freescale Semiconductor  
*A CDM Robust 5V Distributed ESD Clamp Network Leveraging Both Active MOS and Lateral NPN Conduction*

2011016  Johan Van der Borght, Sven Van Wijmeersch, SOFICS BVBA; Bert Semeels, ICsense NV; Chris Goodings, Icera, Inc.  
*Protection of a 3.3V Domain and Switchable 1.8V/3.3V I/O in a 40 nm Pure 1.8V Process*

2011022  Junjun Li, Rahul Mishra, Robert Gauthier, IBM; Mayank Shrivastava, Christian Russ, Intel Mobile Communications; Yang Yang, GLOBALFOUNDRIES, Inc.  
*Technology Scaling Effects on the ESD Performance of Silicide-Blocked PMOSFET Devices in Nanometer Bulk CMOS Technologies*

2011027  Steven Thijs, Alessio Griffoni, Dimitri Linten, Thomas Hoffmann, IMEC; Shih-Hung Chen, Guido Groeseneken, IMEC, Katholieke Universiteit Leuven  
*On Gated Diodes for ESD Protection in Bulk FinFET CMOS Technology*

2011035  Amaury Gendron, Chai Gill, Carol Zhan, Mike Kaneshiro, Bill Cowden, Changsoo Hong, Richard Ida, Dung Nguyen, Freescale Semiconductor  
*New High Voltage ESD Protection Devices Based on Bipolar Transistors for Automotive Applications*

2011045  H. Arbess, D. Tremouilles, M. Bafleur, CNRS/laas, Universite de Toulouse  
*High Temperature Operation MOS-IGBT Power Clamp for Improved ESD Protection in Smart Power SOI Technology*

2011053  Shuji Fujiwara, Kiyofumi Nakaya, Tetsuro Hirano, Yosito Okuda, Yuichi Watanabe, SANYO Semiconductor, Co. Ltd.  
*Source Engineering for ESD Robust NLDMOS*

2011059  Mayank Shrivastava, Christian Russ, Harald Gossner, Intel Mobile Communications; S. Bychikhin, D. Pogany, E. Gornik, Vienna University of Technology  
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2011069  Farzan Fabriz, Akram A. Salman, Gianluca Boselli, Texas Instruments  
*Novel Technologies to Modulate the Holding Voltage in High Voltage ESD Protections*

2011076  Alex Gerdemann, James W. Miller, Michael Stockinger, Norman Herr, Allan Dobbin, Reyhan Ricklefs, Freescale Semiconductor, Inc.  
*When Good Trigger Circuits Go Bad: A Case History*

2011082  P. Galy, J. Bourgeat, J. Jimenez, A. Dray, G. Troussier, B. Jacquier, D. Marin-Cudraz, STMicroelectronics  
*8 Matriz Concept for ESD Power Devices, Demonstrators in C45 nm & C32 nm CMOS Technology*

2011088  Katsuhiko Fukasaku, Takashi Yamazaki, Michihiro Kanno, Sony Corporation  
*Origin of H2 Drop Depending on Process and Layout with Fully Silicided ggMOS*

2011094  Mototsugu Okushima, Junji Tsuruta, Renesas Electronics Corporation  
*CDM Secondary Clamp of RX and TX for High Speed SerDes Application in 40 nm CMOS*

2011100  James Karp, Mohammed Fakhruddin, Michael Hart, Richard Li, Fu-Hing Ho, Steven Reilly, Phoumra Tan, Dean Tsaggaris, S.Y. Pai, Xilinx, Inc.  
*Small Footprint ESD Protection of Hot-Swappable I/Os*

2011106  Adam C. Faust, Elyse Rosenbaum, University of Illinois at Urbana-Champaign; Ankit Srivastava, Qualcomm, Inc. (Formerly with University of Illinois)  
*Effect of On-Chip ESD Protection on 10 Gb/s Receivers*

2011116  Steven Thijjs, Dimitri Linten, IMEC; Kuba Raczkowski, Guido Groeseneken, IMEC, Katholieke Universiteit Leuven; Jen-Chou Tseng, Tzu-Heng Chang, Ming-Hsiang Song, Taiwan Semiconductor Manufacturing Company  
*CDM Protection for Millimeter-Wave Circuits*
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<th>Title</th>
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<td>2011123</td>
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</tr>
<tr>
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<td>A SCR-Based ESD Protection for MEMS-Merits and Challenges</td>
</tr>
<tr>
<td>2011140</td>
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<td>Active Clamp Implementation in Complementary BiCMOS Process with High Voltage BJT Devices</td>
</tr>
<tr>
<td>2011163</td>
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</tr>
<tr>
<td>2011171</td>
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<td>A Positive Exploitation of ESD Events: Micro-Welding Induction on Ohmic MEMS Contacts</td>
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This paper is co-copyrighted by Intel Corporation and the ESD Association.
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20159A1 Dave Clarke, Stephen Heffernan, Analog Devices, Inc.
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20159A2 Jorge Loayza, STMicroelectronics, Université de Lyon; Nicolas Guittard, Blaise Jacquier, Alexandre Dray, Divya Agarwal, Vicky Batra, STMicroelectronics; Bruno Allard, Luong Viét Phung, Université de Lyon
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20159A3 Manjunatha Prabhu, Jian-Hsing Lee, Mahadeva Iyer Natarajan, Vasantha Kumar, Tsung-Che Tsai, Li Zhiqing, Dominic Thurmer, GLOBALFOUNDRIES
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2015RCJ Katsuyuki Takahashi, Akira Goto, Shinichi Yamaguchi, Tomokatsu Saito, Kensuke Sakamoto, Hidemi Nagata, Shishido Electrostatic, Ltd.
RCJ Best Paper
Development of a Perfectly Balanced Electrostatic Eliminator Utilizing an Intermittent Pulse AC Voltage Power Supply

20161A1 M. Scholz, S. Steudel, K. Myny, S. Chen, G. Hellings, D. Linten, imec; R. Boschke, imec, KU Leuven
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20161A3 Jian-Hsing Lee, Natarajan Mahadeva Iyer, Ruchil Jain, Manjunatha Prabhu, GLOBALFOUNDRIES, Inc.
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20161A4 Da-Wei Lai, Shuang Zhao, Jian Gao, Theo Smedes, NXP Semiconductors
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20165B1  Efraim Aharoni, TOWERJAZZ, Kinneret College on the Sea of Galilee; Avi Parvin, Yosi Vaserman, TOWERJAZZ; Evan Grund, Grund Technical Solutions, Inc.

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Todd Mitchell, Vladislav Vashchenko, Maxim Integrated; Terry Meeks, Mentor Graphics

HV Latch-up - Power Analog ICs Co-Design with Block Level Verification

David Alvarez, Michael Asam, Infineon Technologies; Nitesh J. Trivedi, formerly Infineon Technologies

Influence of Self-Heating on ESD Current Distribution in Metal Lines

Darwin Li, Jianchi Zhou, Ahmad Hosseinbeig, David Pommerenke, Missouri University of Science and Technology

Transient Electromagnetic Co-Simulation of Electrostatic Air Discharge

Milova Paul, B. Sampath Kumar, Mayank Shrivastava, Indian Institute of Science; Christian Russ, Harald Gossner, Intel Deutschland GmbH

FinFET SCR: Design Challenges and Novel Fin SCR Approaches for On-Chip ESD Protection

Michael Ammer, Infineon Technologies AG, Universität der Bundeswehr Munchen; Kai Esmark, Friedrich zur Nieden, Andreas Rupp, Yiqun Cao, Infineon Technologies AG; Martin Sauter, Linus Maurer, Universität der Bundeswehr Munchen

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Michael Ammer, Infineon Technologies AG, Universität der Bundeswehr Munchen; Kai Esmark, Friedrich zur Nieden, Andreas Rupp, Yiqun Cao, Infineon Technologies AG; Martin Sauter, Linus Maurer, Universität der Bundeswehr Munchen

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Ilse Backers, Bart Sorgeloos, Benjamin Van Camp, Olivier Marichal, Bart Keppens, Sofics BVBA

Low Capacitive Dual Bipolar ESD Protection

Low Capacitive Dual Bipolar ESD Protection
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**Chip-Level ESD-Induced Noise on Internally and Externally Regulated Power Supplies**

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**A Novel, SCR-Based, Distributed Power Supply ESD Network for Advanced CMOS Technologies**

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