

ESD Target Levels the Industry Council

By The ESD Association

An Industry Council on ESD Target Levels was established in 2006 when a few IC companies decided to understand why during the product qualification process, at every corporation, passing the ESD test is a frequent bottleneck for customer acceptance. The pattern was the same – an IC product fails to meet the historically accepted ESD requirements, leading to several design cycles in order to meet the specified ESD expectations, and at the same time the task became more and more time consuming as the technologies advanced. Simultaneous to this, most companies experienced for different reasons, multiple products supplied to the market that did not meet the same ESD requirements. No one observed reliability problems with these products. The *ad hoc* Council thus embarked on a mission to re-examine and establish safe and practical ESD levels that are necessary for manufacturing and target levels that will have minimum impact on circuit performance requirements.

The original participants included Infineon, Texas Instruments, Philips (now NXP), Barth Electronics, Thermo-Keytek (now Thermo-Fisher Scientific), and Sarnoff-Europe (now SOFICS). What started as a small group that met in Belgium to brainstorm how to approach the ESD qualification issues has now expanded into a worldwide body of 40+ members representing IC suppliers, consultants, contractors, advisers, foundries, as well as some customers. Many in the industry were confused in the beginning if this was a new standardization body. Soon it became clear that the Council consists of individual experts who represent their own companies in conducting studies for the common cause and for interacting with the standardization bodies such as JEDEC and ESDA. The purpose of the Council is to make recommendations through publications of white papers.

The mission of the Industry Council on ESD Target Levels is essentially to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by the downscaled process technologies on practical protection designs, the Council's purpose is to provide consolidated recommendations for future ESD target levels. The Council Members and Associates promote these recommended targets to be adopted as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies. With this original mission, the Council has produced two key white papers [1, 2] on HBM/MM and CDM requirements, during 2007 and 2008 respectively, both published on the ESDA website. The papers were also published as JEDEC documents JEP155 (HBM) and JEP157 (CDM).

These papers have eventually set in motion a realistic view of the required ESD levels for modern IC production. The major conclusions were that as long as all basic ESD control

methods, which are mandatory for IC manufacturing and handling, are followed: 1) HBM levels between 500V to 2kV are safe for qualification, 2) CDM levels of a minimum 250V are safe but lower than this requires more detailed control implementation at the production sites, and 3) MM is a redundant test as meeting the HBM/CDM test provides sufficient protection for IC handling and production. Both of these papers have been accepted by the ESDA and the JEDEC Boards and are now available as public documents.

The nature of the IC industry dictates that circuit performance and reliability are both of paramount importance while the market demands can result in the former overriding the latter. Fortunately in the case of ESD component level requirements, it has been demonstrated by the Council that there is plenty of safe margin that allows the ESD levels to be reduced without reliability consequences. Collection of extensive data and evaluation of modern factory mandatory control methods have established that new ESD levels (500V or greater for HBM and 250V or greater for CDM) allow safe manufacturing and are compatible for IC designs to achieve data rates exceeding 15 Gb/Sec. High performance components (e.g., internet applications) dictate these new levels to be adopted.

Another aspect of much misunderstanding in the industry concerns the requirements for system level ESD protection and its coupling with component level requirements. For example, some IC customers commonly believe that requiring high levels of HBM protection (for example, 8kV) would essentially enable the systems to achieve ESD protection of 8kV as defined by the IEC test. The purpose of testing under these two models vastly differs and a more realistic approach is needed to efficiently design for system level ESD. The Council has recently published a third white paper [3] to not only clarify these misconceptions but also point to a more desired approach for system level ESD protection design strategy, taking into consideration the chip functions (such as HDMI, USB, Ethernet, etc.). The third white paper was also published as a JEDEC document JEP161. The conclusions from this white paper are: 1) requiring high levels of HBM or CDM would not protect at system level, and 2) the optimum strategy for system level protection requires communication between the supplier and the system designer to realize a co-design concept of printed circuit board (PCB) and IC. Based on adequate component level ESD, (which is safe if the minimum necessary levels discussed above are met) the clear attention must be for protecting the entire system on a PCB. To this effect, the Council is now in the process of writing an extension of White Paper 3 examining the full details as well as the nuances of system level ESD that include EMC and EMI considerations.

The Council is very fortunate to have not only eager participation from dedicated experts, but also excellent support from the member organizations' management. The support and encouragement of the ESD Association and JEDEC organization is the key to make credible changes that have impact and acceptance. With the advancement towards sub-50 nm technologies, realistic and efficient ESD will be the new trend. The Council is now proposing a roadmap for component ESD levels for advances to 22nm and beyond. The ESDA is using these inputs to announce an ESD technology roadmap [4] that calls for attention to much better factory control methods to be adopted.

Through this article we are appealing to the industry to come together to address ESD as a common problem for the customer, the supplier, and the consultant alike. We hope the unprecedented initiative taken by the Council will have long lasting impact. If anyone is interested in joining the Council for this common cause they are encouraged to contact the Council chairs, Charvaka Duvvury (c-duvvury@ti.com) or Harald Gossner (harald.gossner@intel.com).

[1] *White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements.*

http://www.esda.org/documents/WhitePaper1_HBM_MM_2010.pdf

[2] *White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements*

<http://www.esda.org/documents/IndustryCouncilWhitePaper2.pdf>

[3] *White Paper 3: System Level ESD Part I: Common Misconceptions and Recommended Basic Approaches*

<http://www.esda.org/documents/IndustryCouncilWhitePaper3.pdf>

[4] *Electrostatic Discharge (ESD) Technology Roadmap – Revised April 2010*

<http://esda.org/documents/2010ElectrostaticDischargeRoadmap.pdf>

Founded in 1982, the ESD Association is a professional voluntary association dedicated to advancing the theory and practice of electrostatic discharge (ESD) avoidance. From fewer than 100 members, the Association has grown to more than 2,000 members throughout the world. From an initial emphasis on the effects of ESD on electronic components, the Association has broadened its horizons to include areas such as textiles, plastics, web processing, cleanrooms, and graphic arts. To meet the needs of a continually changing environment, the Association is chartered to expand ESD awareness through standards development, educational programs, local chapters, publications, tutorials, certification, and symposia.